

MAXWELL INDUSTRIAL APPLICATION BOARD

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REV	E4
VER	1.0

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Size: PROC064

Date: Thursday, August 23, 2018

Rev: E4

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REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.1	17th AUG 2018	Drafted from Rev E3, Ver 1.0 schematics.	Mistral Design Team	AJIT MB	AJIT MB
0.2	17th AUG 2018	Added TX_CLK jumper options to connect MII& RGMII mode and added Pullup on IDK_SPI_CS _n _3V3 net	Mistral Design Team	AJIT MB	AJIT MB
0.3	23rd AUG 2018	Added Test Points on EDC_SYNC_OUT signals	Mistral Design Team	AJIT MB	AJIT MB
1.0	23rd AUG 2018	Baselined	Mistral Design Team	AJIT MB	AJIT MB

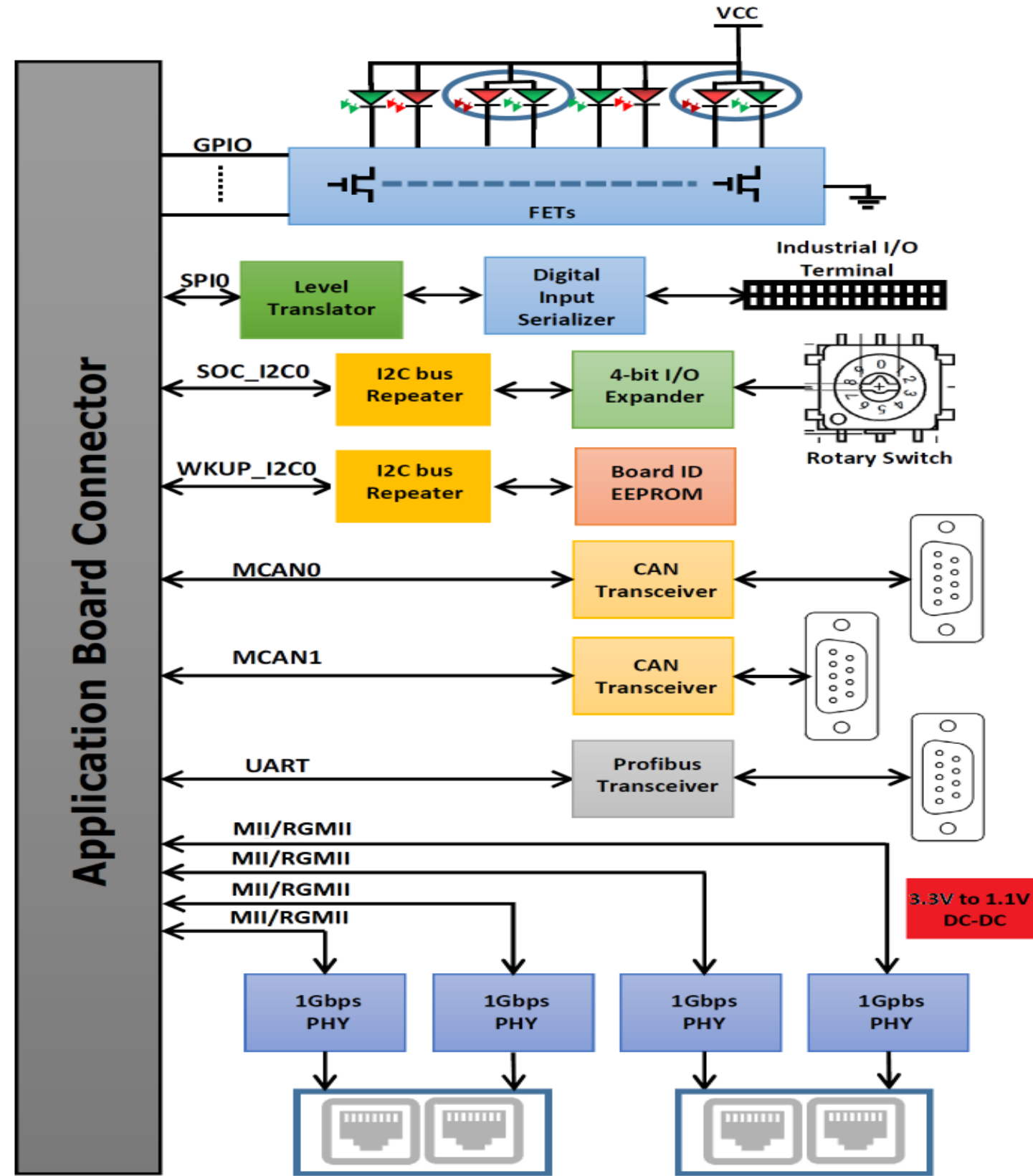
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Title: REVISION HISTORY

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BLOCK DIAGRAM



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Title: BLOCK DIAGRAM

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D

C

B

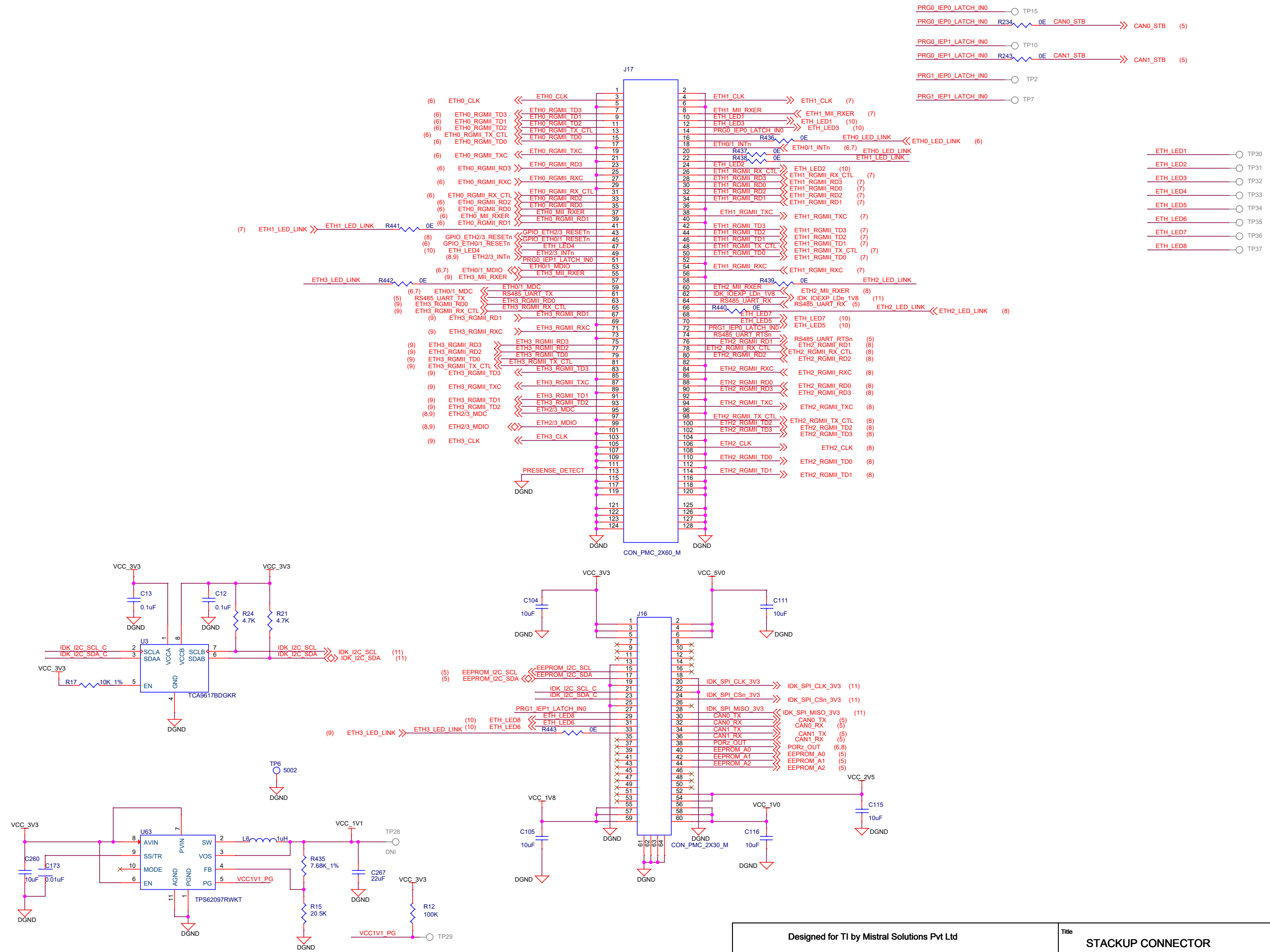
A

D

C

B

A

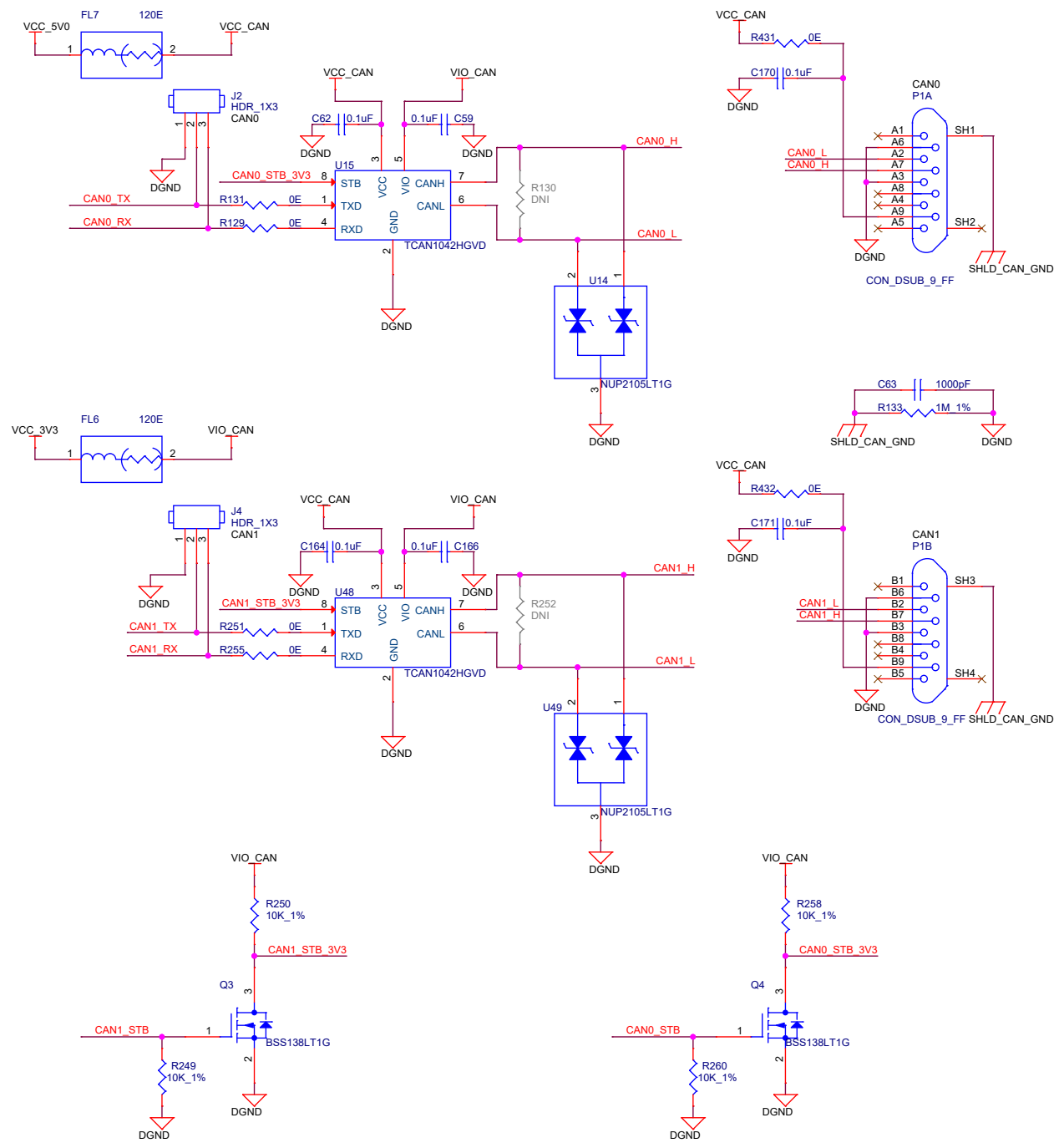


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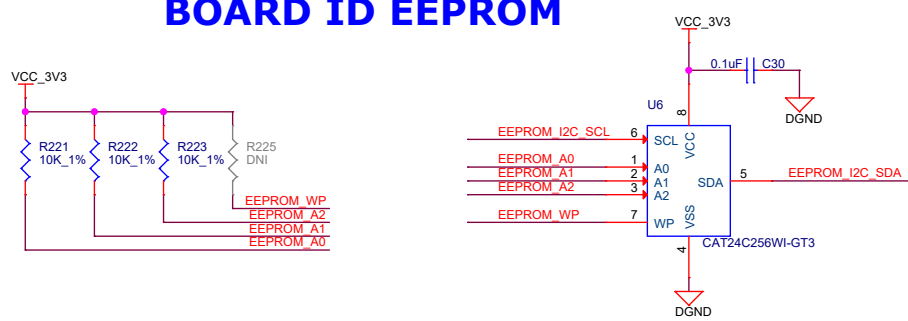
TEXAS INSTRUMENTS **MISTRAL**

Title		STACKUP CONNECTOR	
Size	PROC064	Rev	
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CAN INTERFACE

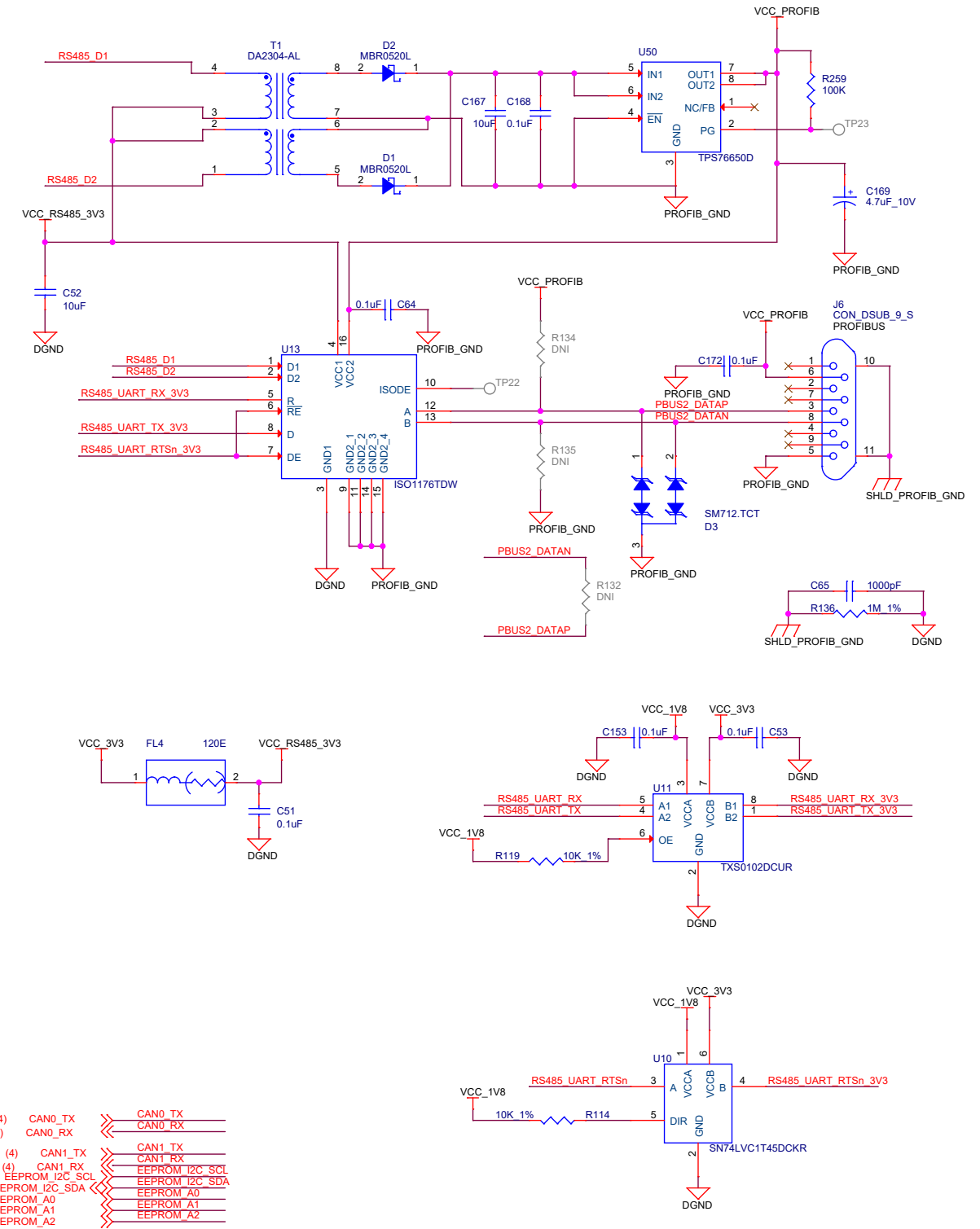


BOARD ID EEPROM



I2C address: 0x52h or Set by CP board

RS485 INTERFACE

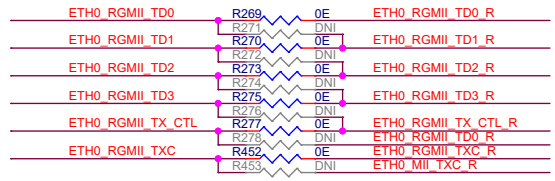
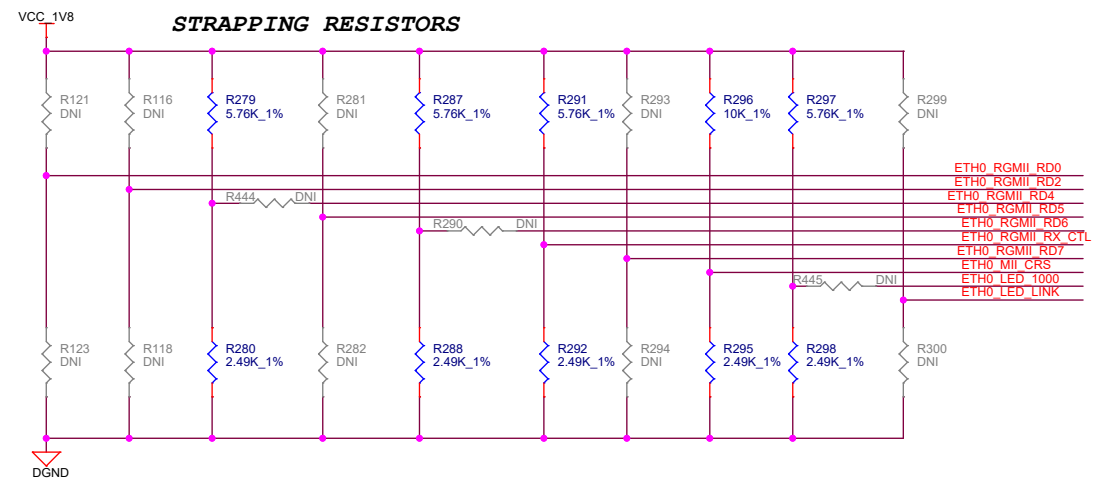
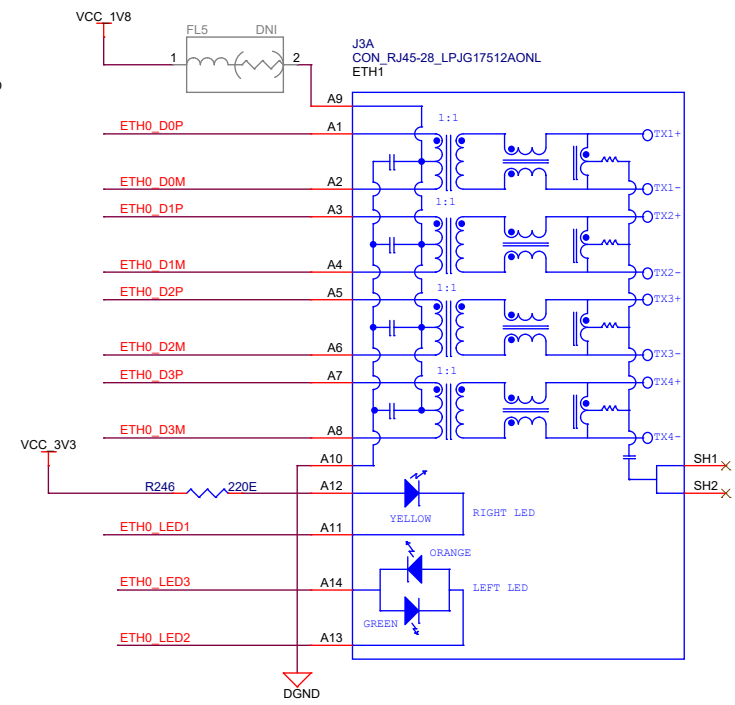
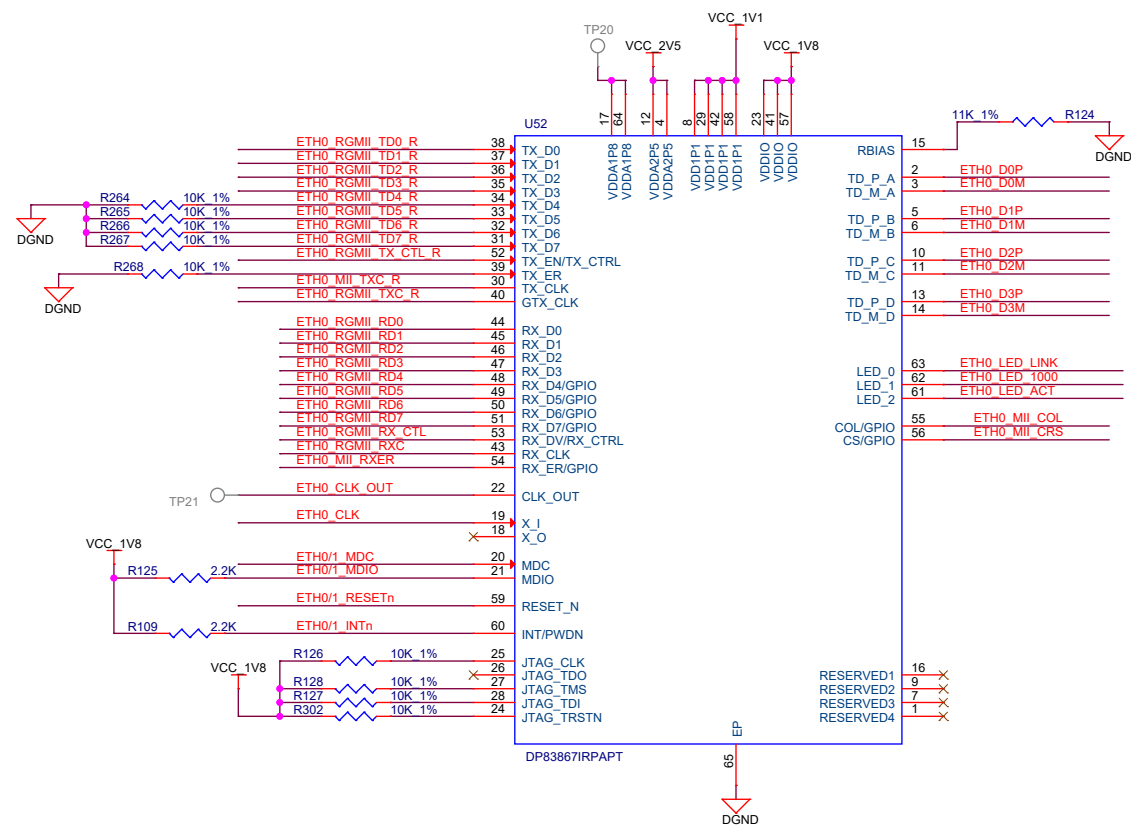
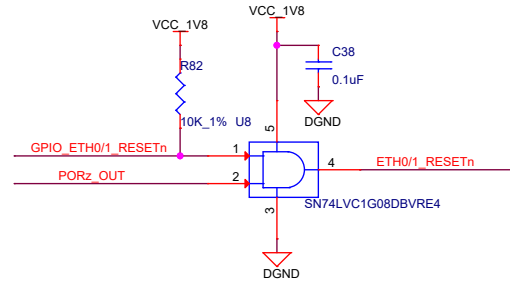
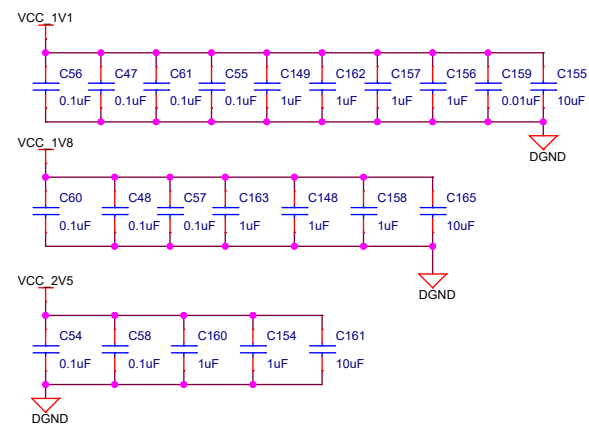


- (4) CAN0_TX <>> CAN0_TX
- (4) CAN0_RX <>> CAN0_RX
- (4) CAN1_TX <>> CAN1_TX
- (4) CAN1_RX <>> CAN1_RX
- (4) EEPROM_I2C_SCL <>> EEPROM_I2C_SCL
- (4) EEPROM_I2C_SDA <>> EEPROM_I2C_SDA
- (4) EEPROM_A0 <>> EEPROM_A0
- (4) EEPROM_A1 <>> EEPROM_A1
- (4) EEPROM_A2 <>> EEPROM_A2
- (4) RS485_UART_RX <>> RS485_UART_RX
- (4) RS485_UART_RTSn <>> RS485_UART_RTSn
- (4) RS485_UART_TX <>> RS485_UART_TX
- (4) CAN0_STB <>> CAN0_STB
- (4) CAN1_STB <>> CAN1_STB

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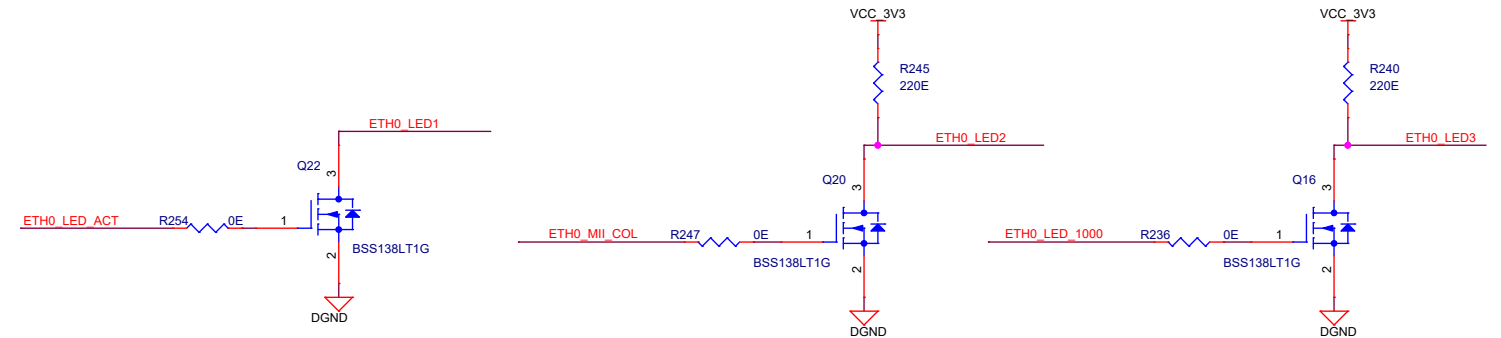
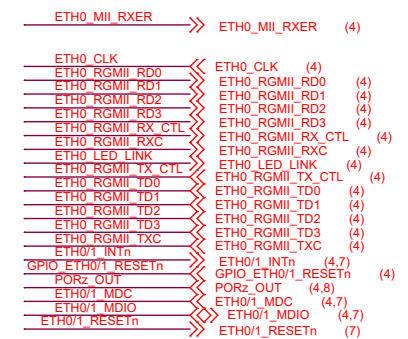
Title		CAN/RS485/BOARD ID INTERFACE	
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RGMII Mode:
 Mount : R269, R270, R273, R275, R277, R452
 Unmount : R271, R272, R274, R276, R278, R290, R444, R445, R453

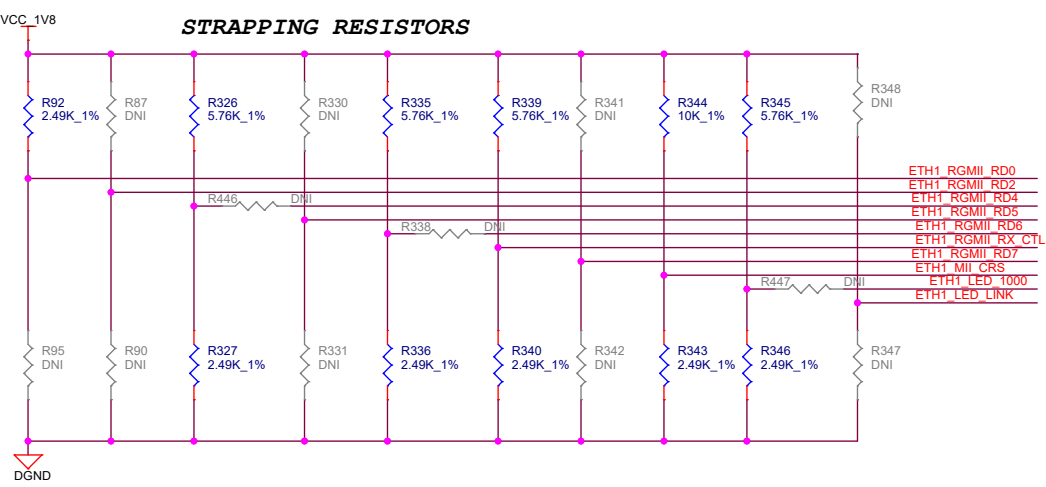
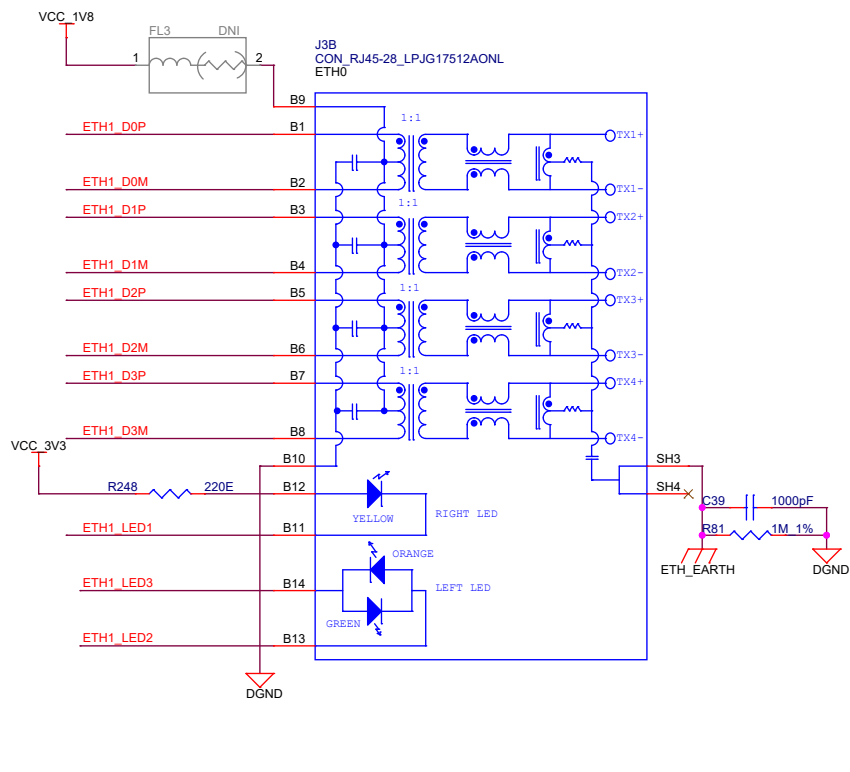
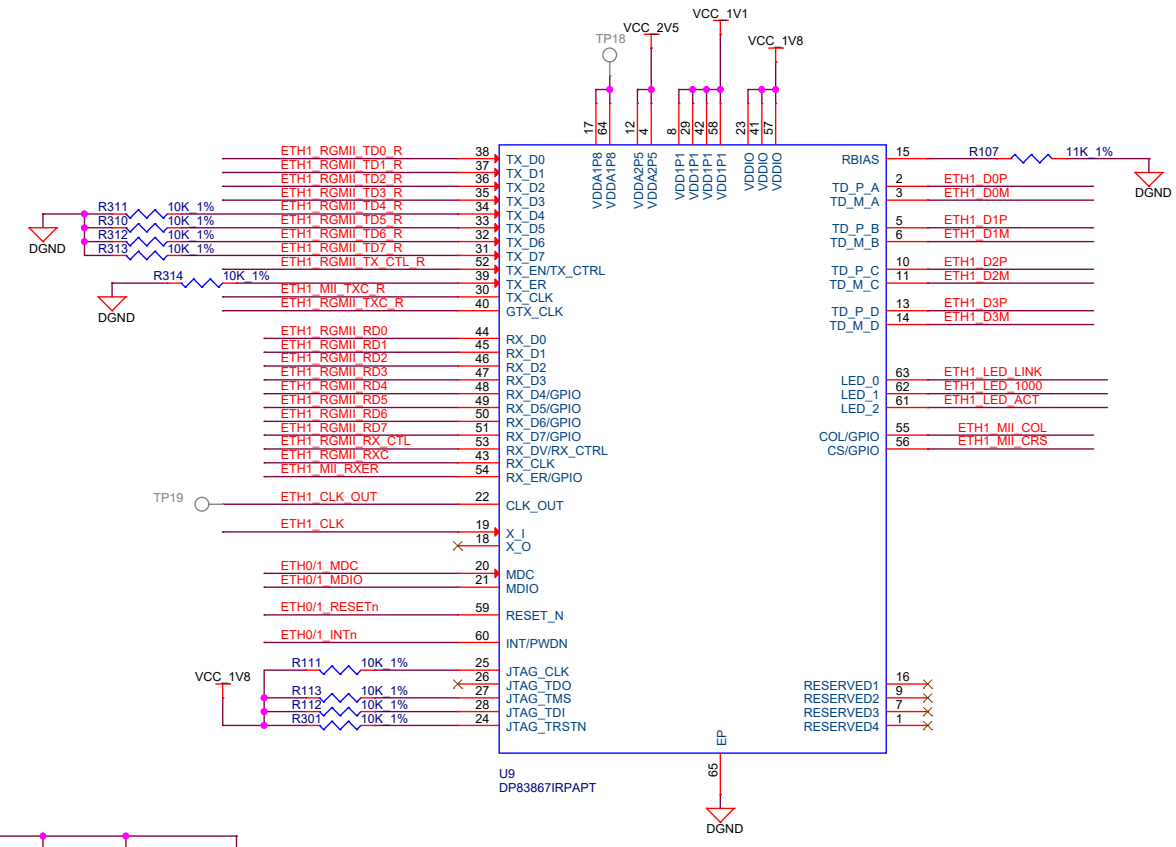
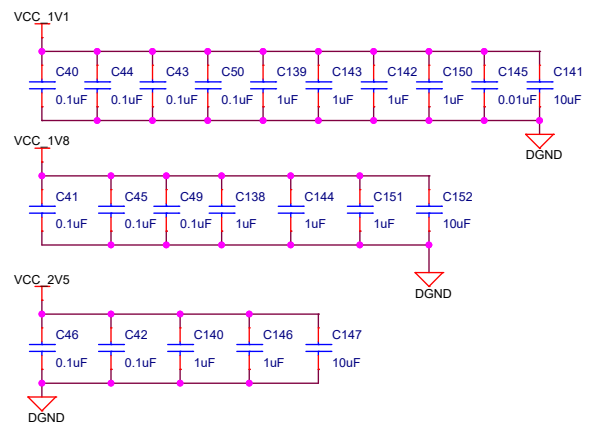
MII Mode:
 Mount : R271, R272, R274, R276, R278, R290, R444, R445, R453
 Unmount : R269, R270, R273, R275, R277, R452

PHY ADD = 00000
 Auto_neg = Enabled
 ANEGSel 10/100/1000

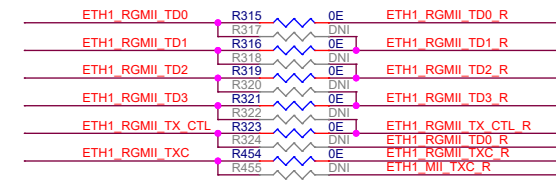


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Title		RGMII ETHERNET PHY 0	
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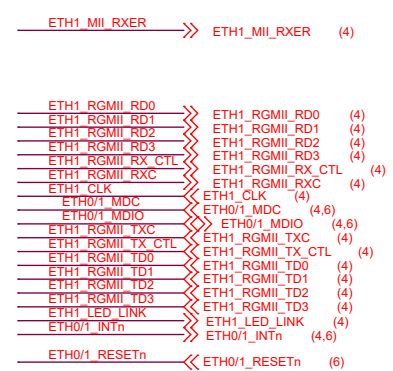
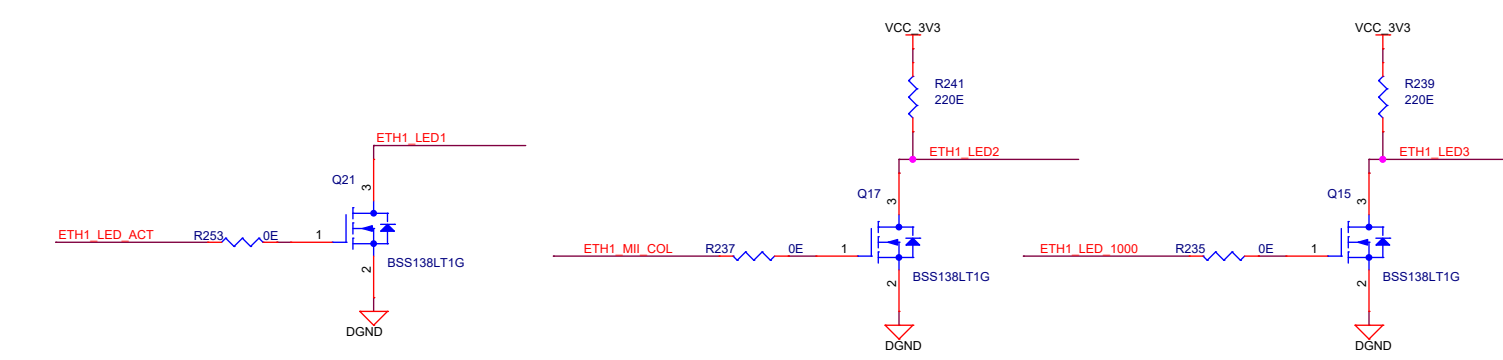


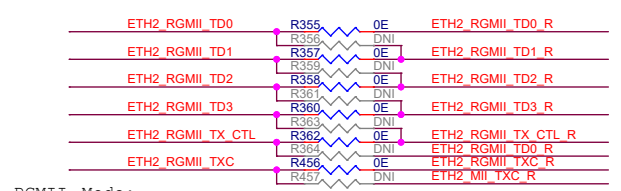
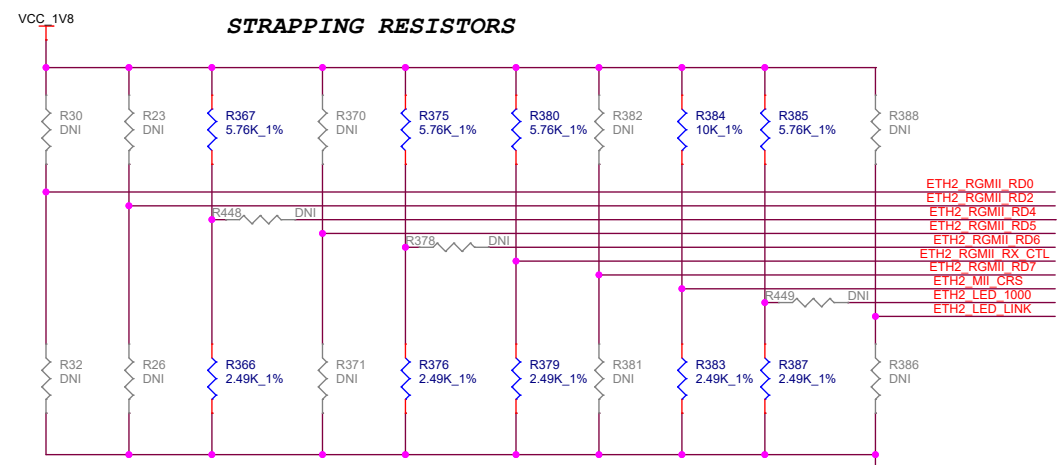
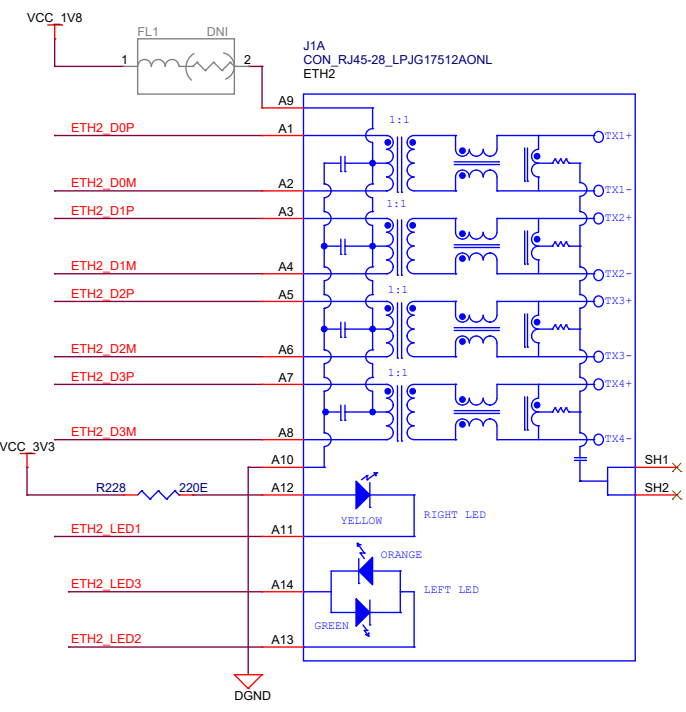
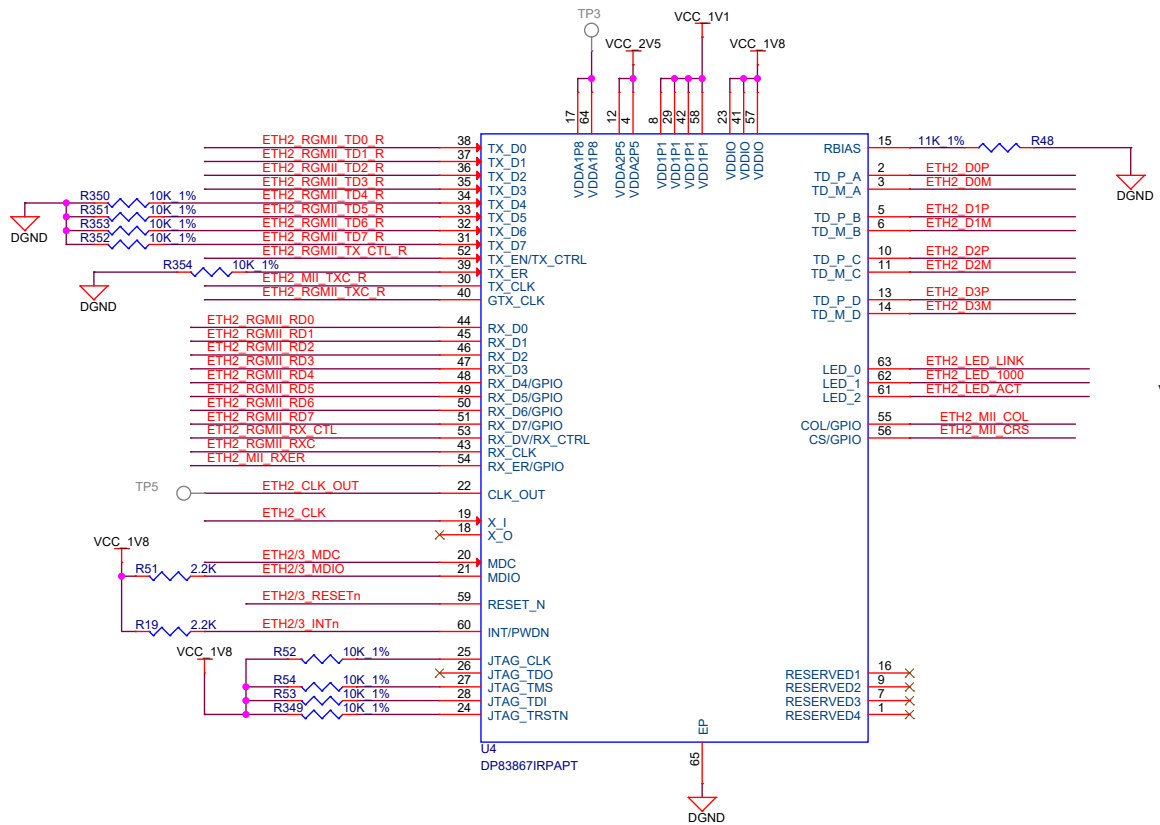
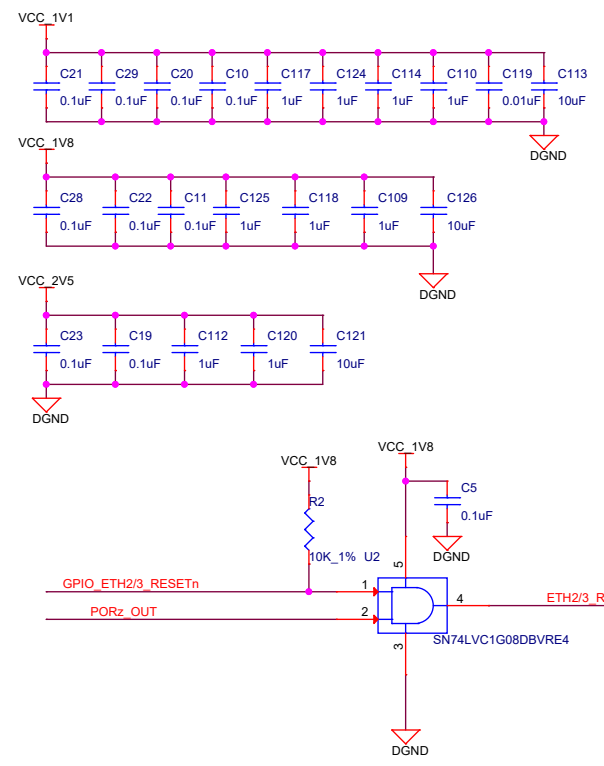
PHY ADD = 00011
 Auto_neg =Enabled
 ANEGsel 10/100/1000



RGMII Mode:
 Mount : R315, R316, R319, R321, R323, R454
 Unmount : R317, R318, R320, R322, R324, R338, R446, R447, R455

MII Mode:
 Mount : R317, R318, R320, R322, R324, R338, R446, R447, R455
 Unmount : R315, R316, R319, R321, R323, R454



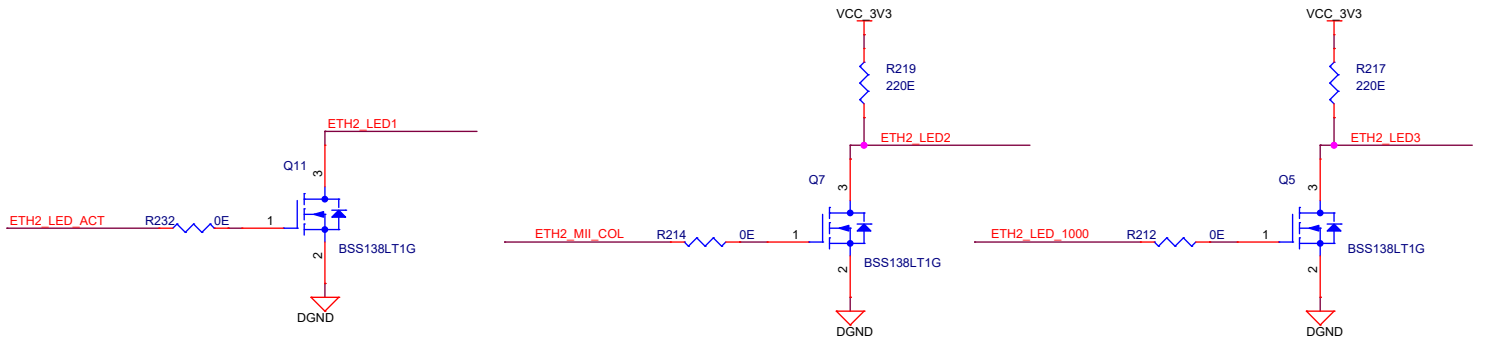


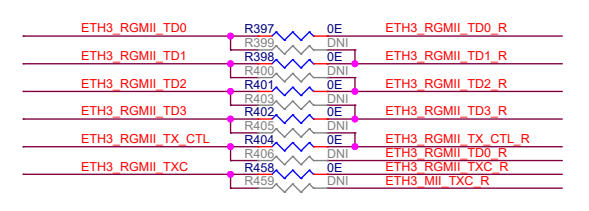
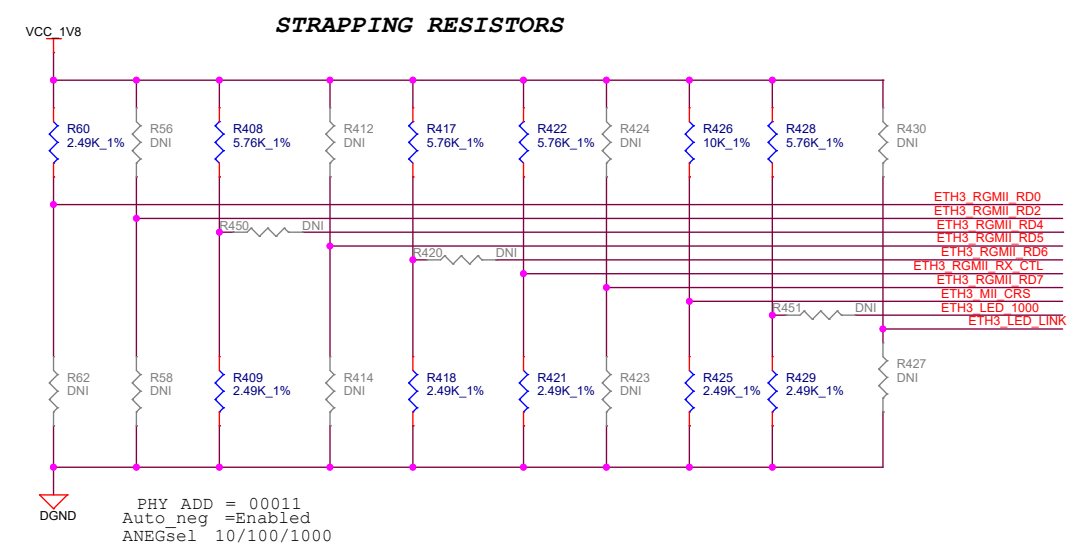
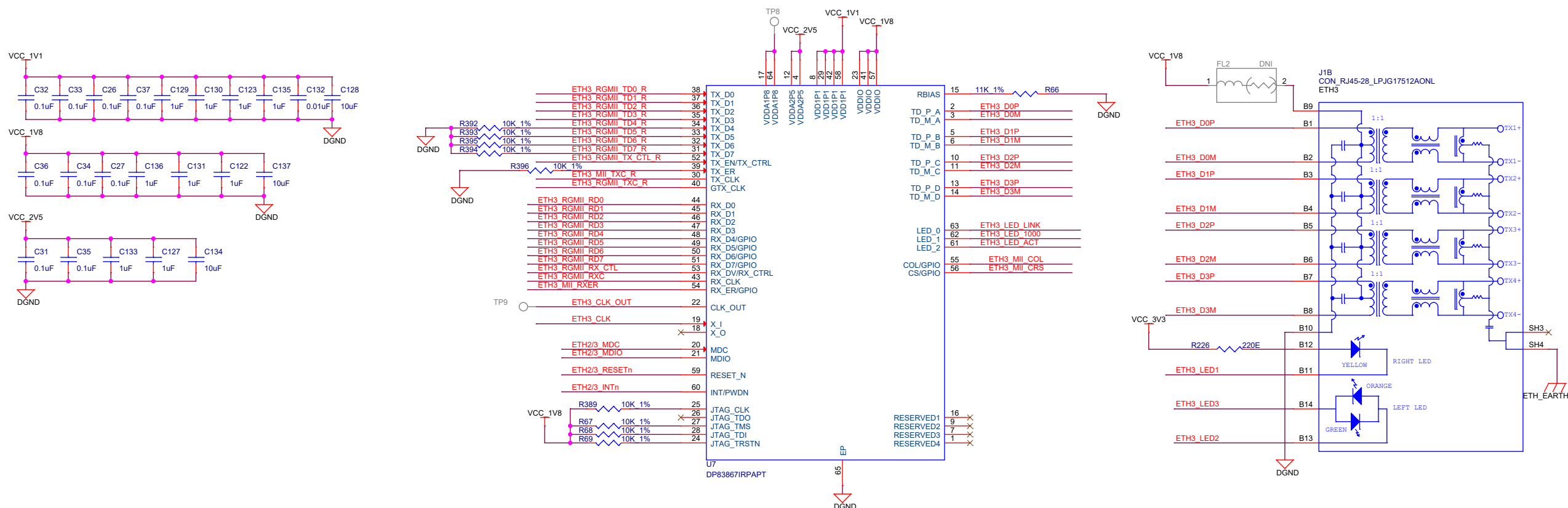
RGMII Mode:
 Mount : R355, R357, R358, R360, R362, R456
 Unmount : R356, R359, R361, R363, R364, R378, R448, R449, R457

MII Mode:
 Mount : R356, R359, R361, R363, R364, R378, R448, R449, R457
 Unmount : R355, R357, R358, R360, R362, R456

- (4) ETH2_MII_RXER << ETH2_MII_RXER
- (4) ETH2_LED_LINK << ETH2_LED_LINK
- (4,9) ETH2/3_INTn << ETH2/3_INTn
- (4) ETH2_CLK << ETH2_CLK
- (4) ETH2_RGMII_TD0 << ETH2_RGMII_TD0
- (4) ETH2_RGMII_TD1 << ETH2_RGMII_TD1
- (4) ETH2_RGMII_TD2 << ETH2_RGMII_TD2
- (4) ETH2_RGMII_TD3 << ETH2_RGMII_TD3
- (4) ETH2_RGMII_TXC << ETH2_RGMII_TXC
- (4) ETH2_RGMII_TX_CTL << ETH2_RGMII_TX_CTL
- (4) ETH2_RGMII_RD0 << ETH2_RGMII_RD0
- (4) ETH2_RGMII_RD1 << ETH2_RGMII_RD1
- (4) ETH2_RGMII_RD2 << ETH2_RGMII_RD2
- (4) ETH2_RGMII_RD3 << ETH2_RGMII_RD3
- (4) ETH2_RGMII_RXC << ETH2_RGMII_RXC
- (4) ETH2_RGMII_RX_CTL << ETH2_RGMII_RX_CTL
- (4,9) ETH2/3_MDC << ETH2/3_MDC
- (4,9) ETH2/3_MDIO << ETH2/3_MDIO
- (4) GPIO_ETH2/3_RESETh << GPIO_ETH2/3_RESETh
- (4,6) PORz_OUT << PORz_OUT
- (9) ETH2/3_RESETh << ETH2/3_RESETh

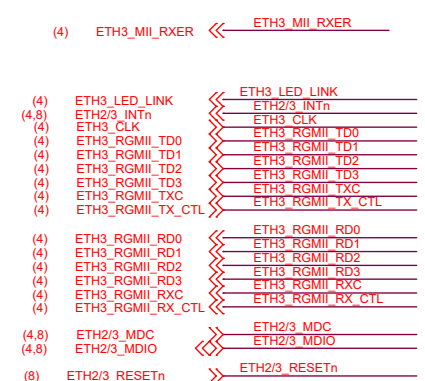
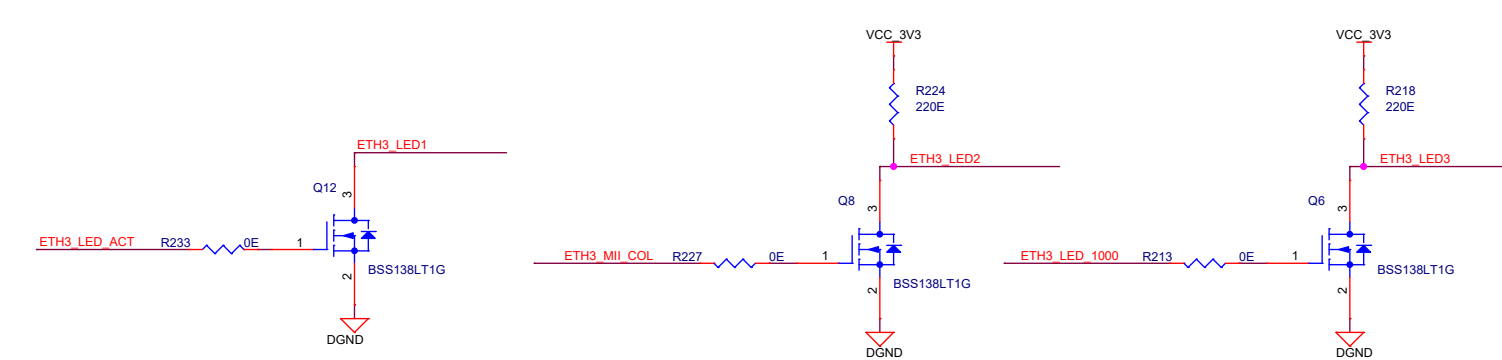
PHY ADD = 00000
 Auto_neg =Enabled
 ANEGsel 10/100/1000

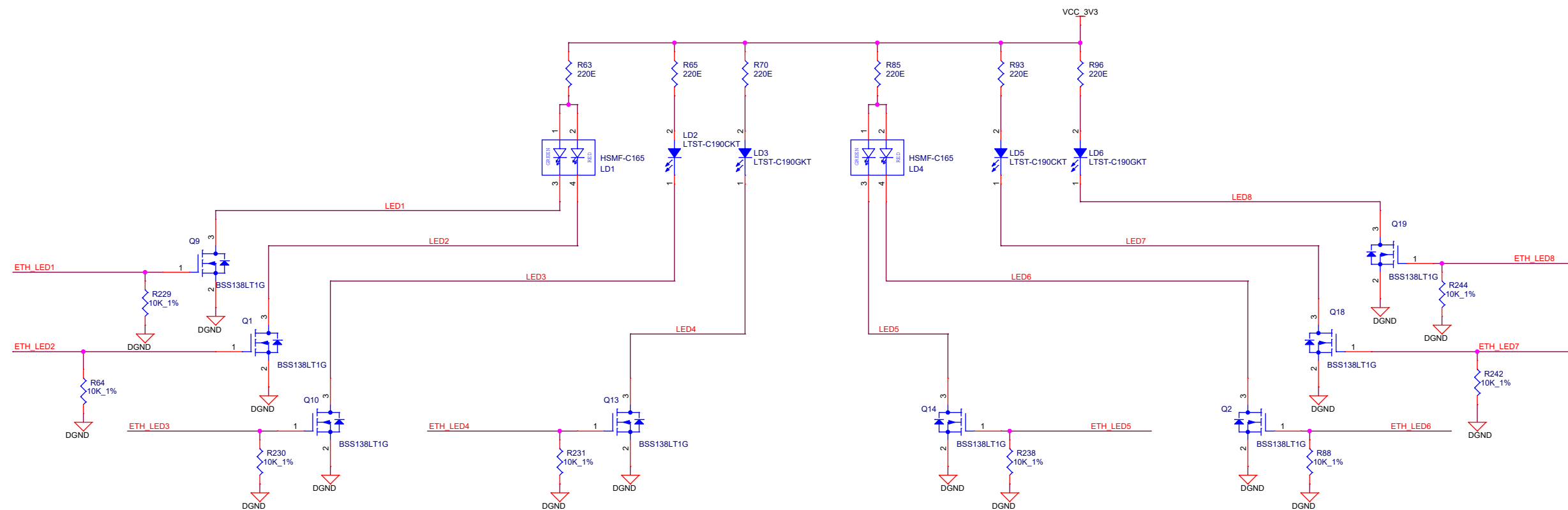




RGMII Mode:
Mount : R397, R398, R401, R402, R404, R458
Unmount : R399, R400, R403, R405, R406, R420, R450, R451, R459

MII Mode:
Mount : R399, R400, R403, R405, R406, R420, R450, R451, R459
Unmount : R397, R398, R401, R402, R404, R458





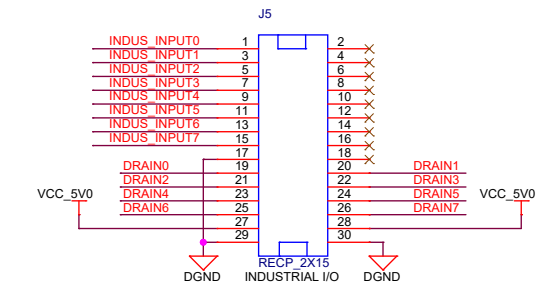
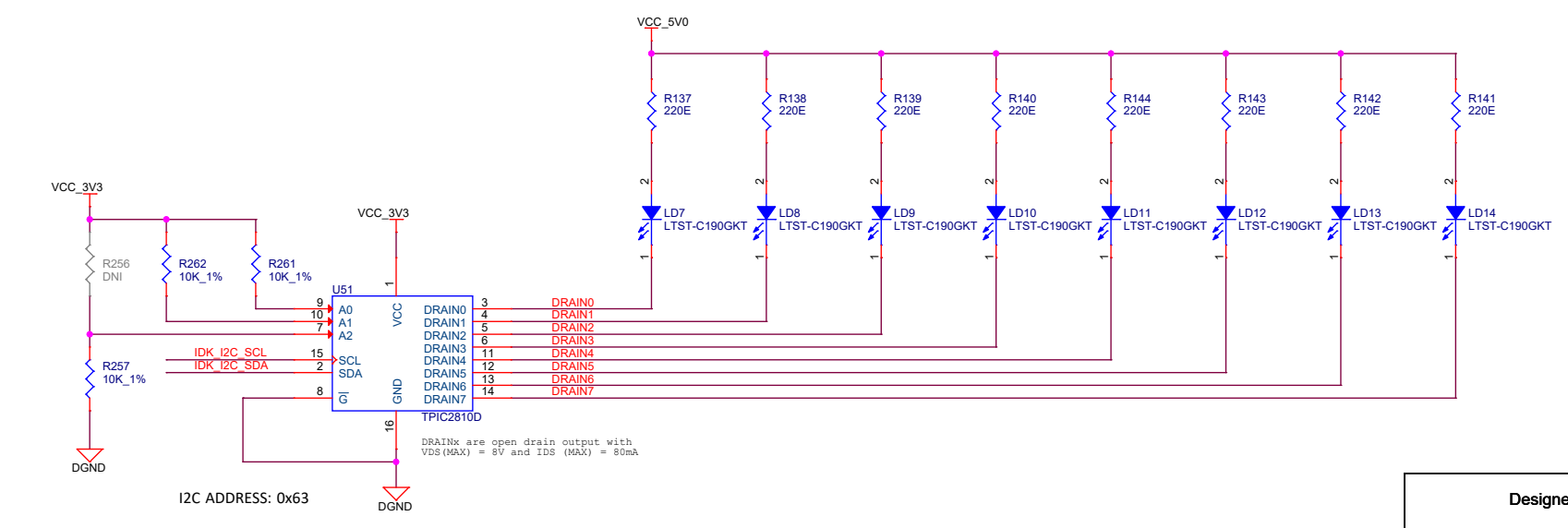
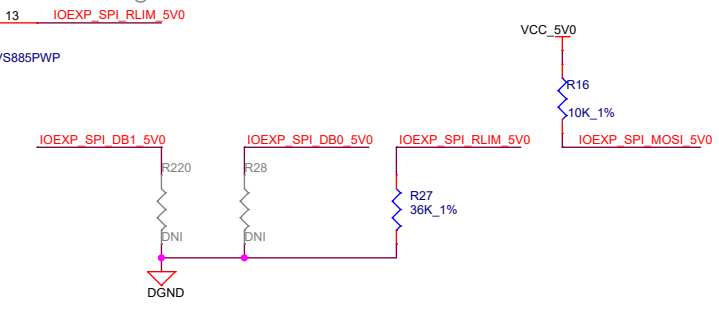
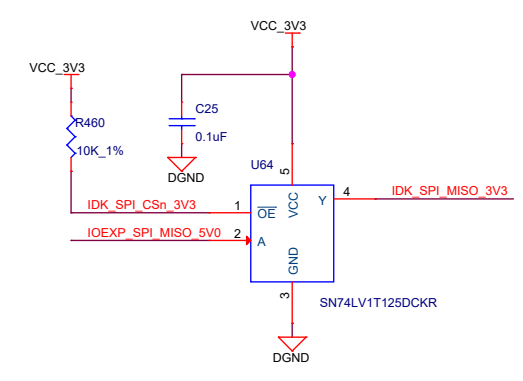
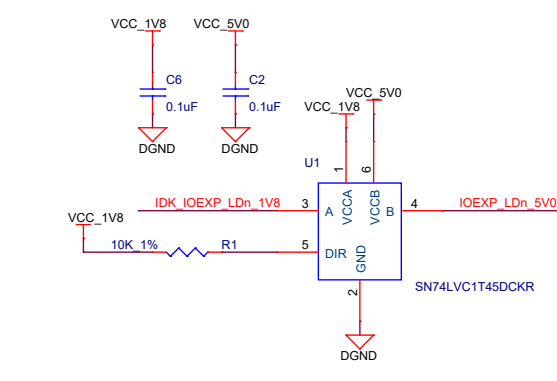
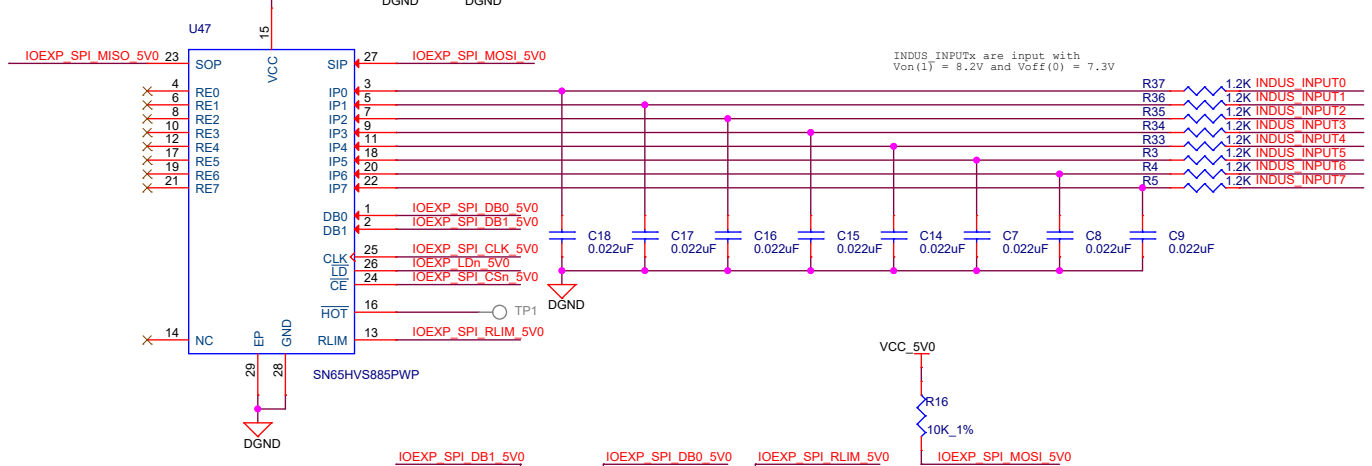
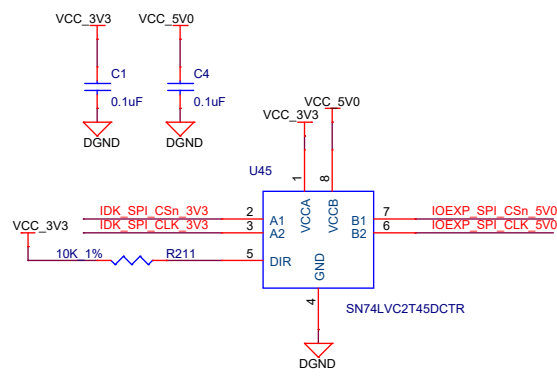
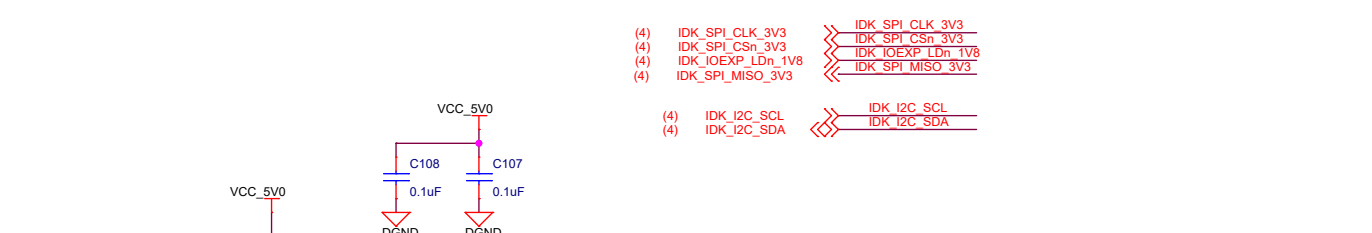
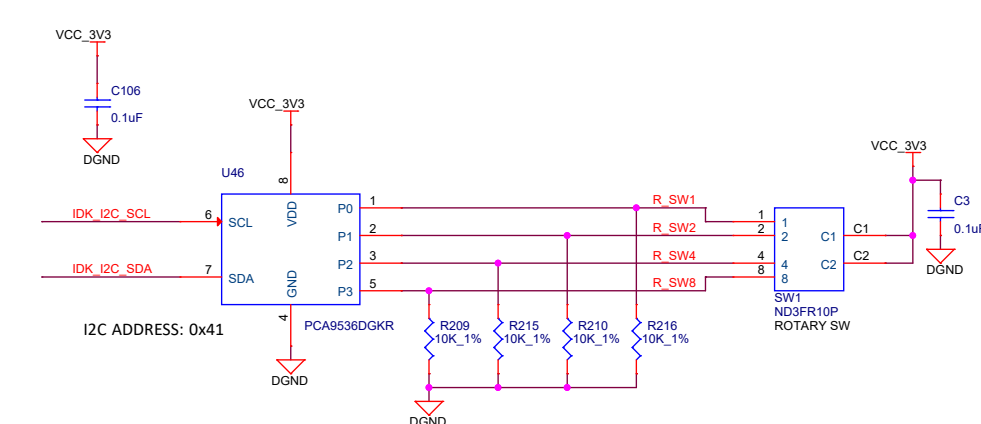
- (4) ETH_LED1
- (4) ETH_LED2
- (4) ETH_LED3
- (4) ETH_LED4
- (4) ETH_LED5
- (4) ETH_LED6
- (4) ETH_LED7
- (4) ETH_LED8

- ETH_LED1
- ETH_LED2
- ETH_LED3
- ETH_LED4
- ETH_LED5
- ETH_LED6
- ETH_LED7
- ETH_LED8

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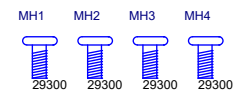


HARDWARE SCHEMATICS

ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.
2. PCB should be baked at 120 degree for 8 hours.
3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
4. These assemblies are ESD sensitive, ESD precautions shall be observed.
5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
6. Provide serial numbers to the assembled boards for identification.
7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

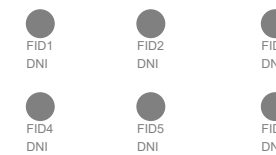
SCREWS



WASHER'S

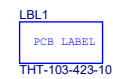


FIDUCIALS



LABEL

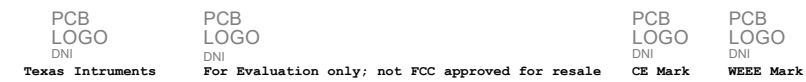
Board Serial No.



BARE PCB



LOGOS



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Title
HARDWARE SCHEMATICS

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