Note: Over-voltage protection is designed to withstand up to +7V.
PERIPHERAL 3V3

Place the whole section near DDR3L.
Place C536 near pin 10, C533, C537 near pin 2

2V8 LDO

2V5 LDO

SD CARD VOLTAGE SELECT

VDD_DDR_VTT Currently not using
Decoupling capacitor should connect close to power and ground.

Stitching Capacitors for SDI signals

Note: Remove R103 if R102 is populated

Keep ESD Diodes near SD connector
NOTE:
This design assumes a normal loading on the VDD_3V3_PERI rail of up to 1A.
The VDD_LDO_1V5 rail is allowed a maximum of 250 mA.
WiFi/BT

TP54, TP55, TP56, TP57 are for debug purpose

VDD_1V8
VDD_3V3
VDD_1V8

BT_REG_ON 8
WL_REG_ON 8
UART6_RXD 8
UART6_TXD 8
UART6_CTS_B 8,12
UART6_RTS_B 8,12

SD2_DATA07
SD2_DATA17
SD2_DATA27
SD2_DATA37

SD2_CMD 7
SD2_CLK 7

WL_IRQ 8
UART6_CTS_B 8,12
UART6_RTS_B 8,12
Note:
- Debug UART1 for Cortex-A7
- Debug UART2 for Cortex-M4

Layout:
- Route 90 ohm differential for USB
- Place R776, R777 close to the micro USB connector

Option: Discharge resistor for debug uart

Keep ESD Diodes near USB connector
Keep ESD Diodes near USB connector
.Layout: Place 1µF, 0.1µF capacitor as close as possible to VDD pins.

The RESET input must be held low for a minimum of 1µs.

Auto neg enable. For disabling RX0[2:0], RX0[6:6/0/0].
RX0[2:0] Auto-negotiation = [0]
PHY_LED[0:2] GPERT CONFIG in MODE4.
TXS0102 have internal pull up of value 10k at A1, A2, B1, B2 pins
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