TIDA-00424 Video Sync Clock Generator
Analog Input and LMH1981 Sync Separator

External HVF+INIT Input Header

Quad SPDT Input MUX with Output Hi-Z

27 MHz Clock Source from VCXO or SMA Input
Power Supply Input and Low-Noise 3.3V LDO Regulator

Layout Note: Unless otherwise noted, label all ICs, Test Points, Jumpers and Headers per the component comment. For jumpers and headers, label pins according to the pin legend noted. All labels should be present on top and bottom silk screen (except for ICs).

Layout Note: Labels should be present on top and bottom silk label pins according to the pin legend noted. All labels should be present on top and bottom silk screen (except for ICs).

Layout Note: Pin Legend is "5V IN" (pin 8) "NC" (pin 7) "LDO 3.3V" (pin 6) "3.3V" (pin 5) "GND" (pins 1-4)

Layout Note: Distribute caps around the 4 sides of LMH1983 for decoupling the VDD power supply plane.

Layout Note: LED Legend is "3.3V"

Layout Note: LED Legend is "5V IN"

Note: Remove 0R resistor when applying an external 3.3V power supply to the V3V input.

Note: LDO output voltage Vout = 1V*(1+R_l/R_lo) = 3.30V

Note: LDO 3V3

Note: Power supply to the 3V3 input.

Applying an external 3.3V power
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