MAJOR REVISION HISTORY:

<table>
<thead>
<tr>
<th>PCB REV.</th>
<th>SCH. REV.</th>
<th>DESCRIPTION</th>
<th>DATE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>0.6</td>
<td>Initial Draft</td>
<td>03-FEB-2012</td>
</tr>
<tr>
<td>1.1</td>
<td></td>
<td>Release for Alpha Boards</td>
<td>20-MAR-2012</td>
</tr>
<tr>
<td>2.0</td>
<td>2.5</td>
<td>Release for Beta Boards</td>
<td>26-JUL-2012</td>
</tr>
<tr>
<td>2.9</td>
<td></td>
<td>Redundant pull-up and termination NU on EMU_TCK</td>
<td>28-NOV-2013</td>
</tr>
</tbody>
</table>

I2C ADDRESS TABLE:

<table>
<thead>
<tr>
<th>REF DES</th>
<th>DESCRIPTION</th>
<th>7 BIT ADDRESS</th>
</tr>
</thead>
<tbody>
<tr>
<td>EEPROM1</td>
<td>DSP EEPROM</td>
<td>0x50, 0x51</td>
</tr>
<tr>
<td>U264</td>
<td>ETHERNET EEPROM</td>
<td>0x50</td>
</tr>
</tbody>
</table>

PCB MECHANICAL DETAILS:

1. PCB SIZE: 7.11" x 2.89" x 0.063"
2. PCB MATERIAL: FR4_IT168G
3. NUMBER OF LAYERS: 12
4. IMPEDANCE CONTROL: YES

NOTES, UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES ARE IN OHMS.
2. CAPACITANCE VALUES ARE IN MICROFARADS.
3. PARTS NOT INSTALLED ARE INDICATED WITH "NU".
4. SIGNAL NET NAMES WITH "#" SUFFIX, ARE ACTIVE LOW SIGNALS.
SCHEMATIC PAGE DESCRIPTION:

01 : COVER PAGE
02 : TABLE OF CONTENTS
03 : SYSTEM BLOCK DIAGRAM
04 : PLACEMENT
05 : POWER CONSUMPTION
06 : POWER SEQUENCE
07 : POWER DISTRIBUTION
08 : CLOCK DIAGRAM
09 : FPGA INTERFACE CONTROL
10 : MANAGEMENT MAP
11 : AMC CONNECTOR
12 : MMC, HYPERLINK COMM
13 : DSP - SERDES PORTS
14 : DSP - DDR3
15 : DDR3 & ECC
16 : DSP - EMIF & JTAG
17 : DSP - MISC
18 : DSP - CLOCK & SMART REFLEX
19 : CLOCK GENERATION
20 : USB - JTAG
21 : GIGABIT ETHERNET
22 : FPGA - POWER, RESET CTRL, McBSP
23 : FPGA - BOOT MODE & SMART REFLEX
24 : DSP - POWER 1
25 : DSP - POWER 2
26 : SMART REFLEX & CORE VOLT
27 : POWER SUPPLY 1
28 : POWER SUPPLY 2
29 : REVISION HISTORY
# Power Consumption

<table>
<thead>
<tr>
<th>Components Part No.</th>
<th>Description</th>
<th>Quantity Per Board</th>
<th>Current Consumed by corresponding device on power supply (mA)</th>
<th>Total Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>0.75V</td>
<td>1.00V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>CVDD</td>
<td>CVDD1</td>
</tr>
<tr>
<td>TMS320C6657</td>
<td>CPU</td>
<td>1</td>
<td>2500.0</td>
<td>1000.0</td>
</tr>
<tr>
<td>XC5206A-FFG256C</td>
<td>FPGA</td>
<td>1</td>
<td>125.0</td>
<td></td>
</tr>
<tr>
<td>MT41JU1024M16HA-12S</td>
<td>DDR3 SDRAM</td>
<td>2</td>
<td>50.0</td>
<td>52.0</td>
</tr>
<tr>
<td>MT41JU1024M16HA-12S</td>
<td>DDR3 ECC</td>
<td>0</td>
<td>50.0</td>
<td>525.0</td>
</tr>
<tr>
<td>NAND128M128SA14E</td>
<td>NAND Flash (64/8MB)</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>AT25128B</td>
<td>SPI EEPROM</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FT2232H</td>
<td>USB to JTAG converter</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>08E1112</td>
<td>Ethernet</td>
<td>1</td>
<td>320.0</td>
<td></td>
</tr>
<tr>
<td>M57436</td>
<td>MMC</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C05520065</td>
<td>Clock Generator</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>XDS60b2</td>
<td>XDS60b2 Mezzanine</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Misc</td>
<td></td>
<td>1</td>
<td>100.0</td>
<td></td>
</tr>
<tr>
<td><strong>Total Current on individual power supply (mA)</strong></td>
<td></td>
<td></td>
<td>100.00</td>
<td>2500.0</td>
</tr>
<tr>
<td>5% margin added over design (mA)</td>
<td></td>
<td></td>
<td>105.00</td>
<td>2625.0</td>
</tr>
<tr>
<td><strong>Power Consumption in (mW)</strong></td>
<td></td>
<td></td>
<td>18.75</td>
<td>2625.0</td>
</tr>
</tbody>
</table>

**Vin**

- 3.3V: TPS73701 – 3.3V Aux to 2.5V regulation 372.65 mA
- 3.3V: TPS73701 – 3.3V Aux to 1.8V Aux regulation 330.75 mA
- 3.3V: TPS73701 – 3.3V Aux to 1.8VCC regulation 148.84 mA
- 3.3V: TPS73701 – 3.3V Aux to 1.2V regulation 490.61 mA
- 1.5V: TPS51200 – 1.5V to 0.5V regulation 110.25 mA

**Voltage Regulator**

- 12V: UCD7242 – 12V to 1V CVDD voltage 243.06 mA
- 12V: UCD7242 – 12V to CVDD1 voltage 97.22 mA
- 12V: TPS54520 – 12V to 1.5V 219.48 mA
- 12V: TPS54520 – 12V to 3.3V AUX 946.70 mA
- 12V: TPS54525 – 12V to 5V 328.13 mA

**Total Current at 12V** 1.83A
**Total Current @ 3.3V AMC** 0.65A
**Total Power Consumption** 22.18W
C6657 Design:

1) CVDD1 should ramp at the same time or shortly following CVDD. Although simultaneous ramping is permitted, CVDD1 must never exceed CVDD until after CVDD has reached a valid voltage.

2) DVD15 supply is ramped up following DVDD18. Although ramping DVDD18 and DVDD15 simultaneously is permitted, DVDD15 must never exceed DVDD18.

3) There is no specific power-up nor power-down sequence defined for FPGA.

4) FPGA is first to come up and it generates ENABLE signal for all power supplies using PGGOOD signals.
Place all SERDES DC-blocking caps on top layer adjacent to the DSP's RX pins so that there are no additional vias.
**DDR3 INTERFACE**

**Notes:**
- Place these resistors at the end of the trace.
- 20 mil trace width

**DDR3 Slew-Rate Settings (DDRSRATE[1:0]):**
- 00 Fastest
- 01 Fast
- 10 Slow
- 11 Slowest
**DDR3 MEMORY INTERFACE**

- Data bits can be swapped within the byte lane to ease routing.
- Address/Command/Control/Clock routing must be fly-by in byte order ECC, 0, 1, 2, 3.

**Supported Memories (96 FBGA) :**

<table>
<thead>
<tr>
<th>Mfg</th>
<th>512MB (256MB x 2)</th>
<th>1024MB (512MB x 2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Micron</td>
<td>MT41J128M16HA-125</td>
<td>MT41J256M16RE-125</td>
</tr>
</tbody>
</table>

**DDR3 ECC INTERFACE**

Supported ECC Chip (96 FBGA) : 

<table>
<thead>
<tr>
<th>Mfg</th>
<th>256MB</th>
<th>512MB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Micron</td>
<td>MT41J128M16HA-125</td>
<td>MT41J256M16RE-125</td>
</tr>
</tbody>
</table>
DSP CLOCK

All blocking capacitors to be placed near DSP to keep connecting routes short and minimize vias.

PCI CLOCK MUX

SMART REFLEX
Switch for JTAG emulation
EXT_EMU_DET = 0 --> External / Mezzanine Emulator
EXT_EMU_DET = 1 --> On board emulation

Switch for JTAG emulation
FT2232HL_RESET# = 0 --> AMC
FT2232HL_RESET# = 1 --> Mini USB
If both fiber (SGMII) and copper (1000BASE-X) cables are connected, the preferred media will be selected based on value of register 16_2.11:10. If it is:
- 00: Link with 1st media to establish link
- 01: Prefer fiber media
- 10: Prefer copper media

For EMI

Activity No Activity Activity No Activity Activity No Activity
Status 0 (Green) BLINK SOLID ON BLINK SOLID ON OFF OFF
Status 1 (Orange) OFF OFF BLINK SOLID ON BLINK SOLID ON

**Pin to Configuration Bit Mapping**

<table>
<thead>
<tr>
<th>PIN</th>
<th>BIT[1]</th>
<th>BIT[0]</th>
<th>VALUE</th>
<th>POL_RST</th>
<th>RESET=0</th>
<th>RESET=1</th>
</tr>
</thead>
<tbody>
<tr>
<td>CONFIG0</td>
<td>PHYADR[1]</td>
<td>PHYADR[0]</td>
<td>VDD0</td>
<td>11</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CONFIG3</td>
<td>SEL_WMI</td>
<td>SEL_VTT</td>
<td>VSS</td>
<td>00</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CONFIG4</td>
<td>EEPROM[1]</td>
<td>EEPROM[0]</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CONFIG5</td>
<td>MODE[1]</td>
<td>MODE[0]</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Pin Value Connection Interpretation**

<table>
<thead>
<tr>
<th>PIN</th>
<th>VALUE</th>
<th>CONNECTION</th>
<th>INTERPRETATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>CONFIG0</td>
<td>00</td>
<td>VSS</td>
<td>PHY Address[1:0] is 00</td>
</tr>
<tr>
<td>CONFIG1</td>
<td>10</td>
<td>STATUS[0]</td>
<td>PHY Address[3:2] is 10</td>
</tr>
<tr>
<td>CONFIG2</td>
<td>01</td>
<td>STATUS[1]</td>
<td>SGMII_CLK not supplied; PHY Address[4] is 1</td>
</tr>
<tr>
<td>CONFIG3</td>
<td>00</td>
<td>VSS</td>
<td>MDC/MDIO mode; S_VTT &amp; F_VTT int supplied</td>
</tr>
<tr>
<td>CONFIG4</td>
<td>01</td>
<td>STATUS[1]</td>
<td>Start reading from address 0</td>
</tr>
<tr>
<td>CONFIG5</td>
<td>10</td>
<td>STATUS[0]</td>
<td>SGMII MAC Int to Auto Media select (Cu/SGMII)</td>
</tr>
</tbody>
</table>
3.3V_AUX to 1.2V Generation

\[ \text{Vout} = \frac{R1+R2}{R2} \times 1.204 \]
\[ = \frac{10k+10k}{10k} \times 1.204 \]
\[ = 1.204\text{V} \]

1.2V @ 0.6A

3.3V_AUX to 1.8V_AUX Generation

\[ \text{Vout} = \frac{R1+R2}{R2} \times 1.804 \]
\[ = \frac{28k+56.2k}{56.2k} \times 1.804 \]
\[ = 1.804\text{V} \]

1.8V_AUX @ 0.31A

3.3V_AUX to 2.5V Generation

\[ \text{Vout} = \frac{R1+R2}{R2} \times 2.50 \]
\[ = \frac{39.2k+36.5k}{36.5k} \times 2.50 \]
\[ = 2.50\text{V} \]

2.5V @ 0.35A

3.3V_AUX to 1.8V Generation

\[ \text{Vout} = \frac{R1+R2}{R2} \times 1.804 \]
\[ = \frac{28k+56.2k}{56.2k} \times 1.804 \]
\[ = 1.804\text{V} \]

1.8V @ 0.14A

3.3V_AUX to 0.75V Generation

\[ \text{Vout} = \frac{R1+R2}{R2} \times 0.75 \]
\[ = \frac{28k+56.2k}{56.2k} \times 0.75 \]
\[ = 0.75\text{V} \]

0.75V @ 0.16A

1.8V Supervisor Circuit

\[ \text{Vth} = 1.67\text{V} \]

20 mil trace width
## TMDSEVM6657 - REVISION HISTORY

<table>
<thead>
<tr>
<th>PCB REV</th>
<th>SCH. REV</th>
<th>CHANGE DESCRIPTION</th>
<th>DATE</th>
<th>AUTHOR</th>
</tr>
</thead>
</table>
| 1.0     | 0.6      | - CLK3 removed  
- Series Termination removed from GPIO0 to GPIO13 lines                                                                                         | 3-FEB-2012 | eInfochips |
| 1.1     | 0.6      | - D9 and D10 part changed with one with higher current capacity.  
- R134 changed to 1K from 4.7K.  
- NU resistors R433 and R434 changed to 10K and 1.2K resp. They are to be mounted.  
- R12 and R17 replaced by 100nF caps C1225 and C1226.  
- R70 and R71 mounting status changed from NU to populated.  
- U6 (DDR3 ECC chip) made NU.  
- DDR3 Clock frequency from Clock Gen changed to 50 MHz (software change only). | 20-MAR-2012 | eInfochips |
| 2.0     | 0.1      | - Clock buffer U1132 removed. 2 OR gates (U268, U269) and the corresponding circuitry to buffer EMU_TCK added.  
- 4 Test Points for Gnd added.  
- ETH_SCK net renamed to ETH_SDA.  
- SIGDET unconnected with LOS; its directly pulled high. R145 and R146 removed  
- SYS_PG_D1 LED changed to Yellow colour from Green. | 02-APR-2012 | eInfochips |
|         | 0.2      | - 10 nF capacitors (C457 and C460) added on VCC12 input rail of U34.  
- Capacitors on CVDD rail optimized from two 220uF, two 100uF and four 47uF to two 100uF and two 47uF.  
- Capacitors on VCC10 rail optimized from one 220uF, three 47uF and one 10uF to two 47uF and one 10uF.  
- An additional 22uF cap (C549) added on VCC12 input for U29. C426 changed from 10nF to 100nF.  
- R183 changed to 1K from 4.7K.  
- SIGDET connected to VCC2V5 using R146.  
- R1273 changed to 4.7K from 10K. | 02-MAY-2012 | eInfochips |
|         | 0.3      | - L15 and L16 changed to 2.3uH and 1.2uH respectively  
- R251 and R373 changed to 22.1K.  
- C549 moved before B158 on 12V plane  
- C2325 changed from 100nF to 10uF.  
- R2203 made NU and R1226 to be mounted. | 07-MAY-2012 | eInfochips |
|         | 0.4      | - NOR Flash density label corrected to 32 Mb from 16MB.                                                                                              | 20-JUL-2012 | eInfochips |
|         | 0.5      | - DISCLAIMER Changed                                                                                                                                 | 26-JUL-2012 | eInfochips |
|         | 0.6      | - Asthetical Change  
Name swap between LVDS and HCSL on page 18                                                                                                         | 06-DEC-2012 | eInfochips |
|         | 0.7      | - Asthetical Change  
Note for DDR3 Slew-Rate setting corrected on page 14                                                                                           | 29-JAN-2013 | eInfochips |
|         | 0.8      | - RB2 and RB3 changed to 10K  
- R85 and R957 made NU                                                                                                                              | 22-FEB-2013 | eInfochips |
|         | 0.9      | - The Resistors R896, R67 and capacitor C555 are redundant components on EMU_TCK and can be NU from design.  
- Pull-up resistor R1119 on EMU_TCK change from 10K to 4.7K.                                                                                     | 28-NOV-2013 | eInfochips |
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