### TI TMS320C6678 EVM Board

**Rev. 3A**

**DSPM-8301E**

**PCB PN:** 19C2830103  
**PCB Rev. A104-1**  
**Project Code:**

PCB Thickness: 62 mils (1.6mm)  
12 Layers

---

<table>
<thead>
<tr>
<th>Layer</th>
<th>Width (mil)</th>
<th>Core</th>
<th>Coating</th>
</tr>
</thead>
<tbody>
<tr>
<td>L10</td>
<td>4.8</td>
<td>0.8</td>
<td>core</td>
</tr>
<tr>
<td>L9</td>
<td>4.8</td>
<td>0.8</td>
<td>core</td>
</tr>
<tr>
<td>L8</td>
<td>4.8</td>
<td>0.8</td>
<td>core</td>
</tr>
<tr>
<td>L7</td>
<td>4.8</td>
<td>0.8</td>
<td>core</td>
</tr>
<tr>
<td>L6_GND</td>
<td>4.8</td>
<td>0.8</td>
<td>core</td>
</tr>
<tr>
<td>L5</td>
<td>4.5</td>
<td>0.8</td>
<td>core</td>
</tr>
<tr>
<td>L4_PWR</td>
<td>4.2</td>
<td>0.8</td>
<td>core</td>
</tr>
<tr>
<td>L3</td>
<td>4.2</td>
<td>0.5</td>
<td>core</td>
</tr>
<tr>
<td>L2_GND</td>
<td>4.0</td>
<td>0.5</td>
<td>core</td>
</tr>
<tr>
<td>L1</td>
<td>4.0</td>
<td>0.5</td>
<td>core</td>
</tr>
</tbody>
</table>

---

**DISCLAIMER:** This circuit design is provided as reference only, without warranty expressed or implied. The user is encouraged to perform all due diligence with respect to design and analysis.

---

Copyright (C) 2010 Texas Instruments Incorporated. All rights reserved. This document is proprietary to TI and is intended solely for use by TI and its customers. This document is not to be reproduced, distributed, or disclosed to other parties in its entirety or in part without the express written consent of TI.
# TITLE & TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>Page</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>COVER PAGE</td>
</tr>
<tr>
<td>02</td>
<td>TITLE &amp; TABLE OF CONTENTS</td>
</tr>
<tr>
<td>03</td>
<td>BLOCK DIAGRAM_AMC</td>
</tr>
<tr>
<td>04</td>
<td>POWER SEQUENCE</td>
</tr>
<tr>
<td>05</td>
<td>POWER CONSUMPTION</td>
</tr>
<tr>
<td>06</td>
<td>POWER DISTRIBUTION</td>
</tr>
<tr>
<td>07</td>
<td>CLOCK DIAGRAM</td>
</tr>
<tr>
<td>08</td>
<td>FPGA_BLOCK</td>
</tr>
<tr>
<td>09</td>
<td>BUS Management Map</td>
</tr>
<tr>
<td>10</td>
<td>AMC GF</td>
</tr>
<tr>
<td>11</td>
<td>MMC</td>
</tr>
<tr>
<td>12</td>
<td>DSP_SERDES_PORTS</td>
</tr>
<tr>
<td>13</td>
<td>DSP_DDR3</td>
</tr>
<tr>
<td>14</td>
<td>DSP_EMIF</td>
</tr>
<tr>
<td>15</td>
<td>DSP_JTAG_EMU_TSIP</td>
</tr>
<tr>
<td>16</td>
<td>DSP_MISC</td>
</tr>
<tr>
<td>17</td>
<td>DSP_CLOCK_Smart Reflex</td>
</tr>
<tr>
<td>18</td>
<td>DSP_POWERA</td>
</tr>
<tr>
<td>19</td>
<td>DSP_POWERB</td>
</tr>
<tr>
<td>20</td>
<td>DSP_POWERC</td>
</tr>
<tr>
<td>21</td>
<td>DSP_GND</td>
</tr>
<tr>
<td>22</td>
<td>CLOCK_GEN3</td>
</tr>
<tr>
<td>23</td>
<td>CLOCK_GEN2</td>
</tr>
<tr>
<td>24</td>
<td>DDR3</td>
</tr>
<tr>
<td>25</td>
<td>DDR3_ECC</td>
</tr>
<tr>
<td>26</td>
<td>USB-JTAG</td>
</tr>
<tr>
<td>27</td>
<td>Gigabit Ethernet PHy</td>
</tr>
<tr>
<td>28</td>
<td>RJ45/MISC</td>
</tr>
<tr>
<td>29</td>
<td>Connectors for HyperLink &amp; Debug</td>
</tr>
<tr>
<td>30</td>
<td>FPGA_XC3S200AN_A</td>
</tr>
<tr>
<td>31</td>
<td>FPGA_XC3S200AN_B</td>
</tr>
<tr>
<td>32</td>
<td>FPGA_XC3S200AN_C</td>
</tr>
<tr>
<td>33</td>
<td>Power ucd9222</td>
</tr>
<tr>
<td>34</td>
<td>Power_1.2V/1.8V/2.5V/0.75V</td>
</tr>
<tr>
<td>35</td>
<td>Power_VCC5 / VCC3V3_AUX</td>
</tr>
<tr>
<td>36</td>
<td>Power VCC1V5</td>
</tr>
<tr>
<td>37</td>
<td>History_0</td>
</tr>
<tr>
<td>38</td>
<td></td>
</tr>
<tr>
<td>39</td>
<td></td>
</tr>
</tbody>
</table>
### Power Sequence

#### Power Sequence Diagram

- **S0**: MMC
- **S1**: VCC1V8
- **S2**: Other
- **S3**: XCS5200AN
- **S4**: 88E1111
- **S5**: XCS5200AN
- **S6**: DSP TMS320C6678
- **S7**: UCD9222_ENA2
- **S8**: XCS5200AN
- **S9**: VCC1V8
- **S10**: VCC12
- **S11**: VCC1V8
- **S12**: VCC2V5
- **S13**: VCC1V0
- **S14**: DDR3 SDRAM
- **S15**: XCS5200AN
- **S16**: 88E1111
- **S17**: VCC3V3_AUX
- **S18**: XDS560V2 Madzenine Board

#### Reset Sequence

- **S19**: reset sequence

#### CLK Sequence

- **S20**: clock sequence

#### There is no specific power-up nor power-down sequence.

---

**Notes:**

- When power on VDD
- When power down

---

**Legend:**

- **88E1111 (PHY):**
- **2.5V:**
- **1.2V:**
- **1.5V:**
- **0.75V:**
- **1.0V Fixed:**
- **1.0V scaled:**
- **1.5V:**
- **3.3V / 1.8V / 1.2V:**

---

**Diagram Details:**

- Various power states and voltages indicated for different components.
- Connections and signals for power-on and power-down sequences.
- Specific timing notes for certain events.

---

**Additional Information:**

- Designed for TI by ADVANCED DSPM-8301E
- Document Number: A104-1
- Date: Wednesday, March 07, 2012
# POWER CONSUMPTION

<table>
<thead>
<tr>
<th>VCCD (12V→1.0V)</th>
<th>V</th>
<th>I</th>
<th>Efficiency</th>
<th>Pd (W) 12V</th>
<th>Pd (W) 3.3V</th>
<th>Utilization</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1.00</td>
<td>8.000</td>
<td>90%</td>
<td>8.889</td>
<td>0.741</td>
<td>x</td>
<td>70%</td>
</tr>
<tr>
<td></td>
<td>1.00</td>
<td>5.000</td>
<td>90%</td>
<td>5.556</td>
<td>0.463</td>
<td>x</td>
<td>70%</td>
</tr>
<tr>
<td></td>
<td>1.50</td>
<td>0.850</td>
<td>90%</td>
<td>1.417</td>
<td>0.118</td>
<td>x</td>
<td>70%</td>
</tr>
<tr>
<td></td>
<td>1.50</td>
<td>0.240</td>
<td>90%</td>
<td>2.000</td>
<td>0.167</td>
<td>x</td>
<td>100%</td>
</tr>
<tr>
<td></td>
<td>0.75</td>
<td>0.050</td>
<td>45%</td>
<td>0.417</td>
<td>0.015</td>
<td>x</td>
<td>70%</td>
</tr>
<tr>
<td></td>
<td>3.30</td>
<td>0.024</td>
<td>85%</td>
<td>0.093</td>
<td>0.008</td>
<td>x</td>
<td>70%</td>
</tr>
<tr>
<td></td>
<td>3.30</td>
<td>0.300</td>
<td>85%</td>
<td>1.265</td>
<td>0.097</td>
<td>x</td>
<td>70%</td>
</tr>
<tr>
<td></td>
<td>3.30</td>
<td>0.210</td>
<td>85%</td>
<td>0.815</td>
<td>0.068</td>
<td>x</td>
<td>70%</td>
</tr>
<tr>
<td></td>
<td>3.30</td>
<td>0.060</td>
<td>85%</td>
<td>2.562</td>
<td>0.214</td>
<td>x</td>
<td>70%</td>
</tr>
<tr>
<td></td>
<td>1.80</td>
<td>0.200</td>
<td>40%</td>
<td>0.783</td>
<td>0.055</td>
<td>x</td>
<td>70%</td>
</tr>
<tr>
<td></td>
<td>1.80</td>
<td>0.500</td>
<td>40%</td>
<td>0.591</td>
<td>0.035</td>
<td>x</td>
<td>70%</td>
</tr>
<tr>
<td></td>
<td>1.80</td>
<td>0.075</td>
<td>46%</td>
<td>0.293</td>
<td>0.024</td>
<td>x</td>
<td>70%</td>
</tr>
<tr>
<td></td>
<td>1.20</td>
<td>0.125</td>
<td>30%</td>
<td>0.500</td>
<td>0.042</td>
<td>x</td>
<td>70%</td>
</tr>
<tr>
<td></td>
<td>1.00</td>
<td>0.250</td>
<td>90%</td>
<td>0.278</td>
<td>0.015</td>
<td>x</td>
<td>70%</td>
</tr>
<tr>
<td></td>
<td>2.50</td>
<td>0.210</td>
<td>65%</td>
<td>0.808</td>
<td>0.067</td>
<td>x</td>
<td>70%</td>
</tr>
<tr>
<td></td>
<td>1.000</td>
<td>0.490</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>5.00</td>
<td>1.000</td>
<td>85%</td>
<td>5.882</td>
<td>0.490</td>
<td>x</td>
<td>70%</td>
</tr>
<tr>
<td></td>
<td>3.30</td>
<td>0.048</td>
<td>100%</td>
<td>0.358</td>
<td>0.048</td>
<td>x</td>
<td>70%</td>
</tr>
<tr>
<td><strong>Total power consumption</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VDD</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCCD</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCC1V8</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCC1V8_AUX</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCC1V8_AUX (1.5V_AUX-&gt;1.8V_AUX)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCC1V8_AUX (1.8V_AUX-&gt;1.8V_AUX)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCC1V8_AUX (1.8V_AUX-&gt;1.2V_AUX)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCC1V8_AUX (1.2V_AUX-&gt;1.8V_AUX)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCC1V8_AUX (1.8V_AUX-&gt;1.2V_AUX)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCC1V8_AUX (1.2V_AUX-&gt;1.8V_AUX)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCC1V8_AUX (1.8V_AUX-&gt;1.2V_AUX)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCC1V8_AUX (1.2V_AUX-&gt;1.8V_AUX)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCC1V8_AUX (1.8V_AUX-&gt;1.2V_AUX)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCC1V8_AUX (1.2V_AUX-&gt;1.8V_AUX)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCC1V8_AUX (1.8V_AUX-&gt;1.2V_AUX)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCC1V8_AUX (1.2V_AUX-&gt;1.8V_AUX)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCC1V8_AUX (1.8V_AUX-&gt;1.2V_AUX)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCC1V8_AUX (1.2V_AUX-&gt;1.8V_AUX)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCC1V8_AUX (1.8V_AUX-&gt;1.2V_AUX)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCC1V8_AUX (1.2V_AUX-&gt;1.8V_AUX)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCC1V8_AUX (1.8V_AUX-&gt;1.2V_AUX)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCC1V8_AUX (1.2V_AUX-&gt;1.8V_AUX)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCC1V8_AUX (1.8V_AUX-&gt;1.2V_AUX)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCC1V8_AUX (1.2V_AUX-&gt;1.8V_AUX)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCC1V8_AUX (1.8V_AUX-&gt;1.2V_AUX)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCC1V8_AUX (1.2V_AUX-&gt;1.8V_AUX)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCC1V8_AUX (1.8V_AUX-&gt;1.2V_AUX)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCC1V8_AUX (1.2V_AUX-&gt;1.8V_AUX)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCC1V8_AUX (1.8V_AUX-&gt;1.2V_AUX)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCC1V8_AUX (1.2V_AUX-&gt;1.8V_AUX)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCC1V8_AUX (1.8V_AUX-&gt;1.2V_AUX)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCC1V8_AUX (1.2V_AUX-&gt;1.8V_AUX)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCC1V8_AUX (1.8V_AUX-&gt;1.2V_AUX)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCC1V8_AUX (1.2V_AUX-&gt;1.8V_AUX)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCC1V8_AUX (1.8V_AUX-&gt;1.2V_AUX)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCC1V8_AUX (1.2V_AUX-&gt;1.8V_AUX)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCC1V8_AUX (1.8V_AUX-&gt;1.2V_AUX)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>VCC1V8_AUX (1.2V_AUX-&gt;1.8V_AUX)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Front panel and ESD Strip

OVP: $\sim 12.7V + 0.6V = \sim 13.3V$
The NU resistors on these connections to the MSP430 are for debug use only and will be used only with the shunts removed from pins 1 and 2 of CN7.
Caution!

"Place ALL SERDES DC-blocking caps on top layer adjacent to the DSP's RX pins so that there are no additional vias"

"The HyperLink routes must have a maximum of 2 vias and no via stubs – top layer routing recommended"
"All DC-blocking capacitors to be placed near DSP to keep connecting routes short and minimize vias"
1.0V & 1.5V for Serdes
Those caps should be located near the CDCE62005 (CLK2).

C310 0.1μF
C311 0.1μF
C312 0.1μF
C313 0.1μF
C314 0.1μF
C315 0.1μF
C316 0.1μF
C317 0.1μF
C318 0.1μF
C319 0.1μF
C320 1μF
C321 0.1μF
C322 1μF
C323 0.1μF
C324 1μF
Trace need 20 mil.

* Data bits can be swapped within the byte lane to ease routing.

* Address/Command/Control/Clock routing must be Fly-By in byte order 0, 1, 2, 3 ECC, 4, 5, 6, 7.
Switch for JTAG emulation
FT2232HL_RESET# = 0 → AMC
FT2232HL_RESET# = 1 → Mini USB

Switch for JTAG emulation
EXT_EMU_DET = 0 → External / Mezzanine Emulator
EXT_EMU_DET = 1 → On board emulation
Heatsink Holes

AMC Hole

On board
IPASS+HD for HyperLink Bus connection

Pin Header for debug

the interfaces on the 80-pin header are all 1.8V LVCMOS except for the UART which is 3.3V LVCMOS
During Configuration: Must be High to allow configuration to start.

a. Remove the boundary scan chain from UCD9222.
b. Remove bus switch and loop in the FPGA and PHY.
CVDD / VCC1V0

Place the caps close to UCD9222 on the top side.

PMBus Address

UCD9222_PG1
R418 10K
UCD9222_PG2

R566 2
C372 4.7uF 6.3V
U32 TI_UCD9222RGZR

V33DIO
BPCAP
FLT2A

9222_TMS
R251 4.99K
A103-1

9222_TRST#
R252 1.5K
A103-1

R246 NL/2K
C608 0.01uF
16V

C609 0.01uF
16V

R247 NL/0
C445 0.1uF
50V

R254 100K
C467 560pF

VCC3V3_AUX

R440 10K
R411 10

R437

R438 10K
R259 10K
R256 2K
R255 2K

PMBUS_CLK
PMBUS_DAT
PMBUS_ALT
PMBUS_CTL

1.0V@ 5A

+++output capacitor Calculation for VCC1V0+++ 

\[ \frac{V_{PFF}}{C} = \frac{8 \times C}{f_b} \]

(VPPQ=10mV)

C = 3 / (10m * 8 * 750k)

C = 83.3uF

DSP Vcore @8A

+++output capacitor Calculation for VCC1V0+++ 

\[ \frac{V_{PFF}}{C} = \frac{8 \times C}{f_b} \]

(VPPQ=10mV)

C = 8 / (10m * 8 * 750k)

C = 133.3uF

+++Inductor Calculation for VCC1V0+++ 

\[ L = \frac{V_{IN} - V_{OUT}}{f_b} \times \frac{D}{\Delta I} \]

L = (12 - 1) / (8) / 750K
L = 0.243 uH

+++Inductor Calculation for CVD+++ 

\[ L = \frac{V_{IN} - V_{OUT}}{f_b} \times \frac{D}{\Delta I} \]

L = (12 - 1) / (8) / 750K
L = 0.152 uH

Temperature Coefficient: 10 mV/℃

Each 22uF Cin cap needs to tightly coupled to Vin and PGND of the UCD7242.

Corresponding "EA" Pins MUST be routed as differential signals and connected next to DSP for specific rails

Series resistors on EA nets to be placed at the load for proper voltage feedback.
1.2V @0.38A

\[ \text{Vout} = \frac{(R1+R2)}{R2} \times 1.204 \]

1.204V = (0+10k)/10k*1.204

1.8V_AUX @0.3A

\[ \text{Vout} = \frac{(R1+R2)}{R2} \times 1.204 \]

1.204V = (0+10k)/10k*1.204

2.5V @0.21A

\[ \text{Vout} = \frac{(R1+R2)}{R2} \times 1.204 \]

2.50V = (39.2k+36.5k)/36.5k*1.204

1.8V_AUX @0.5A

\[ \text{Vout} = \frac{(R1+R2)}{R2} \times 1.204 \]

1.805V = (28k+56.2k)/56.2k*1.205
### VCC3V3_AUX

Assume 90% Pe,

\[ \text{In} = (3.3V \times 1.8A) \div 90\% \div 12V = 78mA \]

12V@0.79A

\[ R_t = 4800 \Omega \times (\text{In} \div 0.95) \div 2 \]

\[ R_t = 56.2 \Omega \]

\[ \text{Vout} = 0.8 \times \text{V} \times (R1 \div R2 + 1) \]

\[ \text{R1 R2} \]

### 3.3_AUX @2.585A

**Reference Capacitor=100uF**

**Reference Inductor 3.3uH**

![Circuit Diagram](image)

\[ (\text{KIND}=0.3) \]

\[ L = ([\text{Vin (max)} - \text{Vout}] \div \text{Vout} \times \text{Kind}) \times ([\text{Vout} \div \text{Vin (max)}] \times \text{Fsw}) \]

\[ L = ([12 - 5] \div 5 \times 0.3) \times ([3.3] \div [12 \times 840K]) \]

\[ L = 0.3 \mu\text{H} \]

\[ \text{Cout} > \left( \frac{2 \times \Delta I_{\text{out}}}{\text{Fsw} \times \Delta V_{\text{out}}} \right) \]

\[ \text{Cout} > 87 \mu\text{F} \]

Reference Capacitor=100uF

![Circuit Diagram](image)

### VCC5

Assume 80% Pe,

\[ \text{In} = (5V \times 1A) \div 80\% \div 12V = 520mA \]

12V@0.52A

\[ \text{Vout} = 0.8 \times \text{V} \times (R1 \div R2 + 1) \]

\[ 5V @ 1A \]

5V@1A

\[ \text{Cout} > \left( \frac{2 \times \Delta I_{\text{out}}}{\text{Fsw} \times \Delta V_{\text{out}}} \right) \]

\[ \text{Cout} > \left( \frac{2 \times 3}{840kHz \times 0.0825} \right) \]

\[ \text{Cout} > 87 \mu\text{F} \]

Reference Capacitor=100uF

![Circuit Diagram](image)

\[ (\text{KIND}=0.3) \]

\[ L = \left( \frac{[\text{Vin (max)} - \text{Vout}] \div \text{Vout} \times \text{Kind}}{\text{Vin (max)} \div \text{Fsw}} \right) \]

\[ L = \left( \frac{[7.6]}{0.3} \right) \times \left( 5 \div [7239K] \right) \]

\[ L = 17.5 \mu\text{H} \]

Reference Capacitor=100uF

![Circuit Diagram](image)
VCC1V5

12V@0.3A

1.5V @2.12A

Assume 90% Pe,
In = (1.5V * 2.12A) / 90% / 12V = 295mA

Vout=0.8 V*(R1/R2+1)
1.52=0.8 V*(9.09k/10k+1)

(Over all tolerance is 5%, DC tolerance is 2.5%)

++output capacitor Calculation+++          ++inductor Calculation++

Cout=(2*delta(Iout))/(Fsw*delta(Vout))    L = (Vin - Vout)/(Iout * Kind) * Vout/(Vin * Fsw)

Cout=(2*2.5A)/(840kHz*0.0375)             L = (12 - 1.5)(2.5A * 0.3) * 1.5 / (12 * 840kHz)

Cout=~159uF                                L =~2.08uH

Reference Capacitor=200uF
Reference Inductor 3.3uH
History

DSPM-8301 A101-1 / 19C2830100
Jan.24.2011:

1. BOM change list: (ECOP-078102)
   a. MMC enable pin: remove R11, populate R16.
   b. DDR3 slew rate setting: remove R72, populate R70.
   c. VCC5_AUX enabled by FPGA: remove R237.
   d. Change I2C serial EEPROM for the 50h & 51h of address.
      d.1 Change I2C EEPROM to STMicro_M24M01-HRMN6TP.
      d.2. remove R164.
   e. Change COM1 pin header to the connector with lock.

2. Schematics change list:
   a. Update Block, Sequences, Clock diagrams.
   b. Correct the McMRX sideband pins to output and the McMTX sidebands to input.
   c. Change the note 'NL/' on R235 (RSVD09), populating R234 (RSVD08).

3. FPGA code change list:
   a.1 De-assert PORz first and de-assert RESETFULLz after for DSP reset sequence.
   b. Change DSP clockings: CORECLK = PASSCLK = 100MHz, PCIECLK = 100MHz
   b. Boot mode change to I2C EEPROM and none-boot mode.
   d. All reset behaviours on the board are defined.

DSPM-8301 A102-1 / 19C2830101

1. Add the JTAG connection on AMC edge connector .
2. Remove the SW2, R9, C10, R12, R17 for LEDs re-placement.
3. Change I2C EEPROM (128kB) to M24M01-HRMN6TP and its footprint.
4. Change COM_SEL1 to DIP type and COM1 with lock.
5. Add a clock MUX to select the DSP PCIECLK source from the AMC FCLK or CDCE62005.
6. Change DDR3 1333 to 1600 by the Micron 1G X16.
7. Modify the boundary scan loop and remove the JTAG connections from the UCD9222 portion.
8. Change the PMBUS1 to 5pin/2.54mm connector
9. UCD9222 changes:
   a. Add a 10k pull-up resistor on the PMBUS_CTL and DNI it.
   b. Add a 10k pull-down resistor on the JTAG_T5RT.
   c. Remove the JTAG pins on the UCD9222 from the boundary scan chain.
   d. Add a 10k pull-down resistor on the UCD9222_RST# and DNI it.
   e. Separate analog GND to digital GND.
10. Add test points on all power rails.
11. Remove R443 on the PCIECLK to the DSP, put all terminations next by PCIECLK MUX.
12. Install R440 on 9222_TCK, install R439 on PMBUS_CTL, might have a new firmware loading into the UCD9222 for the Beta2 and production units.
13. Pull down the 85C_JTAG_RST# for normal operation of phy.
15. Add pull up resistor (R908, R909) to the inputs to the switch so that these signals are held high when the AMC JTAG interface is selected.

16. Add 22-ohm series termination resistors at the outputs MCMTXPMCLK and MCMRXFCLK which are HyperLink sideband signal clock outputs.
17. Add a temperature monitor to the unused TEMP2 input to the UCD9222
18. Add 4.7K pull-down resistors on the GPIO[15:1] pins and a 4.7K pull-up resistor on GPIO[0] so that these pins are not floating after FPGA release.
19. Replace the 14-pin JTAG with the Spy-Bi-Wire interface .
20. Add 0 Ohm resistors on all power enable signals.
21. ADD R485 for DSP UARTTXD termination
22. DSP_PCIECLK was set from IN2.
23. Change R425 and R426 package from 0603 to 0402.
24. Change R58 package from 0603 to 0402.
25. To modify the title from C6678 to CLOCK GEN3
26. Change net name from Isenes-2A to Isenes-2A
27. U4, U5, U6, U16 U8 change to SAMSUNG_K4B1G1646G
28. NL/U8
29. NL/R431, NL/R432, R435

DSPM-8301 A103-1 / 19C2830102

1. Page26: Change mini-USB to through-hole type
2. Page13: Change the registers value to 2k ohms and the pull-up voltage to IO 1.8V on the DDR3 slew rate pins
3. Page22,23: Add the test points on unused clock inputs and outputs of CDCE62005s
4. Page10: Enable the expansion I2C by default, populate the registers of R160 and R161 for I2C connections between C6678 and AMC finger
5. Page23: Modify the CLK2 (CDCE62005) inputs for the common HyperLink timing, TCLKB will be the PRI_REF input and branch another one to the FPGA by two pairs. The 100MHz input from CLK3 CDCE62005 will be changed to its SEC_REF input.
6. AGND change to GND
7. Leave R160 and R161 as NL and add 2 more resistors on these nets connecting to AMC connector pins 159 and 160. Install 0 ohms in these new resistors

DSPM-8301 A104-1 / 19C2830103

1. Remove R484 and R487 and cross-wire these signals to make the connections functionally match the C6670 EVMs
2. Change R433 to 10k, change R434 to 1.2k, change R12 and R17 from 0 ohm to 0.1uF

12. Install R440 on 9222_TCK, install R439 on PMBUS_CTL, might have a new firmware loading into the UCD9222 for the Beta2 and production units.
13. Pull down the 85C_JTAG_RST# for normal operation of phy.
15. Add pull up resistor (R908, R909) to the inputs to the switch so that these signals are held high when the AMC JTAG interface is selected.

16. Add 22-ohm series termination resistors at the outputs MCMTXPMCLK and MCMRXFCLK which are HyperLink sideband signal clock outputs.
17. Add a temperature monitor to the unused TEMP2 input to the UCD9222
18. Add 4.7K pull-down resistors on the GPIO[15:1] pins and a 4.7K pull-up resistor on GPIO[0] so that these pins are not floating after FPGA release.
19. Replace the 14-pin JTAG with the Spy-Bi-Wire interface .
20. Add 0 Ohm resistors on all power enable signals.
21. ADD R485 for DSP UARTTXD termination
22. DSP_PCIECLK was set from IN2.
23. Change R425 and R426 package from 0603 to 0402.
24. Change R58 package from 0603 to 0402.
25. To modify the title from C6678 to CLOCK GEN3
26. Change net name from Isenes-2A to Isenes-2A
27. U4, U5, U6, U16 U8 change to SAMSUNG_K4B1G1646G
28. NL/U8
29. NL/R431, NL/R432, R435

DSPM-8301 A103-1 / 19C2830102

1. Page26: Change mini-USB to through-hole type
2. Page13: Change the registers value to 2k ohms and the pull-up voltage to IO 1.8V on the DDR3 slew rate pins
3. Page22,23: Add the test points on unused clock inputs and outputs of CDCE62005s
4. Page10: Enable the expansion I2C by default, populate the registers of R160 and R161 for I2C connections between C6678 and AMC finger
5. Page23: Modify the CLK2 (CDCE62005) inputs for the common HyperLink timing, TCLKB will be the PRI_REF input and branch another one to the FPGA by two pairs. The 100MHz input from CLK3 CDCE62005 will be changed to its SEC_REF input.
6. AGND change to GND
7. Leave R160 and R161 as NL and add 2 more resistors on these nets connecting to AMC connector pins 159 and 160. Install 0 ohms in these new resistors

DSPM-8301 A104-1 / 19C2830103

1. Remove R484 and R487 and cross-wire these signals to make the connections functionally match the C6670 EVMs
2. Change R433 to 10k, change R434 to 1.2k, change R12 and R17 from 0 ohm to 0.1uF
IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated (“TI”) reference designs are solely intended to assist designers (“Buyers”) who are developing systems that incorporate TI semiconductor products (also referred to herein as “components”). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer’s systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. **TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.** TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

**TI REFERENCE DESIGNS ARE PROVIDED “AS IS”. TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER’S USE OF TI REFERENCE DESIGNS.**

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer’s safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have not been so designated is solely at Buyer's risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2015, Texas Instruments Incorporated