Optimized Radar System Design Using 66AK2L06 DSP+ARM® SoC and ADC14X250

Table of Contents

<table>
<thead>
<tr>
<th>Page Number</th>
<th>Page Name</th>
<th>Page Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>k2l soc_05.SchDoc</td>
<td>K2L Resets, Core PLL and SERDES PLL Inputs</td>
</tr>
<tr>
<td>13</td>
<td>k2l soc_06_1.SchDoc</td>
<td>K2L Boot-Config, I2C, SPI, UART, Timer, and USIM</td>
</tr>
<tr>
<td>15</td>
<td>k2l soc_08.SchDoc</td>
<td>K2L DFE, JESD204B SYSREF, SYNCHOUT and DFE I/O</td>
</tr>
<tr>
<td>25</td>
<td>adc14x250_01.SchDoc</td>
<td>ADC power pins, power filtering and decoupling capacitors</td>
</tr>
<tr>
<td>26</td>
<td>adc14x250_02.SchDoc</td>
<td>ADC input, JESD204B interface, SPI and discrete I/O control</td>
</tr>
<tr>
<td>30</td>
<td>lmk04828_01.SchDoc</td>
<td>LMK04828 power pins, power filtering and decoupling capacitors</td>
</tr>
<tr>
<td>31</td>
<td>lmk04828_02.SchDoc</td>
<td>Clock input, clock output, SPI and discrete I/O control</td>
</tr>
</tbody>
</table>

Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rev 1.0</td>
<td>Initial revision release</td>
</tr>
</tbody>
</table>
TI66AK2L06 and ADC14X250 Example System Diagram

66AK2L06 SoC

ADC14X250

MDIO
DDR3ACLK
PCIECLK
SGMIICLK

66AK2L06 SoC

DDR3A (72-bit)

USB 3.0 Super-Speed

 תמיד
do not warrant the accuracy or completeness of this specification or any information contained herein. Texas Instruments and/or its licensors do not warrant that the design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is evaluated worth. You should completely validate and test your design implementation to confirm the system functionality for your application.

http://www.ti.com

Optimized Radar System Design Using 66AK2L06 DSP+ARM® SoC and ADC14X250 Project Title:

Designed for:

Public Release

Assembly Variant:

001

©

Texas Instruments 2015

Drawn By:

Engineer:
a0271760

Version control disabled

SVN Rev:

Number:

E1

ChangeMe!

TID #:

TIDEP0060

Orderable:

http://www.ti.com/support

http://www.ti.com
TI66AK2L06 and ADC14X250 Example System Power Supply Diagram

Channel 1: 3.3V, 4A
Channel 2: 1.8V, 4A
Channel 3: 0.90V, 2A
Channel 4: 1.9V, 2A

Buck Converter
PMBUS Control
TPS65400

TI66AK2L06 SoC Power Nets
– 1.05V, 15A

Serdes Low Voltage (0.85V)
Super-Speed Supply (0.85V)
Super-Speed Supply (3.3V)
USB Digital Supply (3.3V)
DDR3A DLL Supply (1.8V)
Charge Pump 2 3.3V

ADC14X250 Power Nets
Analog 3.0 V
Analog 1.8 V
Analog 1.2 V

Note: Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained herein. Texas Instruments and/or its licensors do not warrant that the design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is evaluation worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
The diagram illustrates the system clocking for the TI66AK2L06 and ADC14X250 Example System. It shows the reference clocks for various components, including PLLs and other oscillators. The diagram also indicates the clock rates and connections between different modules. The example system is designed for optimized Radar System Design Using 66AK2L06 DSP+ARM® SoC and ADC14X250.

Key components and their clocks include:
- **TI66AK2L06 SoC Reference Clocks**: SYSCLK, CSISC2_0_CLK, DEVCLK, SDCLKout_0, SDCLKout_1, SDCLKout_5, DCLKout_1, DCLKout_4, DCLKout_6.
- **ADC14X250 Reference Clocks**: SYSREF, ADC Sampling Clock, REF Clock, JESD204B SYSREF.
- **CDCM6208 v2 Reference Clocks**: DCLKout_0, DCLKout_1, DCLKout_4, 156.25 MHz, 100 MHz, 100 MHz.
- **SPI Control Reference Clocks**: Y0, Y1, Y2, Y3, OSG, 110 MHz, 110 MHz, 110 MHz.
- **PCI Express SERDES Clocks**: PCIECLK, PCIe Clock, PCIe Reference Clock, 100 MHz, 100 MHz.
- **JESD204B SERDES Clocks**: 4.9125Gbps, 122.88 MHz, 122.88 MHz, 122.88 MHz.
- **JESD204B Reference Clocks**: JESD204B SYSREF, DFESYSREF, 245.76 MHz.
- **DSM Clocks**: 32.768KHz XO, 16MHz XO, 19.2MHz TCXO, 25MHz TCXO.
- **USB Clocks**: USBCLK, USB Clock, 100 MHz, 100 MHz, 100 MHz.
K2L Reset and Core Configuration

K2L Core Reference Clock Inputs

For schematic and layout recommendations and requirements see the K2L product page listed below.

TI 66AK21.06 Product Page

For K2L BOOTMODE and RESET pins mastered by Boot Manager Controller (microcontroller) not shown here.

AC-coupling is necessary.

K2L PLLLOCK monitored by System Controller (microcontroller) not shown here.

K2L BOOTCOMPLETE monitored by System Controller (microcontroller) not shown here.
K2L Boot-Config, I2C, SPI, UART, Timer, and USIM

Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. You should completely validate and test your design implementation to confirm the system functionality for your application.
JESD204B SERDES shall be routed according to DFE User Guide.

JESD204B SYSREF and SYNC shall be utilized according to DFE User Guide.

The Keystone 2 SERDES User Guide is necessary.

External bias or termination network is not necessary.
For schematic and layout recommendations and requirements see the ADC14X250 product page linked below.

TI ADC14X250 Product Page

ADC Power Pins and Decoupling Capacitors

*Decoupling caps shall be placed as close to ADC power pins as possible. Use minimum via dog bones (see next page) to ensure lowest possible mounting inductance.

Each VAD1.2 pin should include a 0.1uF and 0.01uF capacitor

Each VAD1.8 pin should include a 0.1uF and 0.01uF capacitor

Each BP2.5 pin should include a 0.1uF and 0.01uF capacitor

Each VAD2.0 pin should include a 0.1uF and 0.01uF capacitor

The ADC14x250 thermal pad (PIN0) provides thermal dissipation for the ADC. Please ensure layout includes ground-stitching vias to create a good thermal coupling between the ADC GND pad and the PCB GND layers.
ADC Input, JESD204B Interface, SPI and Discrete I/O Control

ADC input signal conditioning (bias, op-amps, etc) is not shown here. The input circuit required is application and system specific. Please see ADC14X250 datasheet, application notes and user guides for specific requirements.

ADC common-mode input voltage can be optionally supplied from on-die regulator or externally supplied VCM pin.

For schematic and input recommendations and requirements see the ADC14X250 product page linked below.

TI ADC14X250 Product Page
LMK04828 Decoupling Capacitors

LMK04828 decoupling shall be placed as close to the IC package as possible. See LMK04828 datasheet and EVM for example decoupling layout.

Engineer: [Signature]
Drawn By: [Signature]

© 2015 Texas Instruments Incorporated

Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

Warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated (“TI”) reference designs are solely intended to assist designers (“Buyers”) who are developing systems that incorporate TI semiconductor products (also referred to herein as “components”). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer’s systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. **TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.** TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used.

Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS ARE PROVIDED “AS IS”. TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER’S USE OF TI REFERENCE DESIGNS.

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer’s safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have not been so designated is solely at Buyer's risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.