co licences do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
K2L CVDD CorePower Supply Pins and Decoupling

- 71 CVDD pins
- Core Supply
  - Smart-Reflex (0.95V to 1.05V)
- VDD/VSS/COMMON/CVDD feedback signals routed to TPS544x regulator feedback pins
- VDD/VSS/COMMON/CVDD feedback signals routed to TPS544x regulator feedback pins

**Note:** Recommended PSRR factor simulation to select excess capacitor value in given location and package type.

- 20 caps
- 11 caps
- 10 caps

**Recommended:** Use layer structure to improve signal integrity and decoupling

**Contact:** Orderable: Assembly Variant:

© Texas Instruments
Place larger package caps and ferrites as close to BGA as possible
Place larger package caps and ferrites as close to BGA as possible
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Place larger package caps and ferrites as close to BGA as possible
Place larger package caps and ferrites as close to BGA as possible
K2L Core and Peripheral PLL Reference Clock Inputs

- K2L_SYSCLK sourced by LMK04288B. When using LVDS outputs of LMK04288 only AC coupling is necessary.
- DDR3 controller reference clock solution not shown. Please see K2L EVM schematics.
- Not utilizing ALTCORECLK. Pull-up/down resistor necessary to reserve off clock input.
- Chip-Level PLL References Inputs
- Place AC-coupling as close to BGA as possible.

K2L Reset and Core Configuration

- K2L_BOOTMODE and RESET pins mastered by Board Management Controller (microcontroller) not shown here.
- K2L_CORESEL[2:0] and LRESET/NMIZ/LRESETNMIENZ signals all mastered by Board Management Controller (microcontroller) not shown here.
- K2L_BOOTMODE and RESET pins mastered by Board Management Controller (microcontroller) not shown here.

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For schematic and layout recommendations and requirements see the K2L product page linked below.

TI 66AK2L.06 Product Page
Board management controller (microcontroller) can also master the device boot configuration options as required by application. Recommend designer to utilize pull-up/pull-downs to select default boot-mode pins and reset pins during device boot configuration options as required by application.

K2L Default Boot Configuration Options

K2L Default Static Configuration Options

Selecting the following static configuration options:

- LENDIAN = 0x1
- WAN_PLL_DDR_SEL = 0x0
- ARM_BENDIAN = 0x0
- CSSEL2_0_MUX = 0x0 - Selects JESD Lane0
- CSSEL2_1_MUX = 0x0 - Selects JESD Lane1
- AVSSSEL = 0x0 - 0x0

Recommended designer should utilize pull-up/pull-downs to select default device static configuration options as required by application.

Board management controller (microcontroller) can also master the boot-mode pins and reset pins during device boot configuration options as required by application.

Please see K2L Data Manual Boot Configuration sections for details.
K2L Boot-Config, I2C, SPI, UART, Timer, and USIM

TI K2L Demo 4 software utilizes SPI_0 for controlling ADC

TI K2L Demo 4 software utilizes SPI_1 for controlling DAC

TI K2L Demo 4 software utilizes I2C_0 for configuring/reading ADC temperature sensor.

VSYNC, VDD

10.0 R17
10.0 R18
10.0 R19

10.0 R20
10.0 R21
10.0 R22

TI K2L Demo 4 software utilizes SPI_0 for controlling ADC

TI K2L Demo 4 software utilizes SPI_1 for controlling DAC

TI K2L Demo 4 software utilizes I2C_0 for configuring/reading ADC temperature sensor.

VSYNC, VDD

10.0 R17
10.0 R18
10.0 R19

10.0 R20
10.0 R21
10.0 R22

I2C0 utilized for Smart-Reflex control of TPS544x24 CVDD power supply. Solution not shown here. Please see K2L EVM schematics.

UART port typically utilized as a Linux terminal interface.
K2L JTAG and Emulation Trace Port

The design of the JTAG and Emulation Trace Port should match the logic level of the board management controller. The TGTRSTZ pin pull-up should match the logic level of the board management controller.

Notes:
- MSB EMU port signals not utilized
- K2L_MIPI_EMU07 pin pull-up should match logic level of board management controller
- K2L_MIPI_EMU14 pin pull-up should match logic level of board management controller

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K2L DDR3 Controller - Clock, Address, Command and Control

DDR3 Clock, Address, Command and Control "Fly-by" Termination

Not utilizing Rank1 Signals

All termination for clock, address, command and control nets shall be placed at the end of the "fly-by" routing.

**K2L DDR3A[15..0]**

Rank1 Clock

K2L_DDR3_CLKOUTP0

K2L_DDR3_CLKOUTN0

Rank1 Clock

K2L_DDR3A[15..0]

Not utilizing Rank1 Signals

Rank1 Signals

All termination for clock, address, command and control nets shall be placed at the end of the "fly-by" routing.

**K2L_DDR3A[15..0]**

Rank1 Clock

K2L_DDR3_CLKOUTP0

K2L_DDR3_CLKOUTN0

Rank1 Clock

K2L_DDR3A[15..0]

Not utilizing Rank1 Signals

Rank1 Signals

All termination for clock, address, command and control nets shall be placed at the end of the "fly-by" routing.

**K2L DDR3A[15..0]**

Rank1 Clock

K2L_DDR3_CLKOUTP0

K2L_DDR3_CLKOUTN0

Rank1 Clock

K2L_DDR3A[15..0]

Not utilizing Rank1 Signals

Rank1 Signals

All termination for clock, address, command and control nets shall be placed at the end of the "fly-by" routing.

**K2L DDR3A[15..0]**

Rank1 Clock

K2L_DDR3_CLKOUTP0

K2L_DDR3_CLKOUTN0

Rank1 Clock

K2L_DDR3A[15..0]

Not utilizing Rank1 Signals

Rank1 Signals

All termination for clock, address, command and control nets shall be placed at the end of the "fly-by" routing.

**K2L DDR3A[15..0]**

Rank1 Clock

K2L_DDR3_CLKOUTP0

K2L_DDR3_CLKOUTN0

Rank1 Clock

K2L_DDR3A[15..0]

Not utilizing Rank1 Signals

Rank1 Signals

All termination for clock, address, command and control nets shall be placed at the end of the "fly-by" routing.

**K2L DDR3A[15..0]**

Rank1 Clock

K2L_DDR3_CLKOUTP0

K2L_DDR3_CLKOUTN0

Rank1 Clock

K2L_DDR3A[15..0]
K2L DDR3 Controller - Data Byte-Lanes

DDR3 byte-lane signals shall be routed in point to point topology as shown in the application report "DDR3 Design Requirements for Keystone Devices" (sprabi1b).

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All decoupling and ferrites shall be placed as close as possible to the SDRAM power pins.
All decoupling and ferrites shall be placed as close as possible to the SDRAM power pins.
K2L Time-Stamp (IEEE1588) Peripheral

Time-Stamp peripheral not utilized.

Antenna Texas Subsystem:

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K2L EMIF16 Interface

2Gbyte, x8 NAND Flash

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K2L PCIe and SGMII Interfaces

*PCIe/SGMII SERDES TX/RX not utilized. REFRES still required to be installed.

*SGMII SERDES not utilized. REFRES still required to be installed.

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Contact:
Decoupling caps shall be placed as close to ADC power pins as possible.

The thermal pad is a large ground connection for the ADC. Ensure good connection through multiple vias to the PCB ground planes.

The ADC thermal pad is large ground connection for the ADC. Ensure good connection through multiple vias to the PCB ground planes.

Please decoupling capacitor as close to ADC as possible.

Heat-sink may be required to keep ADC operating under datasheet limits.

*ADC digital inputs VIL = 0.8 V, VIH = 0.4 V
*ADC digital inputs VIL = 0.8 V, VIH = 0.4 V

*ADC digital inputs VIL = 0.8 V, VIH = 0.4 V

Heat-sink may be required to keep ADC operating under datasheet limits.

*ADC digital inputs VIL = 0.8 V, VIH = 0.4 V

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Heat-sink may be required to keep ADC operating under datasheet limits.

*ADC digital inputs VIL = 0.8 V, VIH = 0.4 V

Heat-sink may be required to keep ADC operating under datasheet limits.
ADC Analog Input Filtering and Balancing

Default resistor/capacitor configuration matching ADC32RF4x EVM

- Place all input signal grounds close to transformers
- Shared pads used to provide optimal functionality

ADC input channel signal paths shall be routed as 50-ohm characteristic impedance paths.

- Place all input signal grounds close to transformers
- Shared pads used to provide optimal functionality

- Place all input signal grounds close to transformers
- Shared pads used to provide optimal functionality
The input circuit required is application specific. Please see ADC12J4000 datasheet, application notes and EVM design guide for specific recommendations.
For schematic and layout recommendations and requirements, see the DAC38J84 product page linked below.

**DAC Output, JESD204B Interface, SPI and Discrete I/O Control**

Optional external low-pass filter element. Should be placed as close as possible to DAC BGA.

Please see DAC38J84 datasheet, application notes and EVM design guide for specific recommendations.

Please see DAC38J84 datasheet, application notes and EVM design guide for specific recommendations. Possible to DAC BGA.

The output circuit required for the DAC is application specific. Please see DAC38J84 datasheet, application notes and EVM design guide for specific recommendations.

The output circuit required for the DAC is application specific. Possible to DAC BGA.

For schematic and layout recommendations and requirements, see the DAC38J84 product page linked below.

*Note: The full-scale current output according to dashaet equation:

\[ I_{OUT} = \frac{(V_{DAC} - 1V) \times 1616 \times \frac{64}{1616} \times V_{REF}}{1616 + \frac{64}{1616} \times V_{ESKTI} \times \frac{64}{1616}} \]

*Note: DAC's digital I/O software will utilize the differential, LVDS JESD204B interface. Utilizing the SYNC_AB and SYNC_CD pins is an optional usage of the K2L_DFEIO pins to receive the SYNC signal from the DAC.

See DAC38J84 datasheet for implementation details.
Place all DAC output transformers close to transformers.

Place all DAC output structures close to transformers.

All DAC input channel signal paths shall be routed as 50-ohm characteristic impedance paths.

Please ground clip near associated DAC input channel transformers.

Please ground clip near associated DAC input channel transformers.

Exact transformer characteristics should be chosen based on bandwidth of interest for signals being detected. Please see the ADC32RF65/65G subline for additional design considerations.

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All ADC input channel signal paths shall be routed as 50-ohm characteristic impedance paths.

Place ground clip near associated DAC input channel transformers.

DAC Analog Output Filtering and Balancing - Channels 2 and 3

Exact transformer characteristics should be chosen based on bandwidth of interest for signals being detected. Please see the ADS28RF96/95/99 datasheets for additional design considerations.

Place all DAC output structures close to transformers.

Place ground clip near associated DAC input channel transformers.
LMK04828 Decoupling Capacitors

LMK04828 decoupling shall be placed as close to the IC package as possible. See LMK04828 datasheet and EVM for example decoupling layout.
For schematic and layout recommendations and requirements see the LMK04828 product page linked above.

LMK04828 Reference Clock Input, SPI Control, SYSCLK, SYSREF and Reference Clock Output

19.2 MHz TCXO

Special care should be taken to GND isolate CLKIN0 signal.

The JESD1 SERDES clock for the K2L

LMK04828 Reference Clock Input, SPI Control, SYSCLK, SYSREF and Reference Clock Output

The schematic and layout recommendations and requirements see the LMK04828 product page linked above.

All unused pins shall be routed with short stubs to aid in stability and mechanical robustness. Indicated by the LMK04828 unused pin test network.

19.2 MHz TCXO

Special care should be taken to GND isolate CLKIN0 signal.

For schematic and layout recommendations and requirements see the LMK04828 product page linked above.

LMK04828 DC5VOUT1 used as the device clock for the DAC

LMK04828 DC5VOUT2 used as the SYSREF for the DAC

LMK04828 DC5VOUT3 used as the SYSREF for the DAC

LMK04828 SPI pin used by System Controller (microcontroller) not shown here.

LMK04828 DC5VOUT0 used as the device clock for the DAC

LMK04828 DC5VOUT1 used as the device clock for the DAC

LMK04828 DC5VOUT2 used as the SYSREF for the K2L

LMK04828 DC5VOUT3 used as the SYSREF for the K2L

LMK04828 DC5VOUT0 used as the device clock for the DAC

LMK04828 SPI pin used by System Controller (microcontroller) not shown here.

LMK04828 DC5VOUT1 used as the device clock for the DAC

LMK04828 DC5VOUT2 used as the SYSREF for the K2L

LMK04828 DC5VOUT3 used as the SYSREF for the K2L

LMK04828 SPI pin used by System Controller (microcontroller) not shown here.

LMK04828 DC5VOUT0 used as the device clock for the DAC

LMK04828 SPI pin used by System Controller (microcontroller) not shown here.

LMK04828 DC5VOUT1 used as the device clock for the DAC

LMK04828 DC5VOUT2 used as the SYSREF for the K2L

LMK04828 DC5VOUT3 used as the SYSREF for the K2L

LMK04828 SPI pin used by System Controller (microcontroller) not shown here.

LMK04828 DC5VOUT0 used as the device clock for the DAC

LMK04828 SPI pin used by System Controller (microcontroller) not shown here.

LMK04828 DC5VOUT1 used as the device clock for the DAC

LMK04828 DC5VOUT2 used as the SYSREF for the K2L

LMK04828 DC5VOUT3 used as the SYSREF for the K2L

LMK04828 SPI pin used by System Controller (microcontroller) not shown here.

LMK04828 DC5VOUT0 used as the device clock for the DAC

LMK04828 SPI pin used by System Controller (microcontroller) not shown here.

LMK04828 DC5VOUT1 used as the device clock for the DAC

LMK04828 DC5VOUT2 used as the SYSREF for the K2L

LMK04828 DC5VOUT3 used as the SYSREF for the K2L

LMK04828 SPI pin used by System Controller (microcontroller) not shown here.

LMK04828 DC5VOUT0 used as the device clock for the DAC

LMK04828 SPI pin used by System Controller (microcontroller) not shown here.

LMK04828 DC5VOUT1 used as the device clock for the DAC

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LMK04828 DC5VOUT3 used as the SYSREF for the K2L

LMK04828 SPI pin used by System Controller (microcontroller) not shown here.

LMK04828 DC5VOUT0 used as the device clock for the DAC

LMK04828 SPI pin used by System Controller (microcontroller) not shown here.

LMK04828 DC5VOUT1 used as the device clock for the DAC

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LMK04828 DC5VOUT3 used as the SYSREF for the K2L

LMK04828 SPI pin used by System Controller (microcontroller) not shown here.

LMK04828 DC5VOUT0 used as the device clock for the DAC

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LMK04828 DC5VOUT1 used as the device clock for the DAC

LMK04828 DC5VOUT2 used as the SYSREF for the K2L

LMK04828 DC5VOUT3 used as the SYSREF for the K2L

LMK04828 SPI pin used by System Controller (microcontroller) not shown here.

LMK04828 DC5VOUT0 used as the device clock for the DAC

LMK04828 SPI pin used by System Controller (microcontroller) not shown here.

LMK04828 DC5VOUT1 used as the device clock for the DAC

LMK04828 DC5VOUT2 used as the SYSREF for the K2L

LMK04828 DC5VOUT3 used as the SYSREF for the K2L

LMK04828 SPI pin used by System Controller (microcontroller) not shown here.

LMK04828 DC5VOUT0 used as the device clock for the DAC

LMK04828 SPI pin used by System Controller (microcontroller) not shown here.
Decoupling capacitors shall be placed as close as possible to the CDCM500D power pins.

Secondary input is unused.

Drug information is not intended to take the place of informed, expert advice from your pharmacist about any medication or health-related issues.

fPFD=25MHz, and ICP=2.5mA:
All feedback line should be routed as close to the highest loaded section of the target power plane to account for the highest IR drop on the plane.

Channel 1 - System 3.3V @ 4A
Channel 2 - System 1.8V @ 4A
Channel 3 - K2L 0.850V @ 2A
Channel 4 - K2L 1.0V @ 2A

393K sets up a 393kHz switching frequency. See the TPS65400 datasheet and TI Web Bench for optimization options.

Reset line to the VDD regulator output to automatically come out of reset on power on. Reset can also be controlled by Board Management Controller (microcontroller) not shown here.

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TPS65400 Quad Channel Buck Controller #2

Channel 1 - K2L and DDR3 SDRAM 1.35V @ 4A
Channel 2 - System 1.15V @ 4A
Channel 3 - System 0.9V @ 2A
Channel 4 - System 1.9V @ 2A

All feedback line should be routed as close to the highest sided section of the target power plane to account for the highest IR drop on the plane.

NDRK sets up a 393kHz switching frequency. See the TPS65400 datasheet and TI Web Bench for optimization options.

Reset line to the VDDQ regulator output to automatically come out of reset on power-on. Reset can also be controlled by Board Management Controller (microcontroller) not shown here.

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TI Web Bench Link: TPS54620 12V Input, 3.3V @ 2A output

For design details, please see the below TI Web Bench link.

Feedback resistors shall be routed to the termination resistors of the power pins.

All decoupling and ferrites shall be placed as close as possible to the TPS51200 power pins.

TPS51200 #1 - 3.3V Auxillary Supply for Board Management Controller

TPS51200 - DDR3 VTT/VREF Push-Pull Converter

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TPS54620 #2 - USB 5.0V Buck Converter

For design details, please see the below TI Web Bench link.

For design details, please see the below TI Web Bench link.
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