All the nets highlighted are high current carrying and high voltage carrying, appropriate clearance and width is needed.
Place U1 close to Q1 and Q2, and minimize distance between Q1_Gate and U1-OUTA, Q2_Gate and U1-OUTB, VSS1 & VSS2 and Q1-Source.

Place U2 close to Q3 and Q4, and minimize distance between Q3_Gate and U2-OUTA, Q4-Gate and U2-OUTB, VSS1 & VSS2 and Q3-Source.

Place U3 close to Q5 and Q6, and minimize distance between Q5_Gate and U3-OUTA, Q6-Gate and U3-OUTB, VSS1 & VSS2 and Q5-Source.

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License: Texas Instruments C8051F320 System-C2000 Three Phase PFC (Vienna Rectifier)

Engineer: Manish Bhardwaj

Contact: SVN Rev:

File: Size:

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The connection from RSH3 should be close to U9, also a small GND island needs to be created w.r.t. RSH3_2 to help with the layout.

The connection from RSH2 should be close to U8, also a small GND island needs to be created w.r.t. RSH2_2 to help with the layout.

The connection from RSH1 should be close to U7, also a small GND island needs to be created w.r.t. RSH1_2 to help with the layout.
SD CLK, SD, DATA1/2/3 are 20MHz signal, try to keep lengths the same.
These signals must be kept away from analog signals.
SD_CLK source is pin 57, R100 is DNP as pin 75 is not connected.

Need to add some wire length from RS9 to pin 101, 103 and 107 so that the length matches, does not have to be super accurate.

Please use HSEC180 PCB snippet.
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