The D<7:0> connections polarity have been swapped from the TI standard. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
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As illustrated on the schematic, add short stub traces extending out from the package to aid solderability.

Let C114 and C113 share a pad on the common net. Let C123 and C112 share a pad on the common net.

Polarity inversion on these 2 signals

Le C113 and C112 share a pad on the common
3.3V supply to clocks (LMK, LMX) and LEDs

1.8V and 1.2V supply to LM1585S1 & ADC12UX03S

12V main supply, from jack or via FMC connector to regulators

3.3V supply to clocks (LMK, LMX) and LEDs

Locate at edge opposite FMC connector

12V main supply, from jack or via FMC connector to regulators

Add text label: "5V VIA JACK" and "12V VIA FMC, Install R90 for 12V operation"
<table>
<thead>
<tr>
<th>Place at least two of the GND test points in the power section.</th>
</tr>
</thead>
</table>

**PCB Label**

**ZZ1**
This Assembly Note is for PCB labels only.

**ZZ2**
These assemblies are ESD sensitive. ESD precautions shall be observed.

**ZZ3**
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

**ZZ4**
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

**PCB Number** 600M17

**PCB Rev. A**

**PCB LOGO**
Texas Instruments

**PCB**

**ESD LOGO**
ESD Susceptible

**PCB**

**ESD LOGO**
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