NOTES, UNLESS OTHERWISE SPECIFIED:

1. The netname "DMD_P3P3V" represents connection to the +3.3V digital power plane.
2. The symbol \( \downarrow \) represents connection to the digital ground plane.
3. A "Z" suffix on a signal name indicates an active low signal.
4. All components with designators "U", "D", "Y" and "Q" are electrostatic discharge sensitive.
5. All resistor values are in ohms, 1/16W and 5% unless otherwise specified.

HIGHEST REFERENCE DESIGNATORS USED

<table>
<thead>
<tr>
<th>C103</th>
<th>D5</th>
<th>J4</th>
<th>L5</th>
<th>A56</th>
<th>J911</th>
<th>Q7</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q9</td>
<td></td>
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</tbody>
</table>
From Slave ASIC

From Master ASIC

Input Flex Connector

A/B DMD DATA (DD_AP[15:0], DD_AN[15:0], DD_BP[15:0], DD_BN[15:0])

A/B DMD CLK (DCLK_AP, DCLK_AN, DCLK_BP, DCLK_BN)

A/B SCTRL (SCTRL_AN, SCTRL_AP, SCTRL_BN, SCTRL_BP)

C/D DMD DATA (DD_CP[15:0], DD_CN[15:0], DD_DP[15:0], DD_DN[15:0])

C/D DMD CLK (DCLK_CP, DCLK_CN, DCLK_DP, DCLK_DN)

C/D SCTRL (SCTRL_CN, SCTRL_CP, SCTRL_DN, SCTRL_DP)

SCP CONTROL (CLK, DO, DI, ENZ, IRQZ)

DAD CONTROL (STROBE, MODE[1:0], SEL[1:0], ADDR[3:0], OEZ)

DMD_RSTZ

U2

DMD Power Supplies

U3

0.7 TRP S610 DMD

VBIAS

VRESET

PG_OFFSET

EN_OFFSET

VOFFSET

3.3V

2.3V to 3.4V

3.3V

3.3V to 2.6V

DWN DATE

ISSUE DATE

SCALE

DRAWING NO REV

SHEET OF
Note: Do not install R3 if there is a pull-up on the SCP_DMD_CSZ signal on the Main board.

Note: R4 and C5 are specific values selected to delay DADSEL_0 to allow the DMD enough time to park properly. Recommended installing values as shown.
Bring TP for reset waveform MBRST 0, 15 outside of DMD outline.
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