NOTES, UNLESS OTHERWISE SPECIFIED:

1. The netname "P1P1V" represents connection to the +1.1V FPGA power plane
2. The netname "P1P1V_FIL" represents connection to the +1.1V filtered FPGA power plane
3. The netname "P1P1V_M" represents connection to the +1.1V Master ASIC power plane
4. The netname "P1P1V_S" represents connection to the +1.1V Slave ASIC power plane
5. The netname "P1P15V" represents connection to the +1.15V FPGA power plane
6. The netname "P1P15V_FIL" represents connection to the +1.15V filtered FPGA power plane
7. The netname "P1P5V" represents connection to the +1.5V FPGA power plane
8. The netname "P1P5V_FIL" represents connection to the +1.5V filtered FPGA power plane
9. The netname "P1P8V_M" represents connection to the +1.8V Master ASIC power plane
10. The netname "P1P8V_S" represents connection to the +1.8V Slave ASIC power plane
11. The netname "P1P8V_M" represents connection to the +1.8V Master ASIC power plane for the PLLs
12. The netname "A1P8V_M" represents connection to the +1.8V Master ASIC power plane for the PLLs
13. The netname "A1P8V_S" represents connection to the +1.8V Slave ASIC power plane
14. The netname "P2P5V" represents connection to the +2.5V FPGA power plane
15. The netname "P2P5V_FIL" represents connection to the +2.5V filtered FPGA power plane
16. The netname "P2P5V_M" represents connection to the +2.5V Master ASIC power plane
17. The netname "P2P5V_S" represents connection to the +2.5V Slave ASIC power plane
18. The netname "P3P3V" represents connection to the +3.3V FPGA power plane
19. The netname "P3P3V_M" represents connection to the +3.3V Master ASIC power plane
20. The netname "P3P3V_S" represents connection to the +3.3V Slave ASIC power plane
21. The netname "P5V" represents connection to the +5V power plane
22. The netname "GND" represents connection to the ground plane
23. A "Z" suffix on a signal name indicates an active low signal
24. All components with designators "U*", "Q*", "D*" are electrostatic discharge sensitive.
25. All components with designators above 500 are mounted on the bottom side of the board.
26. All resistor values are in ohms.

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TIDA-01347 P66 4KUHD Formatter Board

DRAWING NO 2514423

APPROVED: DH

DATE: 4/13/2015

APPLICATION: Cadence 16.6
Note: MSEL[4:0] = 10011 for AS mode, standard POR delay
The connection from U24-15 to P3P5V is a blue wire on existing Rev A pwb's.

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Note: See ASIC datasheet for Dual ASIC oscillator requirements on applications using DynamicBlack or BrightSync.
NOTE:
R620, R634, R69, R102, R131, R85 are used for current measurement and are not required for production units.
R713, R100, R232, R638 and R685 are used for alternate lab supplies and are not required for production units.

NOTE: Consult the PMD1000 Data Sheet for external component specifications.

IMPORTANT NOTE: The PCB should be designed such that the specifications are not exceeded when the DDP442x is operated under the maximum current conditions specified in the DDP442x datasheet.
NOTE: Consult the PMD1000 data sheet for material component specifications.

IMPORTANT NOTE: The PCB should be designed such that the specifications are not exceeded when the DDP442x is operated under the maximum current conditions specified in the DDP442x datasheet.

NOTE: R587, R525, R46, R576, R14 are used for current measurement and are not required for production units.

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NOTE: This resistor value is dependant upon the CW motor used. The value range is 0.47 ohms to 2.2 ohms. The target voltage range for the SENSE pin is 100-150mV when the CW is running at a stable speed.
JTAG BOUNDARY SCAN

DO NOT INSTALL JTAG BOUNDARY SCAN

NOTE: TRSTZ should be pulled down for production designs.

REALVIEW ICE
JTAG I/F

TRSTZ p.23,24
TCK p.23,24
TDI p.23
TMS1 p.23,24
TMS2 p.23,24
TDO1 p.24
TDO2 p.24
S_TDO1 p.24
TRSTZ p.23,24
TDI p.23
TRSTZ p.23,24
TDI p.23
TMS1 p.23,24
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TMS2 p.23,24
TCK p.23,24
RTCK p.24
SEQ_SYNC p.24
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Master ASIC Test Points, ARM Trace, JTAG, and Reset
Note: TI recommends signal integrity analysis be performed for the SPI bus to determine the optimum buffering and termination.
Note: TI reference design supports both TSOPII-48 and TSOPII-56 Flash types. The reference design uses a TSOPII-48 Flash part. Please refer to diagram below for pinout and footprint comparison.
Note: TI reference design supports both TSOPII-48 and TSOPII-56 flash types. The reference design uses a TSOPII-48 flash part. Please refer to diagram below for pinout and footprint comparison.
Note: U529 is needed to read from an OSRAM driver.
Slave ASIC GPIO and Smooth Picture I/F

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Revision B:
All Pages: Resequenced reference designators to align with layout
Page 1: Updated notes with correct voltage names
Page 4: Rearranged DDR3_1_DQ[15:0] for routability

Revision C:
Page 3: Change U5 to Do Not Install
Updated C545 and C549 as Do Not Install
Changed U506 to 75 Mhz
Page 11: Added Note Connecting pin 15 of U24 to P3P3V
Page 8: Changed R89, R90, R91, R92, and R541 to 0 ohms.

Revision D:
Page 3: Changed net name TEST_4A_AC6 to VX1_3D_EN.
Changed net name TEST_4A_AE6 to VX1_LR_SYNC.
Page 8: Added R190, R191, R192, and R193.
Changed net name TEST_4A_AC6 to VX1_3D_EN.
Changed net name TEST_4A_AE6 to VX1_LR_SYNC.
Page 11: Connected pin 15 of U24 to P3P3V.
Page 16: Changed C799 and C801 to 1800pF.
Page 21: Added note to ballast circuit.
Page 22: Added R188 and R189.
Page 23: Changed RN501 to Install, added J52 header.
Page 24: Changed RN500 to Install, added J53 header.

Revision E:
Page 11: Changed U24-10, C85 connection from P3P3V to P5V_S.
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