NOTES, UNLESS OTHERWISE SPECIFIED:

1. The netname "DMD_P3P3V" represents connection to the +3.3V digital power plane.
2. The symbol \( \mathbf{\Box} \) represents connection to the digital ground plane.
3. A "Z" suffix on a signal name indicates an active low signal.
4. All components with designators "U", "D", "Y" and "Q" are electrostatic discharge sensitive.
5. All resistor values are in ohms, 1/16W and 5% unless otherwise specified.
J1 & J2
Input Flex Connector

From Slave ASIC
- A/B DMD DATA (DD_AP[15:0], DD_AN[15:0], DD_BP[15:0], DD_BN[15:0])
- A/B DMD CLK (DCLK_AP, DCLK_AN, DCLK_BP, DCLK_BN)
- A/B SCTRL (SCTRL_AN, SCTRL_AP, SCTRL_BN, SCTRL_BP)

From Master ASIC
- C/D DMD DATA (DD_CP[15:0], DD_CN[15:0], DD_DP[15:0], DD_DN[15:0])
- C/D DMD CLK (DCLK_CP, DCLK_CN, DCLK_DP, DCLK_DN)
- C/D SCTRL (SCTRL_CN, SCTRL_CP, SCTRL_DN, SCTRL_DP)

DAD CONTROL (STROBE, MODE[0], SEL[1:0], ADDR[3:0], OEZ)
SCP CONTROL (CLK, DO, DI, ENZ, IRQZ)

DMD_RSTZ

3.3V

From Slave ASIC
- 1.7V~5.4V

From Master ASIC

DMD Power Supplies

U7

U8
0.5 TRP S410 DMD

PAGE 3

PAGE 4

PAGE 5 & 6
Note: Only install one 10 Ohm pull-up resistor on DNL_DDR. If DNL_DDR pull-up is installed on Main board side, do not install R3.

Note: R4 and C5 are specific values selected to delay A3115 and DNL_DDR to allow the SMU enough time to turn properly. Recommended installing values as shown.

Note: Do not install R3 if there’s a pull-up on the SCP_DMD_CSZ signal on the Main board.
Power Down Circuitry

18.0V
-14.0V
10.0V

11V protection diode

Do Not Install. Used to Adjust Vreset Rise Time

DMD Power Supplies
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