DID: When using internal VREG, place one 1.2 µF capacitor between each VDD pin and ground. Higher value capacitors may be used.
VDDIO: Digital I/O and Flash Power Pin. Single supply source when VREG is enabled. Place a 0.1 µF decoupling capacitor on each pin.
VDDA: Analog Power Pin. Tie with a 2.2 µF (Capacitor5 typical) closer to the pin.

X-TAL OSCILLATOR

DIP-SWITCH CONFIGURATION

PMIC DIAG

2C TESTPOINTS

ENCODER TESTPOINTS

REVERSE
DIGITAL & ANALOG DECOUPLING FILTER

EXCITER BOOST DC-DC VIN SELECTOR

MONITOR AFE

X-TAL OSCILLATOR

NOTE: This block is inspired by t.com/TOOL/TIDA-00796
More component optimized version. Symbol is different
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