mmWave Cascade Radar RF Board

Cascade Radar RF System Diagram

Cascade Radar Evaluation Kit Diagram

Engineer: [Name]

Sheet: 1 of 6

Designed for: Public Release

Assembly Variant: 001

Mod. Date: 11/28/2018

Size: 19 1/8 x 19 1/8

Copyright © 2018 Texas Instruments

Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not provide technical support for the software products described in this specification. The software products described in this specification are provided "as is" without warranty of any kind, and Texas Instruments specifically disclaims warranties of merchantability, fitness for a particular purpose, and non-infringement. Texas Instruments will not be liable for any claims or damages arising from or related to the software products described in this specification or the use of such software products.
**Cascade RF System Power**

**PMIC #1 - Master 12XX_1 and Slave 12XX_4**

**LC Filtering, Ferrite Filtering 12XX_1 and 12XX_4**

**3.3V System LDO**

**XWR1243 Cascade System Power Diagram**

**XWR1243 Cascade System Power Sequence Diagram**
System 3.3V Supply

TPS73733-Q1 5.0V to 3.3V LDO - System 3.3V Power

REPLACE WITH higher current TPS73733-Q1
Host to RF Board Connectors

SOP Mode / Functional Mode Signals

Safety Error Signals

12XX and PMIC2 J3C Signals

Note: Both functional mode and SOP mode of these signals are always active when RF event occurs.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.

Waves on these signals are intended to be driven from the input pin. The assertion of these waves is required for proper operation.
Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. You should completely validate and test your design implementation to confirm the system functionality for your application.
References

Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not
Drawn By: TID #: N/A

References
- POAR01V00RF104
- POAR01V00RF204
- POAR01V804

Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments 2018
XWR1243 Pull-Up and Pull-Down Resistors

PULL-UP OPTIONS

PULL DOWN OPTIONS
XWR1243 Pull-Up and Pull-Down Resistors

PULL-UP OPTIONS

PULL DOWN OPTIONS
XWR1243 Pull-Up and Pull-Down Resistors

PULL-UP OPTIONS

PULL DOWN OPTIONS

http://www.ti.com

Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

Contact: http://www.ti.com/mmwave

© Texas Instruments 2018

Designed for: Public Release

Assembly Variant: 001

Not in version control

SVN Rev:

PROC054C_PULL_UP_DOWN_1.SchDoc

Sheet Title: Sheet: of

Drawn By:

Engineer:
a0271760

http://www.ti.com
XWR1243 Pull-Up and Pull-Down Resistors

PULL-UP OPTIONS

PULL DOWN OPTIONS
Test Headers, Connectors and Terminations

Oscillator Clock Output Header

Unused 20GHz LO Output Termination

20GHz LO Test Output
## Cascade Radar RF Board - Revision History

<table>
<thead>
<tr>
<th>Rev</th>
<th>Date</th>
<th>Reason</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>11/28/2018</td>
<td>Changed GPIO2 and PGOOD</td>
<td>Added ESD danger logo</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>11/28/2018</td>
<td>Changed XWR reset circuit</td>
<td>Replaced XWR reset generation circuit with discrete AND gate</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>11/28/2018</td>
<td>Changed series terminations on LMK00804B output with 43 ohm resistors per LMK00804B datasheet</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>11/28/2018</td>
<td>Changed R136, R140 FMCW LO power divider resistor to RF resistor CH02016-100RJFT</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>11/28/2018</td>
<td>Changed 12XX_2_1V8_FILT and 12XX_3_1V8_FILT into 12XX_23_1V8_FILT</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This also removed a few power net segments which will now be fed directly from PMIC output</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Removed: C21, C29, C78, C86</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Combined 12XX_2_1V8_FILT and 12XX_3_1V8_FILT into 12XX_23_1V8_FILT</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Combined 12XX_1_1V8_FILT and 12XX_4_1V8_FILT into 12XX_14_1V8_FILT</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This also removed a few power net segments which will now be fed directly from PMIC output</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Removed: C21, C29, C78, C86</td>
</tr>
</tbody>
</table>

---

**Notes**

- Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
- Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not assume any liability for errors or omissions.

**Engineer:**

[Contact information]

**Drawn By:**

[Contact information]

**Orderable:** NOT ORDERABLE

**File:**

PROC054C_Revision_History.SchDoc

**Assembly Variant:** 001

**Mod. Date:** 11/28/2018

**Sheet:** of 11/28/2018
IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated