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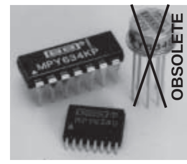


MPY634

SBFS017A – DECEMBER 1995 – REVISED DECEMBER 2004

Wide Bandwidth PRECISION ANALOG MULTIPLIER

FEATURES

- WIDE BANDWIDTH: 10MHz typ
- ±0.5% MAX FOUR-QUADRANT ACCURACY
- INTERNAL WIDE-BANDWIDTH OP AMP
- EASY TO USE
- LOW COST

APPLICATIONS

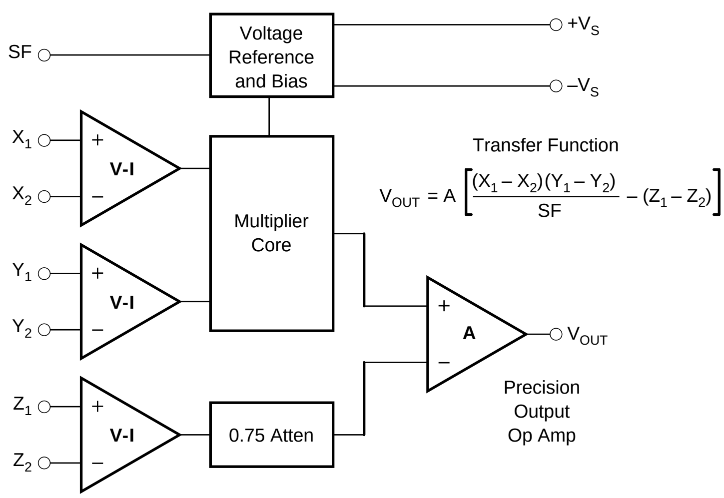
- PRECISION ANALOG SIGNAL PROCESSING
- MODULATION AND DEMODULATION
- VOLTAGE-CONTROLLED AMPLIFIERS
- VIDEO SIGNAL PROCESSING
- VOLTAGE-CONTROLLED FILTERS AND OSCILLATORS

DESCRIPTION

The MPY634 is a wide bandwidth, high accuracy, four-quadrant analog multiplier. Its accurately laser-trimmed multiplier characteristics make it easy to use in a wide variety of applications with a minimum of external parts, often eliminating all external trimming. Its differential X, Y, and Z inputs allow configuration as a multiplier, squarer, divider, square-rooter, and other functions while maintaining high accuracy.

The wide bandwidth of this new design allows signal processing at IF, RF, and video frequencies. The internal output amplifier of the MPY634 reduces design complexity compared to other high frequency multipliers and balanced modulator circuits. It is capable of performing frequency mixing, balanced modulation, and demodulation with excellent carrier rejection.

An accurate internal voltage reference provides precise setting of the scale factor. The differential Z input allows user-selected scale factors from 0.1 to 10 using external feedback resistors.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SPECIFICATIONS

ELECTRICAL

At $T_A = +25°C$ and $V_S = \pm15VDC$, unless otherwise noted.

MODEL	MPY634KP/KU			MPY634AM OBSOLETE			MPY634BM OBSOLETE			MPY634SM OBSOLETE			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
MULTIPLIER PERFORMANCE													
Transfer Function	$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10V} + Z_2$			$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10V} + Z_2$				*			*		
Total Error(1)													
(–10V ≤ X, Y ≤ +10V)			±2.0			±1.0			±0.5			*	%
T_A = min to max		±2.5			±1.5			±1.0				±2.0	%
Total Error vs Temperature		±0.03			±0.022			±0.015				±0.02	%/°C
Scale Factor Error													
(SF = 10.000V Nominal)(2)		±0.25			±0.1			*			*		%
Temperature Coefficient of													
Scaling Voltage		±0.02			±0.01			±0.01			*		%/°C
Supply Rejection (±15V ±1V)		±0.01			±0.01			*			*		%
Nonlinearity													
X (X = 20Vp-p, Y = 10V)		±0.4			±0.4			0.2	±0.3		*		%
Y (Y = 20Vp-p, X = 10V)		±0.01			±0.01			*	±0.1		*		%
Feedthrough(3)													
X (Y Nulled, X = 20Vp-p, 50Hz)		±0.3			±0.3			±0.15	±0.3		*		%
Y (X Nulled, Y = 20Vp-p, 50Hz)		±0.01			±0.01			*	±0.1		*		%
Both Inputs (500kHz, 1Vrms)													
Unnulled	40	50		45	55		*	60		*	*		dB
Nulled	55	60		55	65		60	70		*	*		dB
Output Offset Voltage		±50	±100		±5	±30		*	±15		*	*	mV
Output Offset Voltage Drift		*			±200			±100			*	±500	µV/°C
DYNAMICS													
Small Signal BW,													
(V_{OUT} = 0.1Vrms)	6	10		8	10		*	*		6	*		MHz
1% Amplitude Error													
(C_{LOAD} = 1000pF)		100			100			*			*		kHz
Slew Rate (V_{OUT} = 20Vp-p)		20			20			*			*		V/µs
Settling Time													
(to 1%, ΔV_{OUT} = 20V)		2			2			*			*		µs
NOISE													
Noise Spectral Density:													
SF = 10V		0.8			0.8			*			*		$\mu V/\sqrt{Hz}$
Wideband Noise:													
f = 10Hz to 5MHz		1			1			*			*		mVrms
f = 10Hz to 10kHz		90			90			*			*		µVrms
OUTPUT													
Output Voltage Swing	±11			±11			*			*			V
Output Impedance (f ≤ 1kHz)		0.1			0.1			*			*		Ω
Output Short Circuit Current													
(R_L = 0, T_A = min to max)		30			30			*			*		mA
Amplifier Open Loop Gain													
(f = 50Hz)		85			85			*			*		dB
INPUT AMPLIFIERS (X, Y and Z)													
Input Voltage Range													
Differential V_{IN} (V_{CM} = 0)		±12			±12			*			*		V
Common-Mode V_{IN} (V_{DIFF} = 0)		±10			±10			*			*		V
(see Typical Performance Curves)													
Offset Voltage X, Y		±25	±100		±5	±20		±2	±10		*	*	mV
Offset Voltage Drift X, Y		200			100			50			*		µV/°C
Offset Voltage Z		±25	±100		±5	±30		±2	±15		*	*	mV
Offset Voltage Drift Z		200			200			100				500	µV/°C
CMRR	60	80		60	80		70	90		*	*		dB
Bias Current		0.8	2.0		0.8	2.0		*	*		*	*	µA
Offset Current		0.1			0.1			*			*	2.0	µA
Differential Resistance		10			10			*			*		MΩ
DIVIDER PERFORMANCE													
Transfer Function ($X_1 > X_2$)	$10V\frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$			$10V\frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$				*			*		
Total Error(1) untrimmed													
(X = 10V, –10V ≤ Z ≤ +10V)		1.5			±0.75			±0.35			±0.75		%
(X = 1V, –1V ≤ Z ≤ +1V)		4.0			±2.0			±1.0			*		%
(0.1V≤ X ≤ 10V, –10V ≤ Z ≤ 10V)		5.0			±2.5			±1.0			*		%
SQUARE PERFORMANCE													
Transfer Function	$\frac{(X_1 - X_2)^2}{10V} + Z_2$			$\frac{(X_1 - X_2)^2}{10V} + Z_2$				*			*		
Total Error (–10V ≤ X ≤ 10V)		±1.2			±0.6			±0.3			*		%

SPECIFICATIONS (CONT)

ELECTRICAL

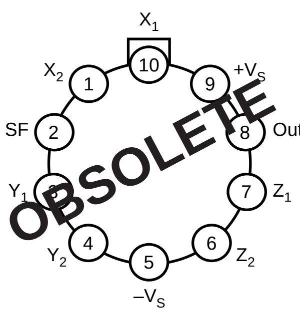
At T_A = +25°C and V_S = ±15VDC, unless otherwise noted.

	MPY634KP/KU			MPY634AM OBSOLETE			MPY634BM OBSOLETE			MPY634SM OBSOLETE			
MODEL	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
SQUARE-ROOTER PERFORMANCE													
Transfer Function ($Z_1 \le Z_2$)		$\sqrt{10V (Z_2 - Z_1)} + X_2$			$\sqrt{10V (Z_2 - Z_1)} + X_2$			*			*		
Total Error(1) (1V ≤ Z ≤ 10V)		±2.0			±1.0			±0.5			*		%
POWER SUPPLY													
Supply Voltage:													
Rated Performance		±15			±15			*			*		VDC
Operating	±8		±18	±8		±18	*		*	*		±20	VDC
Supply Current, Quiescent		4	6		4	6		*	*		*	*	mA
TEMPERATURE RANGE													
Specification	–40		+85	–25		+85	*		*	–55		+125	°C
Storage	–40		+85	–65		+150	*		*	*		*	°C

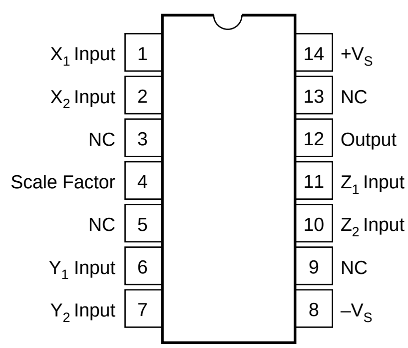
* Specification same as for MPY634AM.
Gray indicates obsolete parts.
NOTES: (1) Figures given are percent of full scale, ±10V (i.e., 0.01% = 1mV). (2) May be reduced to 3V using external resistor between $-V_S$ and SF. (3) Irreducible component due to nonlinearity; excludes effect of offsets.

PIN CONFIGURATIONS

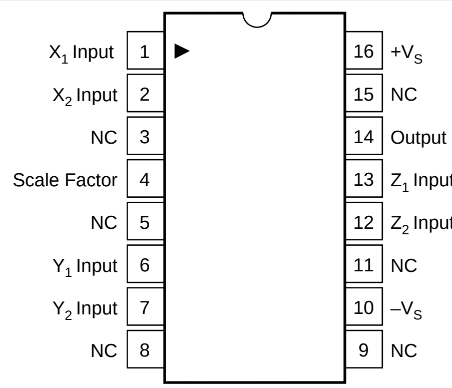
Top View



TO-100: MPY634AM/BM/SM



DIP: MPY634KP



SOIC: MPY634KU

ABSOLUTE MAXIMUM RATINGS

PARAMETER	MPY634AM/BM OBSOLETE	MPY634KP/KU	MPY634SM OBSOLETE
Power Supply Voltage	±18	*	±20
Power Dissipation	500mW	*	*
Output Short-Circuit to Ground	Indefinite	*	*
Input Voltage (all X, Y and Z)	$\pm V_S$	*	*
Temperature Range:			
Operating	–25°C/+85°C	–40°C/+85°C	–55°C/+125°C
Storage	–65°C/+150°C	–40°C/+85°C	*
Lead Temperature (soldering, 10s)	+300°C	*	*
SOIC 'KU' Package		+260°C	

* Specification same as for MPY634AM/BM.
NOTE: Gray indicates obsolete parts.

ORDERING INFORMATION

MPY634 ( ) ( )

Basic Model Number
Performance Grade(1)
K: U: –40°C to +85°C
Package Code
P: Plastic 14-pin DIP
U: 16-pin SOIC

NOTE: (1) Performance grade identifier may not be marked on the SOIC package; a blank denotes "K" grade.

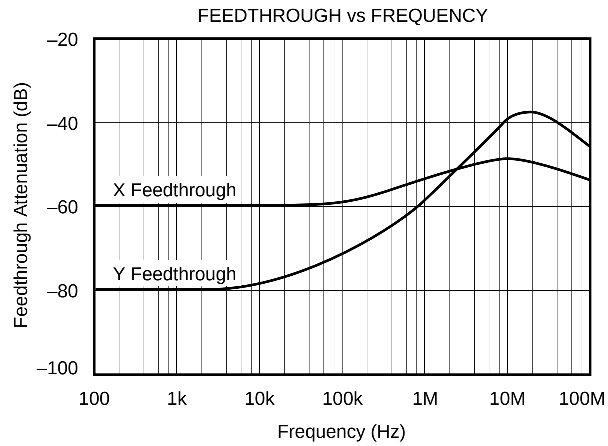
PACKAGE INFORMATION(1)

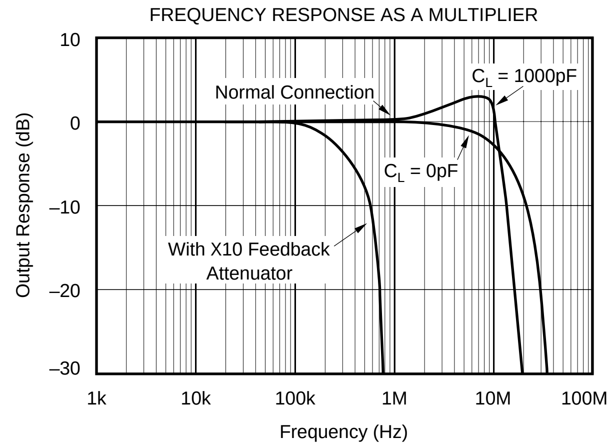
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER
MPY634KP	14-Pin PDIP	010
MPY634KU	16-Pin SOIC	211

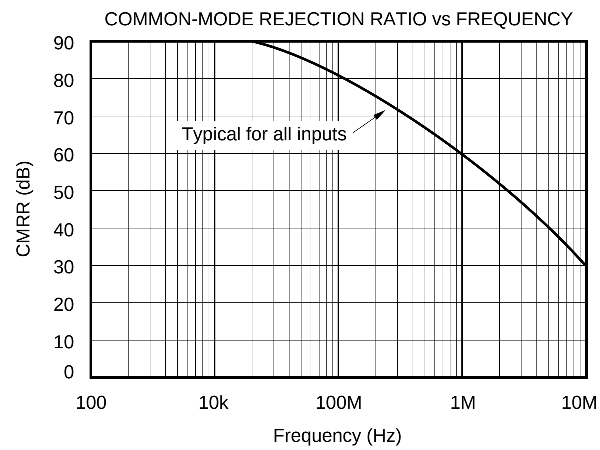
NOTE: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

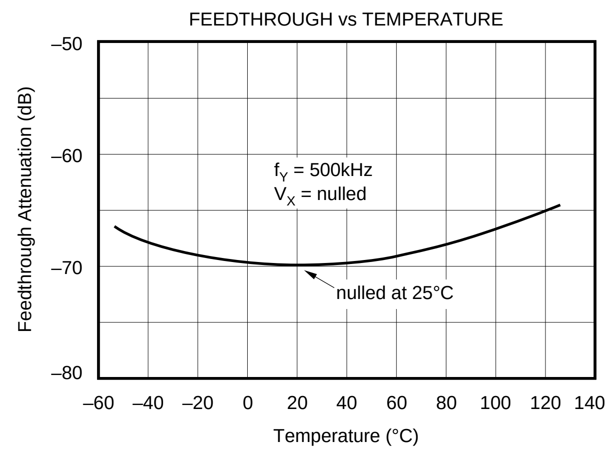
TYPICAL PERFORMANCE CURVES

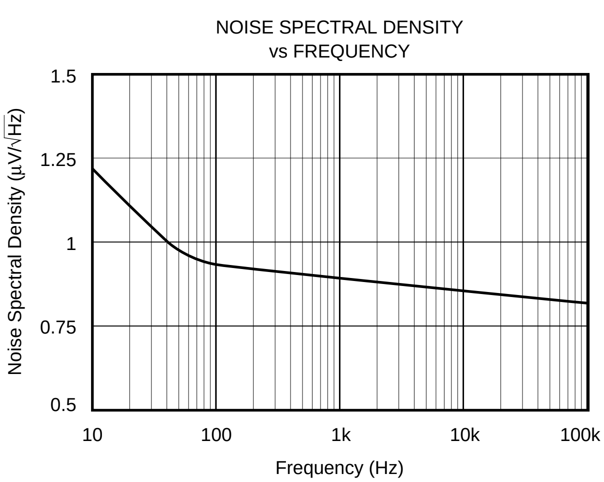
At T_A = +25°C, V_S = ±15VDC, unless otherwise noted.

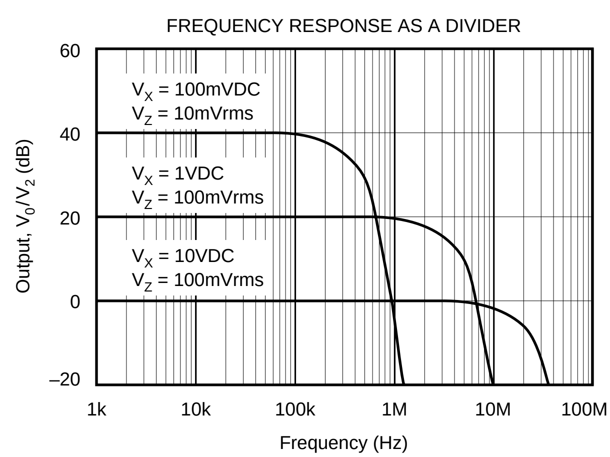






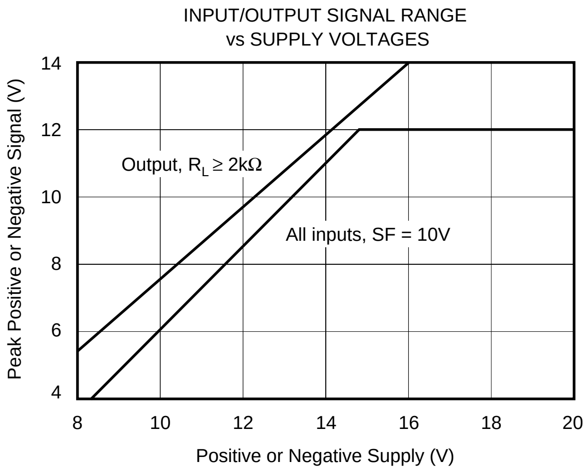


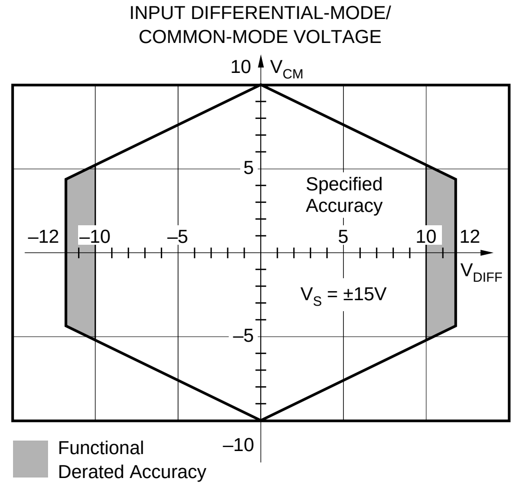


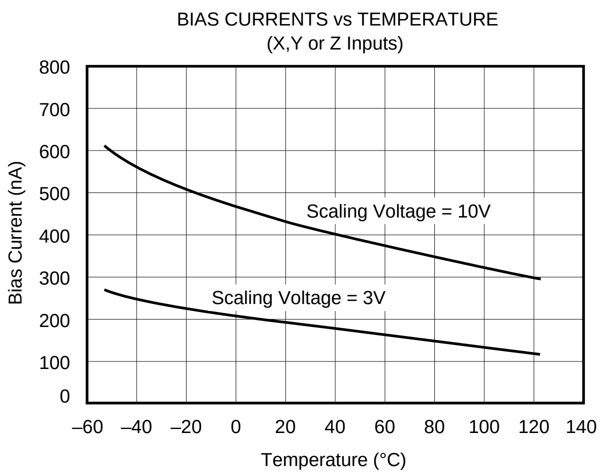


TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15VDC, unless otherwise noted.







THEORY OF OPERATION

The transfer function for the MPY634 is:

$$V_{OUT} = A\left[\frac{(X_1 - X_2)(Y_1 - Y_2)}{SF} - (Z_1 - Z_2)\right]$$

where:

A = open-loop gain of the output amplifier (typically 85dB at DC).

SF = Scale Factor. Laser-trimmed to 10V but adjustable over a 3V to 10V range using external resistors.

X, Y, Z are input voltages. Full-scale input voltage is equal to the selected SF. (Max input voltage = ±1.25 SF).

An intuitive understanding of transfer function can be gained by analogy to the op amp. By assuming that the open-loop gain, A, of the output operational amplifier is infinite, inspection of the transfer function reveals that any V_{OUT} can be created with an infinitesimally small quantity within the brackets. Then, an application circuit can be analyzed by assigning circuit voltages for all X, Y and Z inputs and setting the bracketed quantity equal to zero. For example, the basic multiplier connection in Figure 1, $Z_1 = V_{OUT}$ and $Z_2 = 0$. The quantity within the brackets then reduces to:

$$\frac{(X_1 - X_2)(Y_1 - Y_2)}{SF} - (V_{OUT} - 0) = 0$$

This approach leads to a simple relationship which can be solved for V_{OUT} to provide the closed-loop transfer function.

The scale factor is accurately factory adjusted to 10V and is typically accurate to within 0.1% or less. The scale factor may be adjusted by connecting a resistor or potentiometer between pin SF and the $-V_S$ power supply. The value of the external resistor can be approximated by:

$$R_{SF} = 5.4k\Omega\left(\frac{SF}{10 - SF}\right)$$

Internal device tolerances make this relationship accurate to within approximately 25%. Some applications can benefit from reduction of the SF by this technique. The reduced input bias current, noise, and drift achieved by this technique can be likened to operating the input circuitry in a higher gain, thus reducing output contributions to these effects. Adjustment of the scale factor does not affect bandwidth.

The MPY634 is fully characterized at V_S = ±15V but operation is possible down to ±8V with an attendant reduction of input and output range capability. Operation at voltages greater than ±15V allows greater output swing to be achieved by using an output feedback attenuator (Figure 1).

As with any wide bandwidth circuit, the power supplies should be bypassed with high frequency ceramic capacitors. These capacitors should be located as near as practical to the power supply connections of the MPY634. Improper bypassing can lead to instability, overshoot, and ringing in the output.

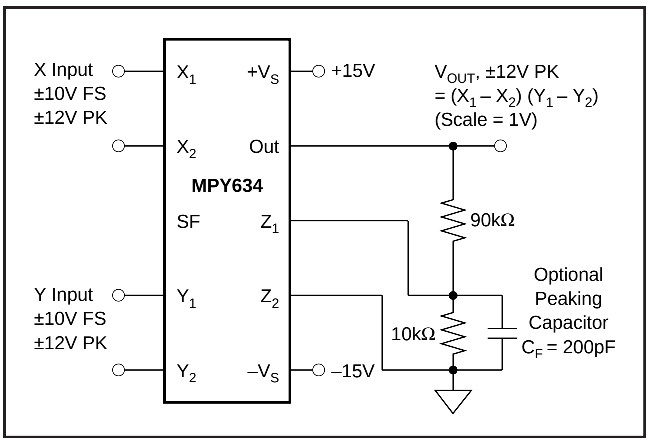


FIGURE 1. Connections for Scale-Factor of Unity.

BASIC MULTIPLIER CONNECTION

Figure 2 shows the basic connection as a multiplier. Accuracy is fully specified without any additional user-trimming circuitry. Some applications can benefit from trimming of one or more of the inputs. The fully differential inputs facilitate referencing the input quantities to the source voltage common terminal for maximum accuracy. They also allow use of simple offset voltage trimming circuitry as shown on the X input.

The differential Z input allows an offset to be summed in V_{OUT}. In basic multiplier operation, the Z_2 input serves as the output voltage ground reference and should be connected to the ground of the driven system for maximum accuracy.

A method of changing (lowering) SF by connecting to the SF pin was discussed previously. Figure 1 shows an alternative method of changing the effective SF of the overall circuit by using an attenuator in the feedback connection to Z_1. This method puts the output amplifier in a higher gain and is thus accompanied by a reduction in bandwidth and an

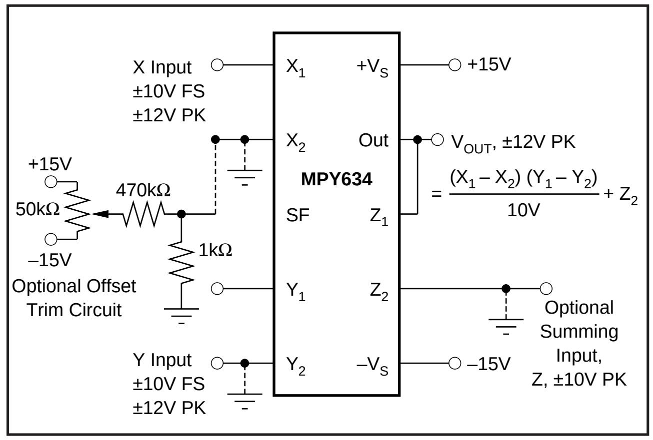


FIGURE 2. Basic Multiplier Connection.

increase in output offset voltage. The larger output offset may be reduced by applying a trimming voltage to the high impedance input, Z_2.

The flexibility of the differential Z inputs allows direct conversion of the output quantity to a current. Figure 3 shows the output voltage differentially-sensed across a series resistor forcing an output-controlled current. Addition of a capacitor load then creates a time integration function useful in a variety of applications such as power computation.

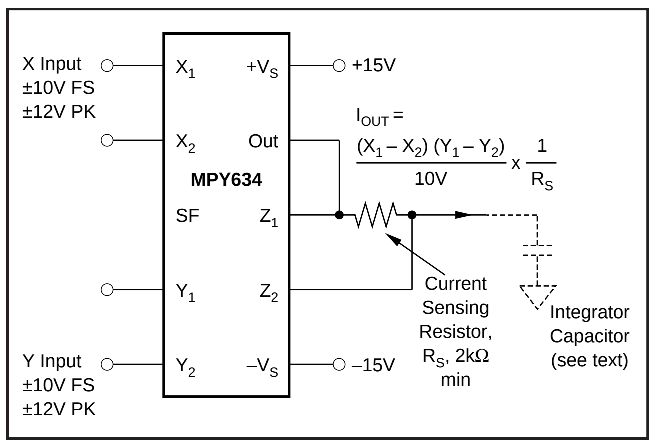


FIGURE 3. Conversion of Output to Current.

SQUARER CIRCUIT (FREQUENCY DOUBLER)

Squarer, or frequency doubler, operation is achieved by paralleling the X and Y inputs of the standard multiplier circuit. Inverted output can be achieved by reversing the differential input terminals of either the X or Y input. Accuracy in the squaring mode is typically a factor of two better than the specified multiplier mode with maximum error occurring with small (less than 1V) inputs. Better accuracy can be achieved for small input voltage levels by reducing the scale factor, SF.

DIVIDER OPERATION

The MPY634 can be configured as a divider as shown in Figure 4. High impedance differential inputs for the numerator and denominator are achieved at the Z and X inputs, respectively. Feedback is applied to the Y_2 input, and Y_1 is normally referenced to output ground. Alternatively, as the transfer function implies, an input applied to Y_1 can be summed directly into V_{OUT}. Since the feedback connection is made to a multiplying input, the effective gain of the output op amp varies as a function of the denominator input voltage. Therefore, the bandwidth of the divider function is proportional to the denominator voltage (see Typical Performance Curves).

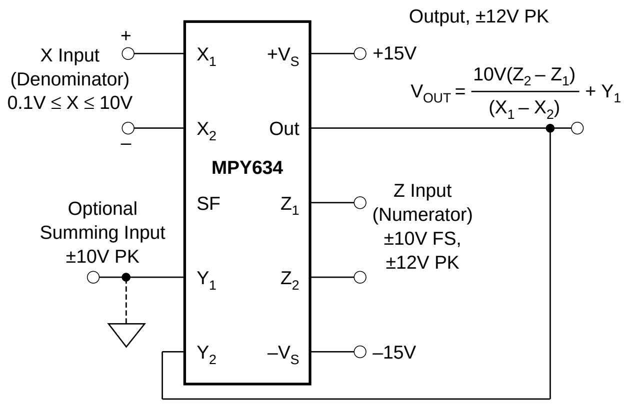


FIGURE 4. Basic Divider Connection.

Accuracy of the divider mode typically ranges from 1.0% to 2.5% for a 10 to 1 denominator range depending on device grade. Accuracy is primarily limited by input offset voltages and can be significantly improved by trimming the offset of the X input. A trim voltage of ±3.5mV applied to the "low side" X input (X_2 for positive input voltages on X_1) can produce similar accuracies over 100 to 1 denominator range. To trim, apply a signal which varies from 100mV to 10V at a low frequency (less than 500Hz). An offset sine wave or ramp is suitable. Since the ratio of the quantities should be constant, the ideal output would be a constant 10V. Using AC coupling on an oscilloscope, adjust the offset control for minimum output voltage variation.

SQUARE-ROOTER

A square-rooter connection is shown in Figure 5. Input voltage is limited to one polarity (positive for the connection shown). The diode prevents circuit latch-up should the input go negative. The circuit can be configured for negative input and positive output by reversing the polarity of both the X and Y inputs. The output polarity can be reversed by reversing the diode and X input polarity. A load resistance of approximately 10kΩ must be provided. Trimming for improved accuracy would be accomplished at the Z input.

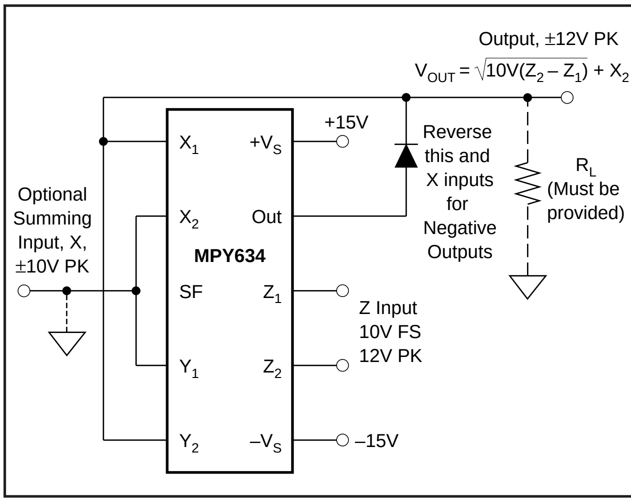
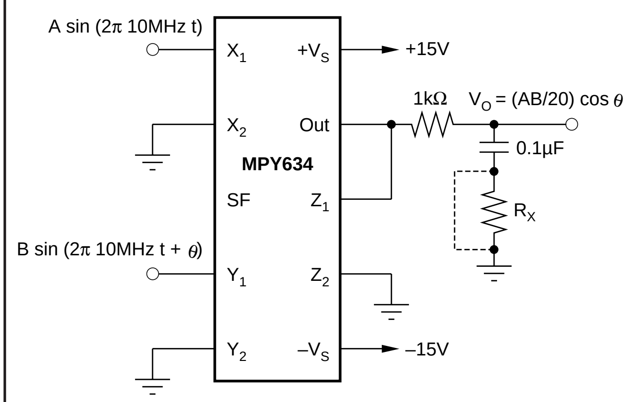


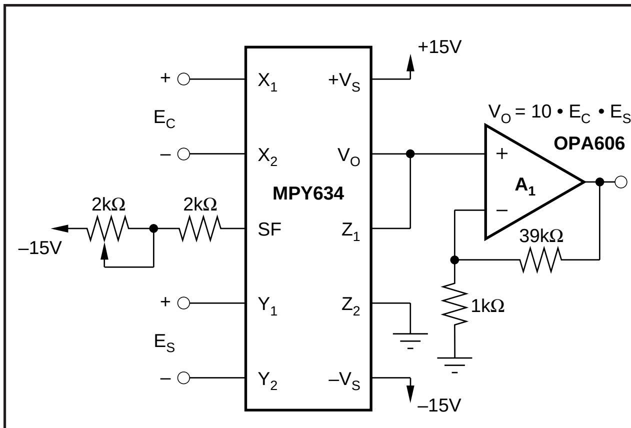
FIGURE 5. Square-Rooter Connection.

APPLICATIONS



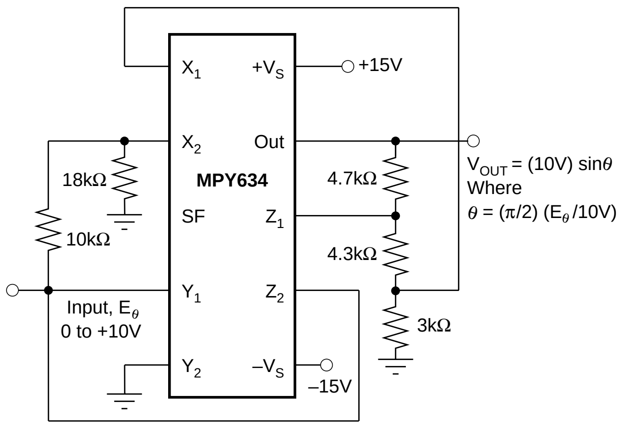
Multiplier connection followed by a low-pass filter forms phase detector useful in phase-locked-loop circuitry. R_X is often used in PLL circuitry to provide desired loop-damping characteristics.

FIGURE 6. Phase Detector.



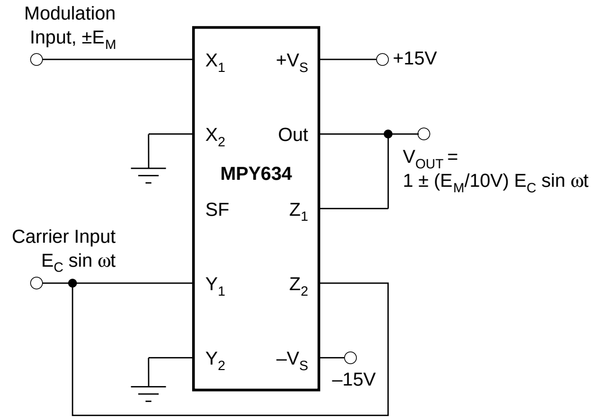
Minor gain adjustments are accomplished with the 1kΩ variable resistor connected to the scale factor adjustment pin, SF. Bandwidth of this circuit is limited by A_1, which is operated at relatively high gain.

FIGURE 7. Voltage-Controlled Amplifier.



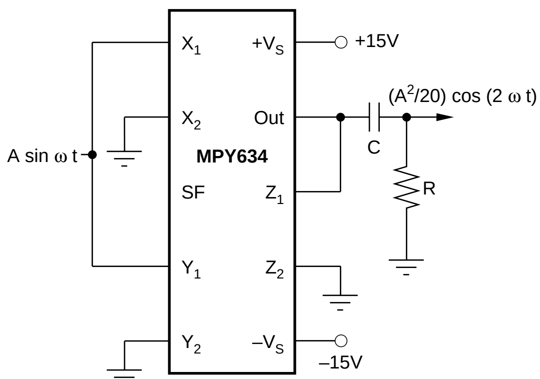
With a linearly changing 0-10V input, this circuit's output follows 0° to 90° of a sine function with a 10V peak output amplitude.

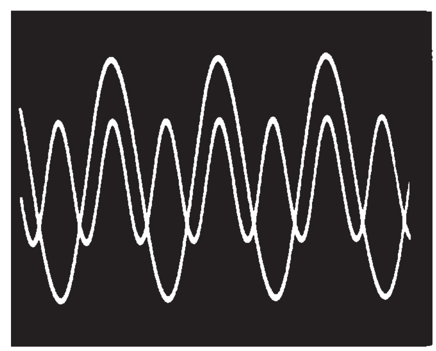
FIGURE 8. Sine-Function Generator.



By injecting the input carrier signal into the output through connection to the Z_2 input, conventional amplitude modulation is achieved. Amplification can be achieved by use of the SF pin, or Z attenuator (at the expense of bandwidth).

FIGURE 9. Linear AM Modulator.



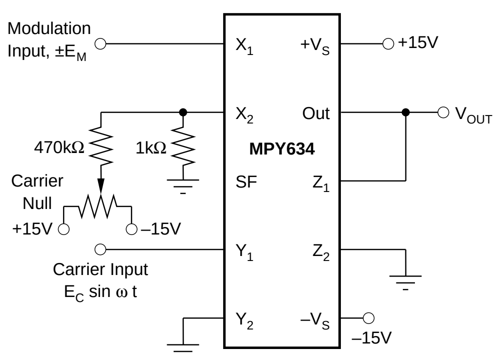


Squaring a sinusoidal input creates an output frequency of twice that of the input. The DC output component is removed by AC-coupling the output.

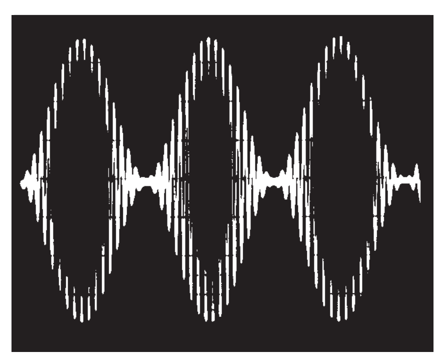
Frequency Doubler

Input Signal: 20Vp-p, 200kHz
Output Signal: 10Vp-p, 400kHz

FIGURE 10. Frequency Doubler.



The basic muliplier connection performs balanced modulation. Carrier rejection can be improved by trimming the offset voltage of the modulation input. Better carrier rejection above 2MHz is typically achieved by interchanging the X and Y inputs (carrier applied to the X input).



Carrier: f_c = 2MHz, Amplitude = 1Vrms
Signal: f_s = 120kHz, Amplitude = 10V peak

FIGURE 11. Balanced Modulator.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MPY634KP	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type		MPY634KP	Samples
MPY634KU	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	MPY634U	Samples
MPY634KU/1K	ACTIVE	SOIC	DW	16	1000	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	MPY634U	Samples
MPY634KU/1KE4	ACTIVE	SOIC	DW	16	1000	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	MPY634U	Samples
MPY634KUE4	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	MPY634U	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

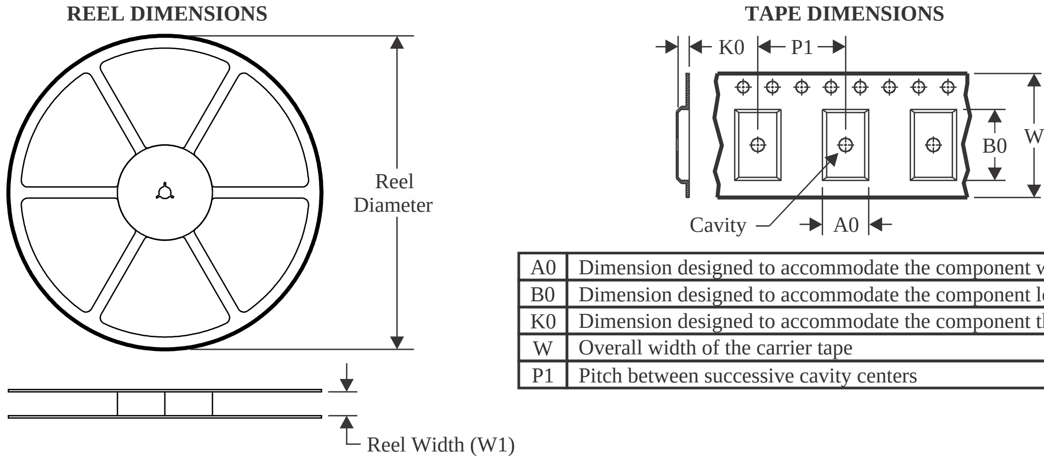
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

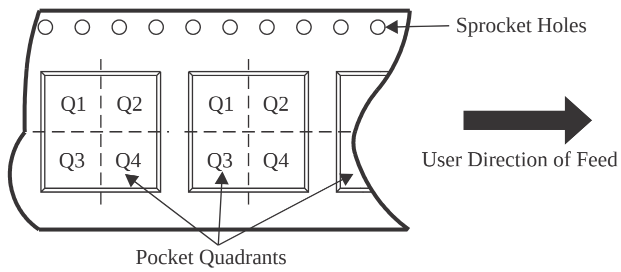
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



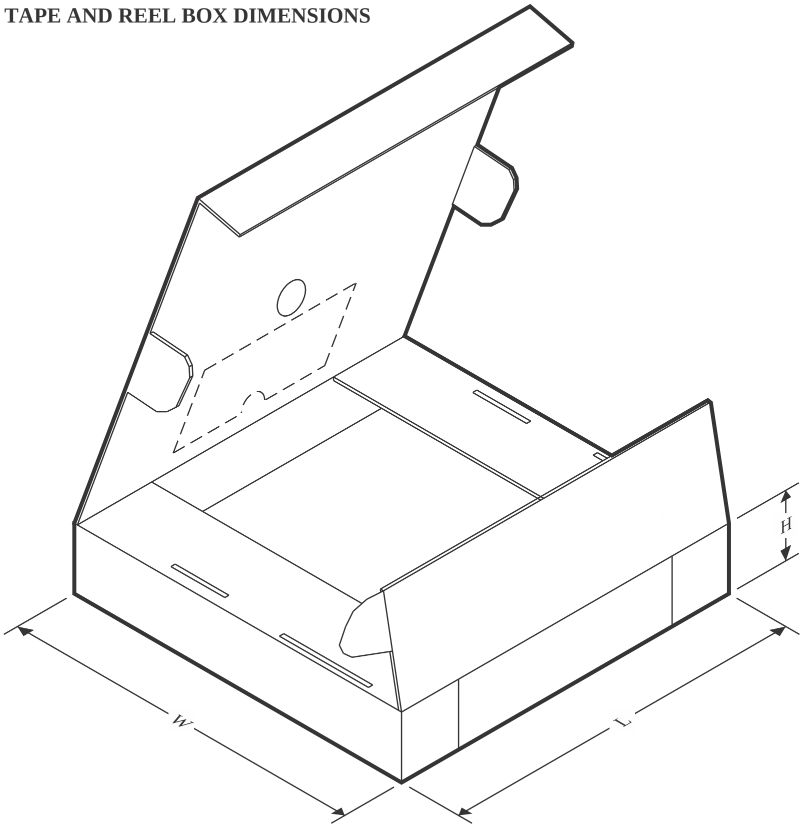
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MPY634KU/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

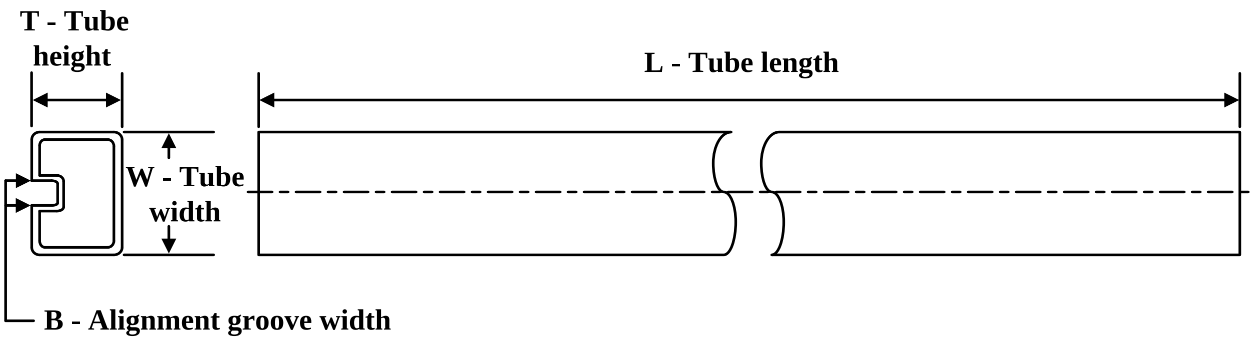
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MPY634KU/1K	SOIC	DW	16	1000	356.0	356.0	35.0

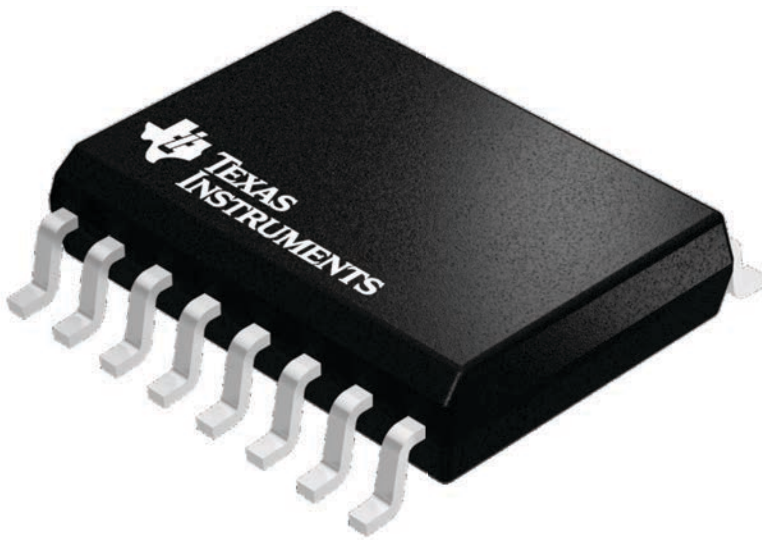
TUBE

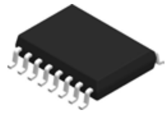


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
MPY634KP	N	PDIP	14	25	506	13.97	11230	4.32
MPY634KU	DW	SOIC	16	40	507	12.83	5080	6.6
MPY634KUE4	DW	SOIC	16	40	507	12.83	5080	6.6

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



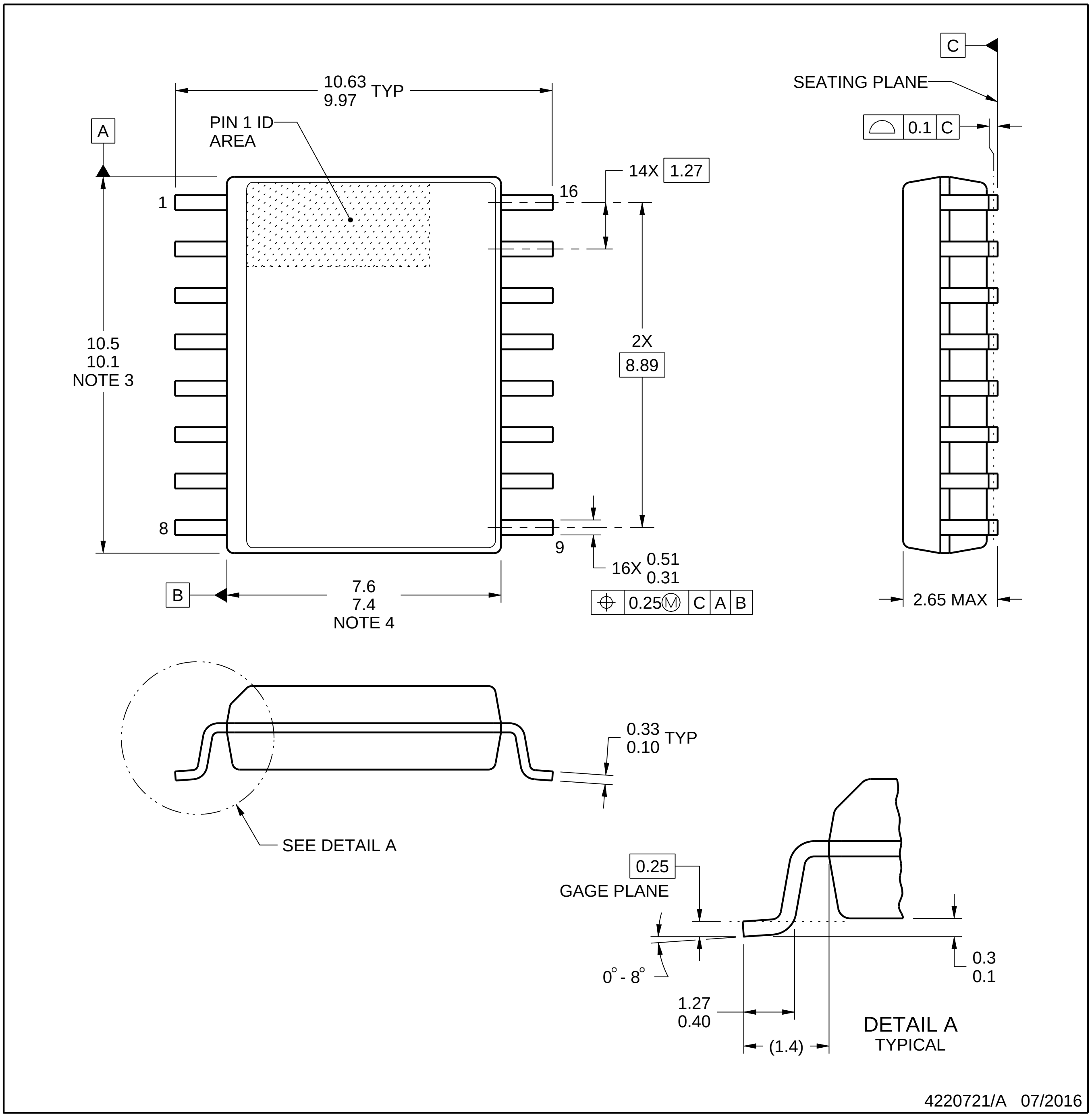


PACKAGE OUTLINE

DW0016A

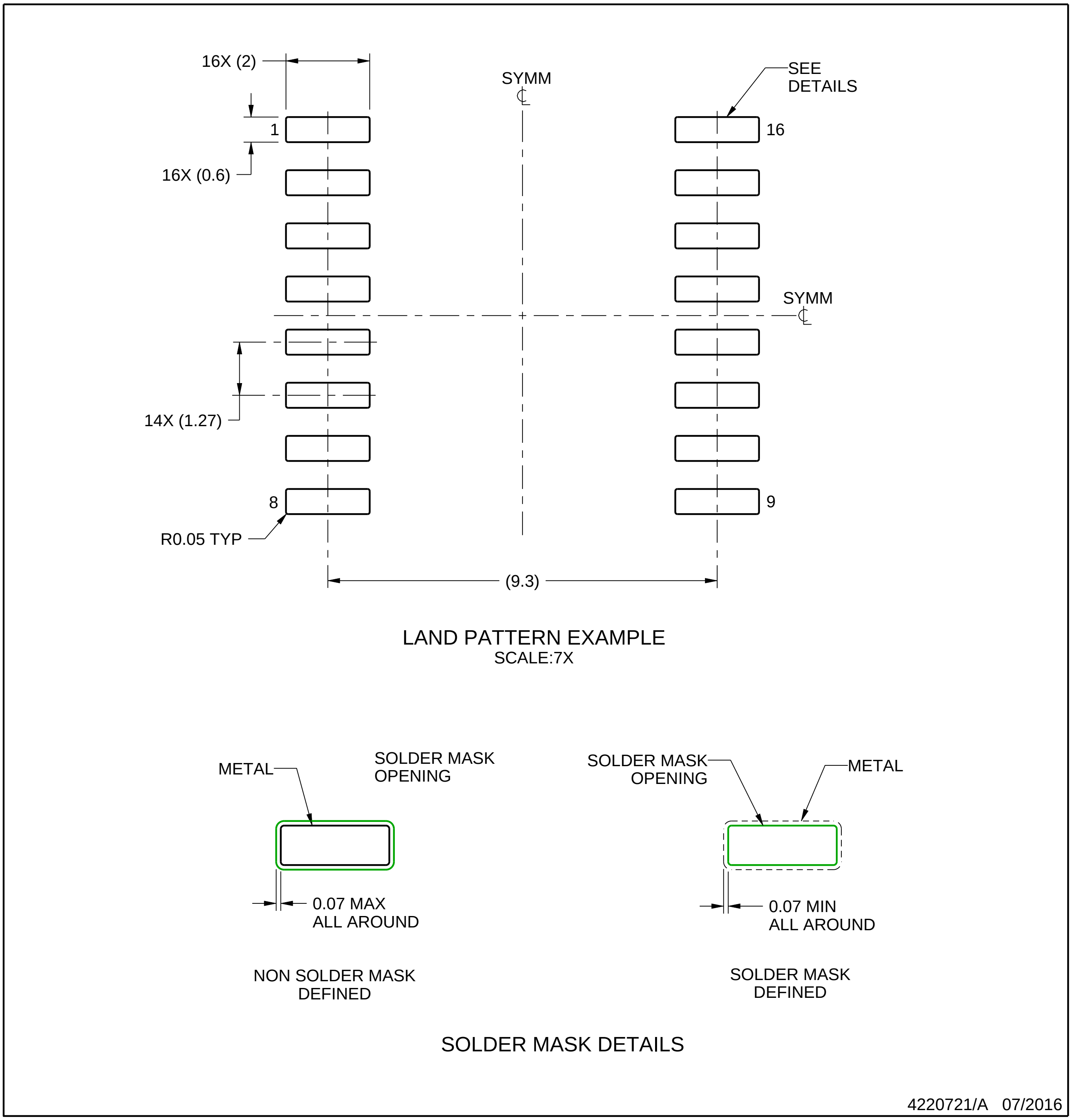
SOIC - 2.65 mm max height

SOIC



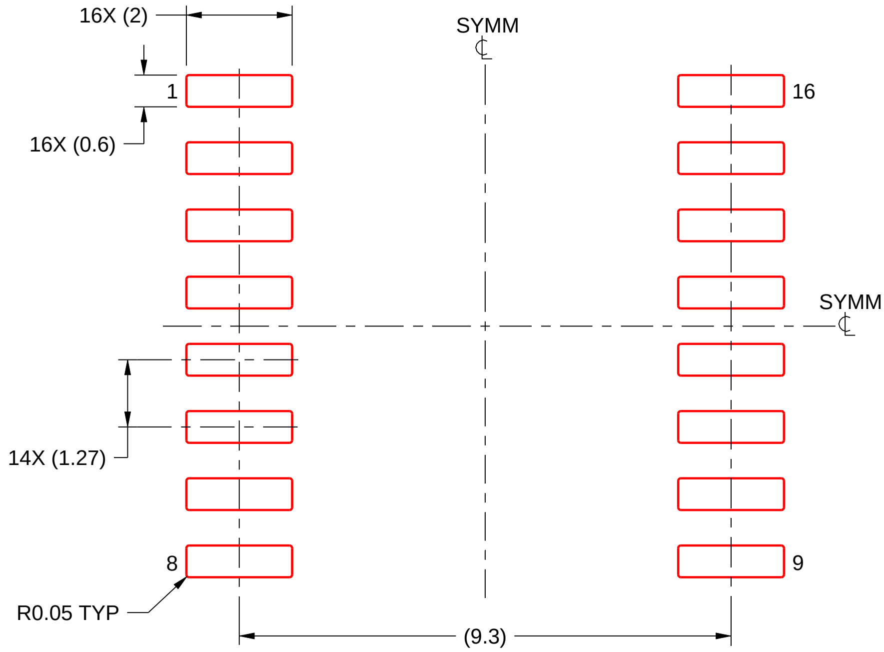
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

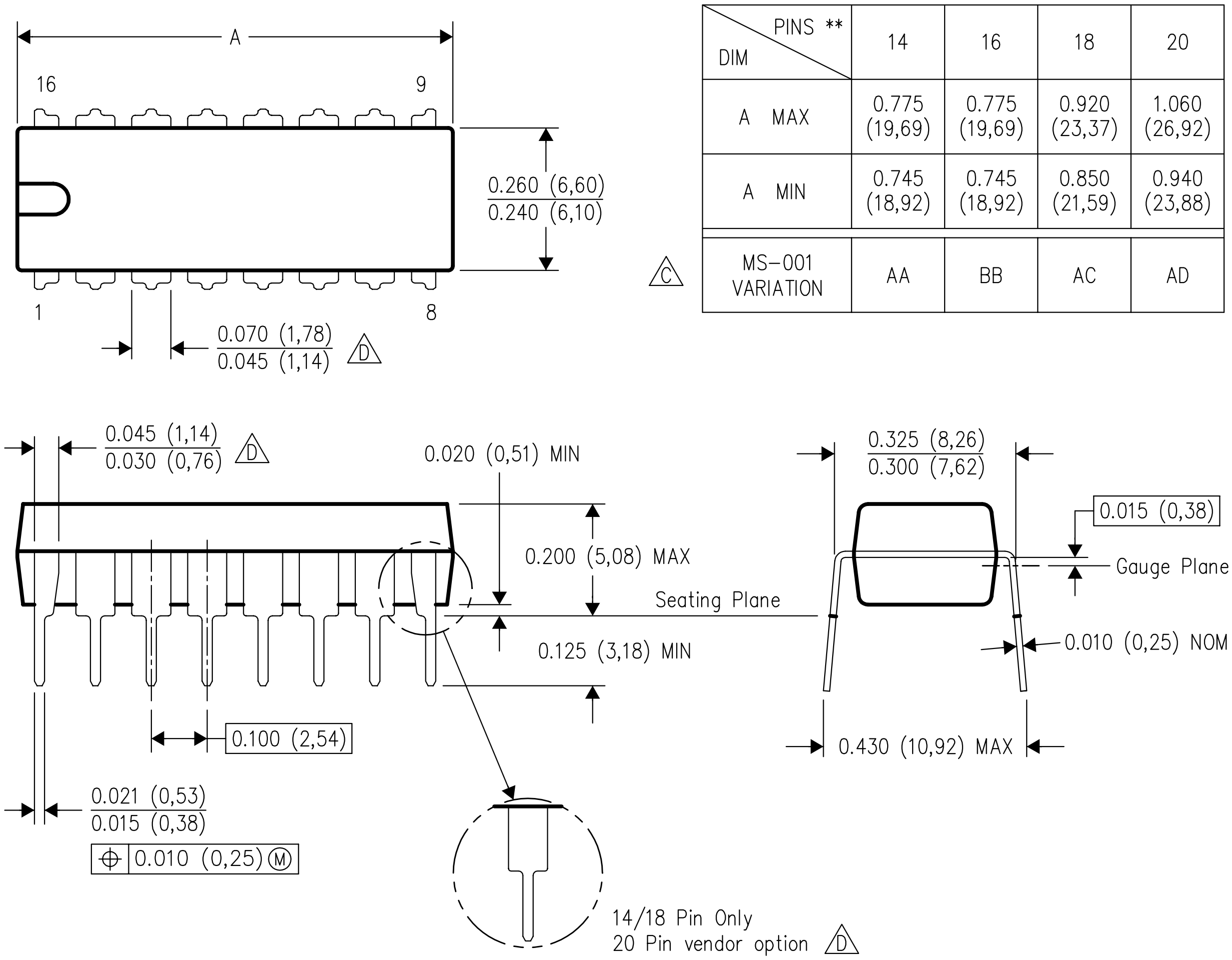
4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION	AA	BB	AC	AD

4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265