Programmable Voltage Source
with Memory

FEATURES

- **10-BIT RESOLUTION**
- **RAIL-TO-RAIL OUTPUT**
- **ONBOARD NONVOLATILE MEMORY**
- **I_{OUT}: 100mA**
- **LOW SUPPLY CURRENT: 900μA**
- **SUPPLY VOLTAGE: 7V to 18V**
- **DIGITAL SUPPLY: 2.0V to 5.5V**
- **INDUSTRY-STANDARD, TWO-WIRE INTERFACE**
- **HIGH ESD RATING:
  2kV HBM, 500V CDM**

APPLICATIONS

- **LCD PANEL V_{COM} CALIBRATION**
- **LCD PANEL BRIGHTNESS AND CONTRAST CONTROL**
- **POTENTIOMETER REPLACEMENT**
- **MOTOR DRIVE**
- **PROGRAMMABLE POWER SUPPLY**
- **PROGRAMMABLE OFFSET ADJUSTMENT**
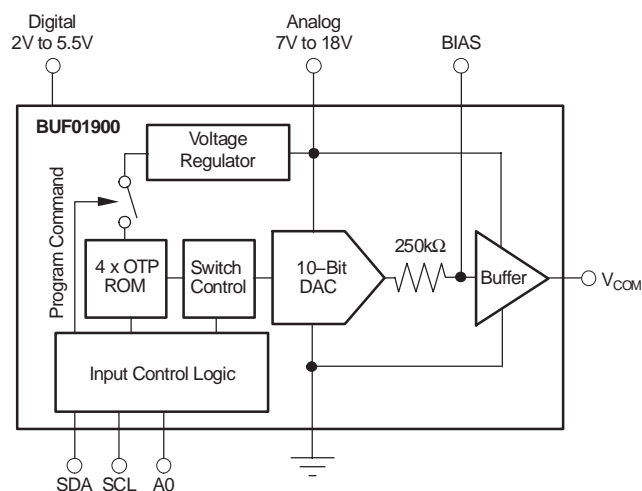- **ACTUATOR CONTROL**

DESCRIPTION

The BUF01900 and BUF01901 provide a programmable voltage output with 10-bit resolution. Programming of the output occurs through an industry-standard, two-wire serial interface. Once the correct V_{COM} voltage is established it can easily be stored into the integrated nonvolatile memory.

An initial output voltage and adjustment range can be set by an external resistor-divider. With its large output current capability (up to 100mA), the BUF01900 and BUF01901 are ideally suited as programmable V_{COM} calibrators in LCD panels.

The BUF01901 has the digital-to-analog converter (DAC) output brought out directly. It has a slightly lower cost than the BUF01900, and works very well with the integrated V_{COM} in traditional gamma buffers such as the BUFxx702, BUFxx703, BUFxx704 and BUF11705.

The BUF01900 and BUF01901 are both available in TSSOP-8 and 3mm x 3mm DFN-10 packages. The DFN-10 package (only 0.9mm in height) is especially well-suited for notebook computers. Both devices are specified from –40°C to +85°C.

BUF01900, BUF01901 RELATED PRODUCTS

FEATURES	PRODUCT
22V High Supply Voltage Gamma Buffers	BUF11705
12--Channel Programmable Buffer, 10-Bit, V_{COM}	BUF12800
20-Channel Programmable Buffer, 10-Bit, V_{COM}	BUF20800
16-Channel Programmable Buffer with Memory	BUF16820
20-Channel Programmable Buffer with Memory	BUF20820

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS INSTRUMENTS
www.ti.com

Copyright © 2006, Texas Instruments Incorporated

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage, V_S . . . . +20V
Supply Voltage, V_{SD} . . . . +6V
Signal Input Terminals,
  BIAS:
    Voltage . . . . –0.5V to V_S +0.5V
  SCL, SDA, A0, A1:
    Voltage . . . . –0.5V to +6V
    Current . . . . ±10mA
Output Short Circuit[2] . . . . Continuous
Operating Temperature . . . . –40°C to +95°C
Storage Temperature . . . . –65°C to +150°C
Junction Temperature . . . . +125°C
ESD Rating:
  Human Body Model (HBM) 2000V
  Charged-Device Model (CDM) 500V

[1] Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

[2] Short-circuit to ground.

ORDERING INFORMATION[1]

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
BUF01900	DFN-10	DRC	BOO
BUF01900	TSSOP-8	PW	F01900
BUF01901	DFN-10	DRC	BOP
BUF01901	TSSOP-8	PW	F01901

[1] For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

PIN CONFIGURATIONS
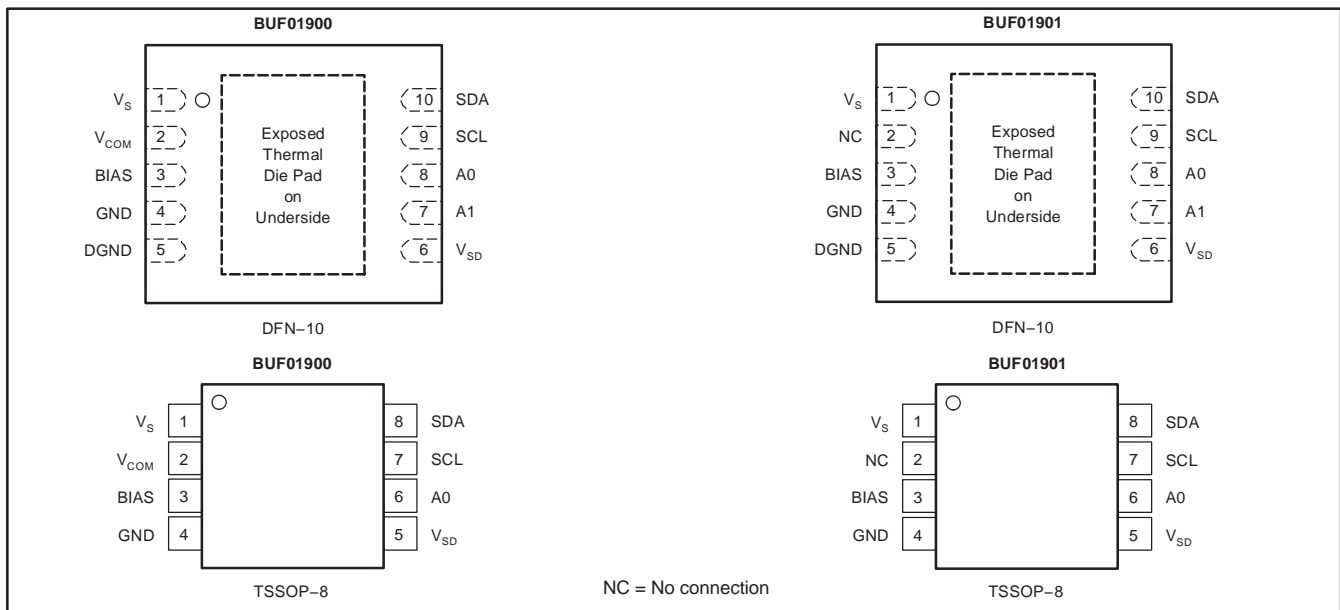
ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range, T_A = –40°C to +85°C.

At T_A = +25°C, V_S = 18V, V_{SD} = 5V, R_L = 1.5kΩ connected to ground, and C_L = 200pF, unless otherwise noted.

PARAMETER		CONDITIONS	BUF01900, BUF01901			UNIT
			MIN	TYP	MAX	
ANALOG						
V_{COM} Output Swing[1]		**Sourcing 10mA, Code 1023**	**17.7**	**17.8**		**V**
		Sinking 10mA, Code 00		**0.6**	**1**	**V**
		Sourcing 100mA, Code 1023	**15**	**16**		**V**
		Sinking 100mA, Code 00		**0.75**	**1**	**V**
V_{COM} Output Reset and Power-Up Value[1]		OTP not programmed, Code 512		$V_S/2$		V
Nominal V_{BIAS} Output Impedance		No Load on V_{BIAS}, V_{COM}		250		kΩ
Program to Out Delay	t_D			5		µs
Output Accuracy		$1V < V_{COM} < 17.7$		20	50	mV
Load Regulation	REG	$V_{OUT} = V_S/2$, I_{OUT} = +50mA to –50mA Step		0.5	1.5	mV/mA
V_{COM}[1]						
Offset				±5	±25	mV
Offset Drift		–25°C to +100°C		5		µV/°C
Common-Mode Range				0.8 to 18		V
Common-Mode Rejection	CMR	$0.8V < V_{IN} < 17.9V$		85		dB
Slew Rate				5		V/µs
V_{BIAS}		No Load on V_{BIAS}				
Integral Nonlinearity	INL			0.1	2	LSB
Differential Nonlinearity	DNL			0.1	2	LSB
Gain Error				0.1	1	%FSC
Accuracy				20	50	mV
ANALOG POWER SUPPLY						
Operating Range[2]	V_S		7		18	V
Total Analog Supply Current	I_S	Output at Reset Values, No Load		0.9	1.5	mA
over Temperature					**1.5**	**mA**
DIGITAL						
Logic 1 Input Voltage	V_{IH}		$0.7 \times V_{SD}$			V
Logic 0 Input Voltage	V_{IL}				$0.3 \times V_{SD}$	V
Logic 0 Output Voltage	V_{OL}	I_{SINK} = 3mA		0.15	0.4	V
Input Leakage				±0.01	±10	µA
Clock Frequency	f_{CLK}	**Standard/Fast Mode**			**400**	**kHz**
		High-Speed Mode			**3.4**	**MHz**
DIGITAL POWER SUPPLY						
Operating Voltage Range	V_{SD}		2.0		5.5	V
Digital Supply Current[2]	I_{SD}			25	50	µA
over Temperature				**100**		**µA**
TEMPERATURE						
Specified Temperature Range			–40		+85	°C
Operating Temperature Range		Junction Temperature < 125°C	–40		+95	°C
Storage Temperature Range			–65		+150	°C
Thermal Resistance	θ_{JA}					
TSSOP-8				150		°C/W
DFN-10				47		°C/W

(1) BUF01900 only.
(2) Minimum analog supply voltage is 8.5V when programming OTP memory.

BUF01900
BUF01901

TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = 18V, V_{SD} = 5V, R_L = 1.5kΩ connected to ground, and C_L = 200pF, unless otherwise noted.

ANALOG SUPPLY CURRENT vs TEMPERATURE

Figure 1

DIGITAL SUPPLY CURRENT vs TEMPERATURE

Figure 2

BUFFER OFFSET VOLTAGE vs TEMPERATURE
(V_S = 18V, V_{SD} = 5V)

Figure 3

OUTPUT VOLTAGE vs OUTPUT CURRENT

Figure 4

INTEGRAL NONLINEARITY ERROR vs INPUT CODE

Figure 5

DIFFERENTIAL NONLINEARITY ERROR vs INPUT CODE
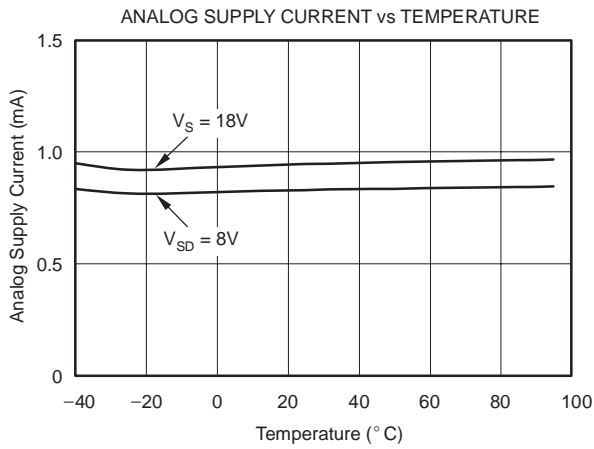
Figure 6

TYPICAL CHARACTERISTICS (cont)

At T_A = +25°C, V_S = 18V, V_{SD} = 5V, R_L = 1.5kΩ connected to ground, and C_L = 200pF, unless otherwise noted.
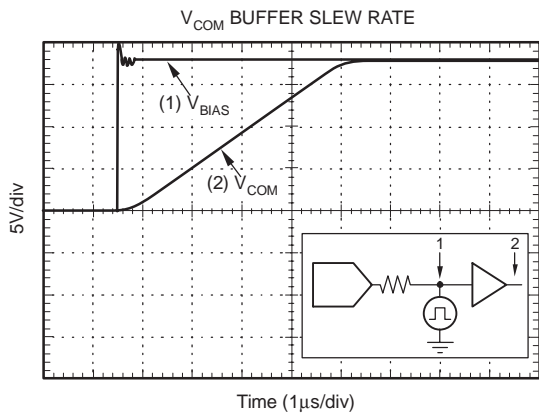
Figure 7
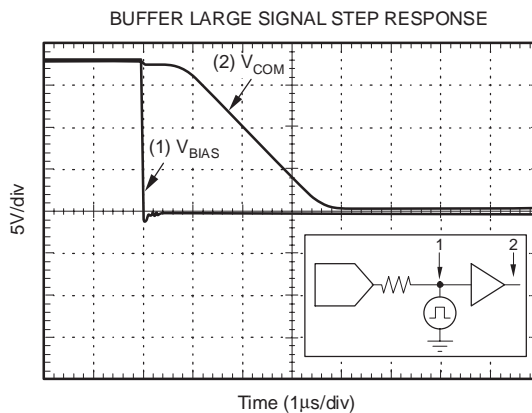
Figure 8
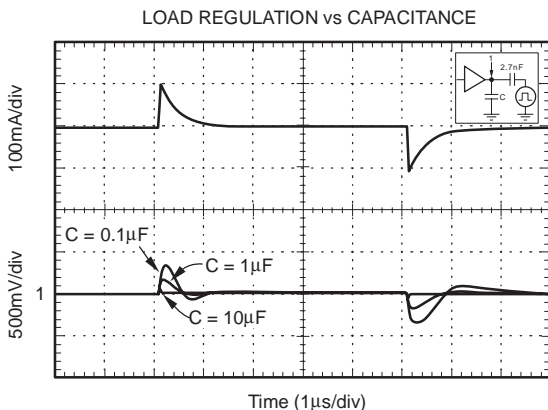
Figure 9
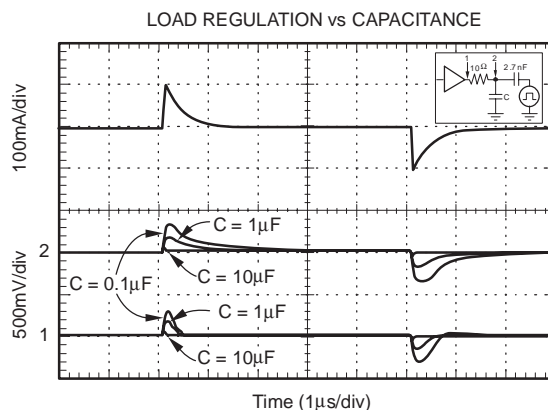
Figure 10
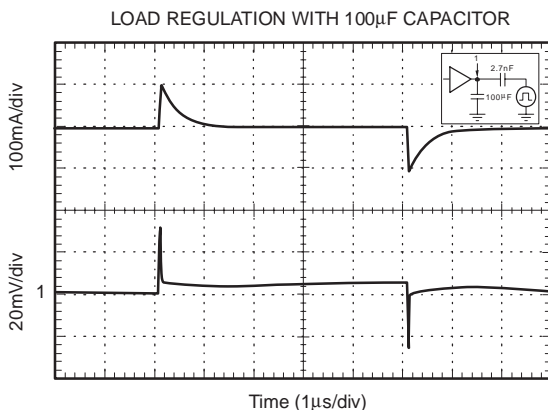
Figure 11
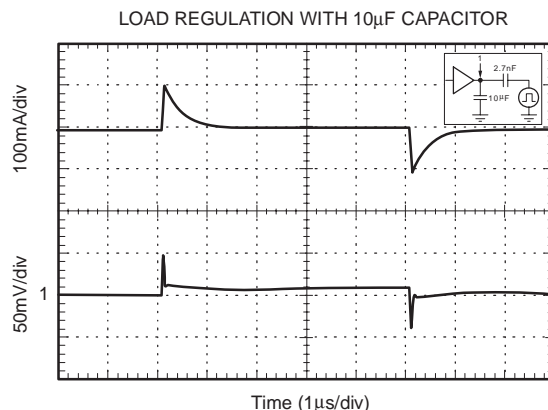
Figure 12

TYPICAL CHARACTERISTICS (cont)

At T_A = +25°C, V_S = 18V, V_{SD} = 5V, R_L = 1.5kΩ connected to ground, and C_L = 200pF, unless otherwise noted.

LOAD REGULATION WITH 1μF CAPACITOR
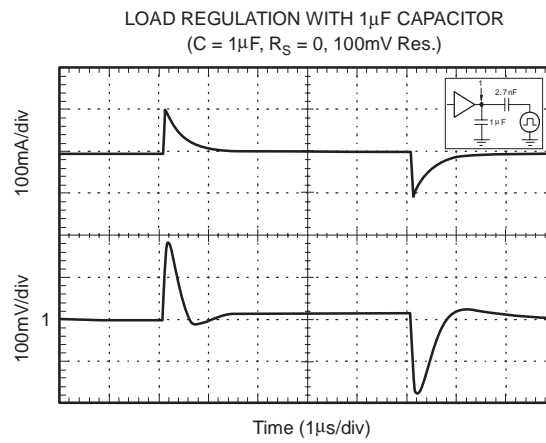(C = 1μF, R_S = 0, 100mV Res.)

Figure 13

APPLICATIONS INFORMATION

OVERVIEW

The BUF0190x family of products consists of a 10-bit digital-to-analog converter (DAC) that is programmed through an industry-standard two-wire interface. It contains on-chip nonvolatile memory that stores a specific DAC value that is read at power-up. The BUF0190x family consists of two devices: The BUF01900 contains a voltage buffer that is capable of driving high-current; the BUF01901 is a lower-cost version without the buffer. The BUF0190x is especially well-suited for V_{COM} calibration in LCD panels; however, it can also be used in many other applications. Figure 14 shows the BUF01900 in a typical configuration.

BUF01900: ON-CHIP BUFFER

Unlike many programmable V_{COM} calibrators on the market, the BUF01900 offers an integrated V_{COM} buffer with high current output drive capability. The output is capable of delivering peak currents over 100mA to within 4V from the positive supply and to within 2V from the negative supply. Using this option is very cost-effective and convenient in systems that do not use multi-channel gamma buffers with integrated V_{COM} drive. Figure 15 shows the BUF01900 in a typical configuration.
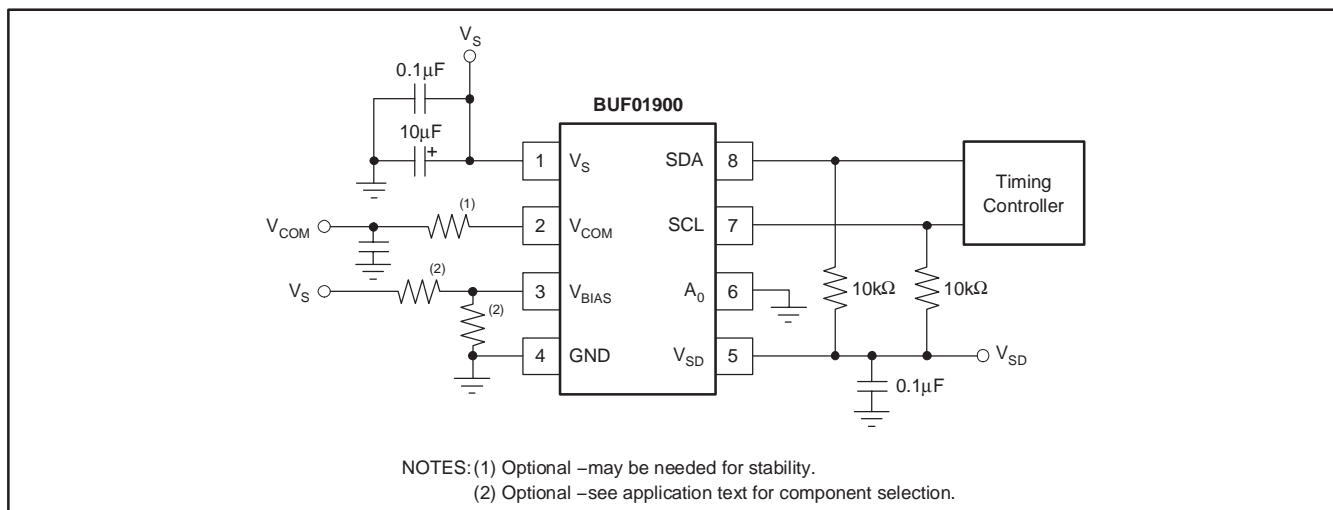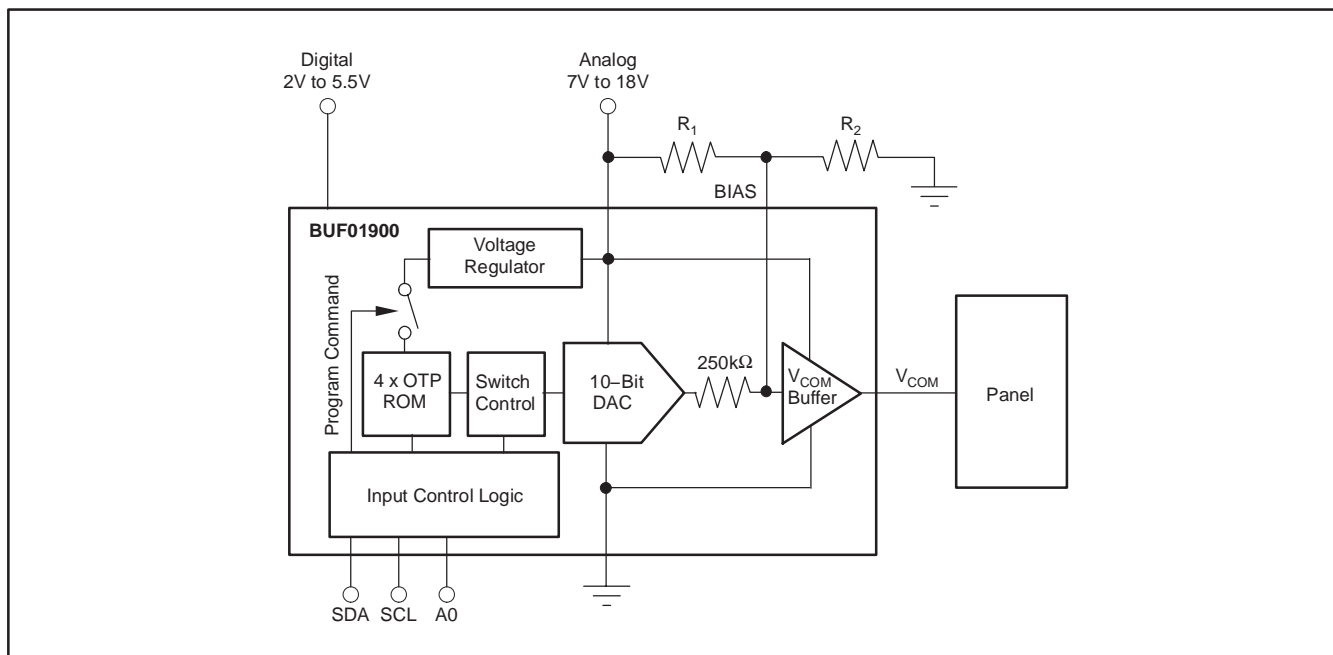

NOTES: (1) Optional – may be needed for stability.
(2) Optional – see application text for component selection.

Figure 14. Typical Application Diagram

Figure 15. BUF01900 Typical Configuration

BUF01900
BUF01901

![Texas Instruments logo]
TEXAS INSTRUMENTS
www.ti.com

SBOS337A – OCTOBER 2006 – REVISED OCTOBER 2006

BUF01901: USING EXTERNAL V_{COM} BUFFER

Many LCD panel modules use gamma buffers, such as TI's BUFxx704, BUFxx703, BUF11702 and the new BUF11705, that already include an integrated V_{COM} driver. Some other LCD modules use more complicated compensation schemes that require an external high-speed V_{COM} op amp. BUF01901 is optimized for lowest cost and is intended to be used with an external V_{COM} buffer or op amp. Figure 16 illustrates a typical configuration of the BUF01901 with the BUF11705.

ON-CHIP NONVOLATILE MEMORY

The BUF0190x is optimized for the smallest die size available and consequently the lowest cost to support high vol-

ume production. The on-chip OTP (one-time-programmable) memory helps to achieve significant die size reduction over EEPROM memory technology. This reduction is partly because of the smaller area of the OTP memory cell, but also a result of the fact that an EEPROM requires a high programming voltage typically generated with an onboard charge pump. OTP memory technology does not require the higher programming voltage; consequently, no charge pump is needed, resulting in a smaller and lower-cost solution.

During production, the V_{COM} voltage is typically adjusted only once. However, to allow for programming errors and rework, the BUF0190x supports a total of four write cycles to the OTP memory. This capacity means that the previously programmed code in the OTP can be overwritten a total of three times.
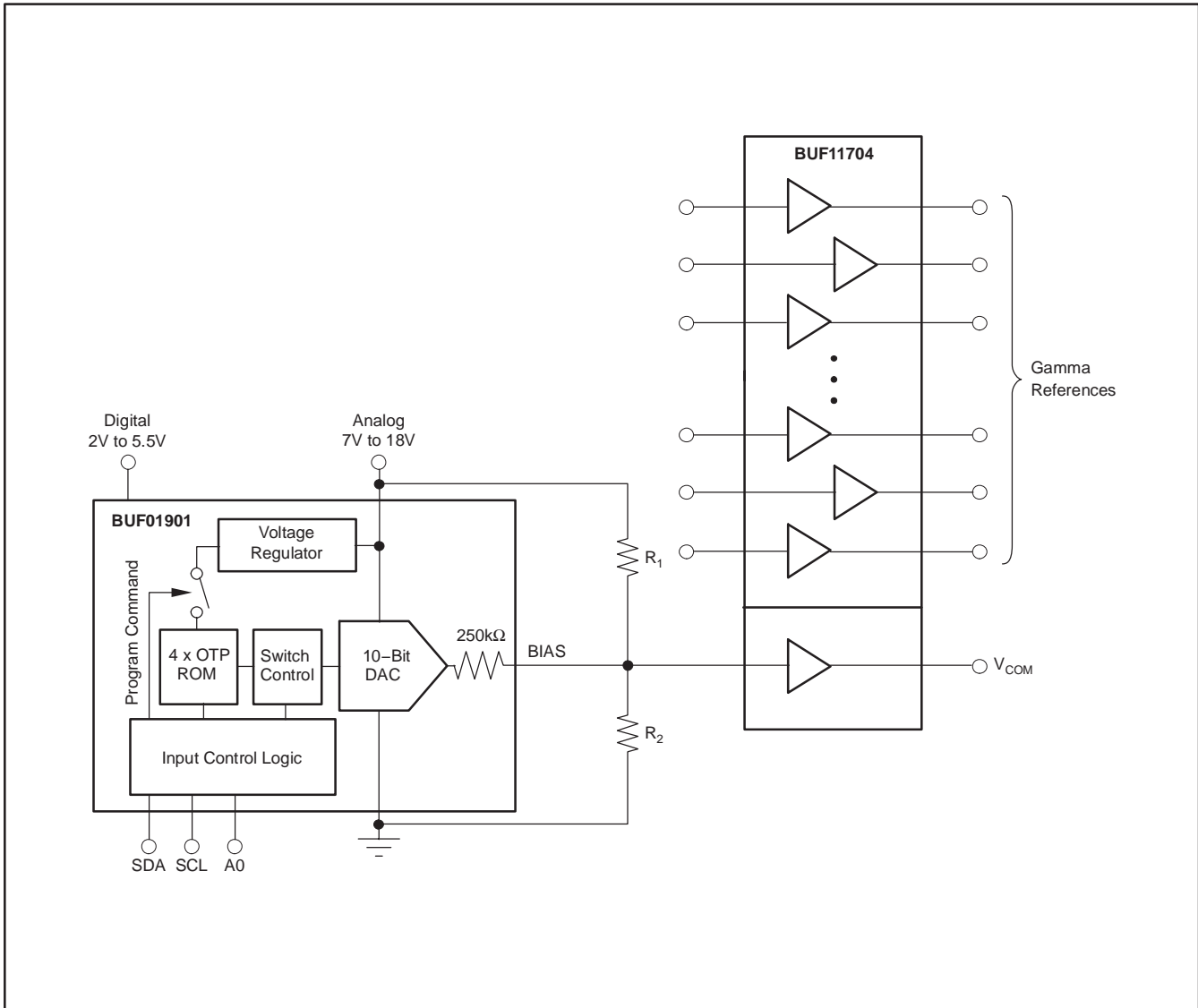

Figure 16. BUF01901 Typical Configuration

POWER-SUPPLY VOLTAGE

The BUF0190x can be powered using an analog supply voltage from 7V to 18V, and a digital supply from 2V to 5.5V. The digital supply must be applied prior to the analog supply to avoid excessive current and power consumption.

During programming of the OTP, the analog power supply must be at least 8.5V.

BUFFER INPUT AND OUTPUT RANGE

The integrated buffer has a single p-channel input stage. The input range includes the positive supply and extends down to typically 0.8V above the negative supply (GND). In a typical LCD application, this is normally sufficient because the nominal V_{COM} level is often close to $V_2/2$ and, therefore, fairly far away from either supply rail. In addition, the adjustment range is usually not much larger than 1V in either direction of the nominal V_{COM} voltage. In applications requiring a wider output swing, the output voltage to the buffer should be limited to approximately 0.8V above the negative power supply to keep the buffer input stage in its linear operating region. For lower input voltages, the output results might not be valid; however, they will also not lead to damage of the device.

The Rail-to-Rail output stage is designed to drive large peak currents greater than 100mA.

TWO-WIRE BUS OVERVIEW

The BUF0190x communicates through an industry-standard, two-wire interface to receive data in slave mode. This standard uses a two-wire, open-drain interface that supports multiple devices on a single bus. Bus lines are driven to a logic low level only. The device that initiates the communication is called a *master*, and the devices controlled by the master are *slaves*. The master generates the serial clock on the clock signal line (SCL), controls the bus access, and generates START and STOP conditions.

To address a specific device, the master initiates a START condition by pulling the data signal line (SDA) from a HIGH to LOW logic level while SCL is HIGH. All slaves on the bus shift in the slave address byte, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA LOW.

Data transfer is then initiated and eight bits of data are sent, followed by an Acknowledge bit. During data transfer, SDA must remain stable while SCL is HIGH. Any change in SDA while SCL is HIGH will be interpreted as a START or STOP condition.

Once all data has been transferred, the master generates a STOP condition, indicated by pulling SDA from LOW to HIGH while SCL is HIGH.

The BUF0190x can act only as a slave device; therefore, it never drives SCL. The SCL is only an input for the BUF0190x.

ADDRESSING THE BUF01900 AND BUF01901

The address of the BUF0190x in the TSSOP-8 package is 111011x, where *x* is the state of the A0 pin. When the A0 pin is LOW, the device acknowledges on address 76h. If the A0 pin is HIGH, the device acknowledges on address 77h. Table 1 summarizes device addresses.

Table 1. Quick-Reference Table of Addresses

DEVICE/COMPONENT	ADDRESS
TSSOP Package:	
A0 pin is LOW (device will acknowledge on address 76h)	1110110
A0 pin is HIGH (device will acknowledge on address 77h)	1110111
DFN Package:	
A0 pin is LOW, A1 is LOW (device will acknowledge on address 74h)	1110100
A0 pin is HIGH, A1 is LOW (device will acknowledge on address 75h)	1110101
A0 pin is LOW, A1 is HIGH (device will acknowledge on address 76h)	1110110
A0 pin is HIGH, A1 is HIGH (device will acknowledge on address 77h)	1110111

The address of the BUF0190x in the DFN-10 package is 11101yx, where *x* is the state of the A0 pin and *y* is the state of the A1 pin. When the A0 and A1 pins are both LOW, the device acknowledges on address 74h. If the A0 is HIGH and A1 is LOW, the device acknowledges on address 75h. When the A0 is LOW, and A1 is HIGH, the device acknowledges on address 76h. If the A0 and A1 pins are both HIGH, the device address is 77h.

Other addresses are possible through a simple mask change. Contact your TI representative for ordering information and availability.

DATA RATES

The two-wire bus operates in one of three speed modes:

- Standard: allows a clock frequency of up to 100kHz;
- Fast: allows a clock frequency of up to 400kHz; and
- High-speed mode (or Hs mode): allows a clock frequency of up to 3.4MHz.

The BUF0190x is fully compatible with all three modes. No special action is required to use the device in Standard or Fast modes, but High-speed mode must be activated. To activate High-speed mode, send a special address byte of 00001xxx, with SCL ≤ 400kHz, following the START condition; *xxx* are bits unique to the Hs-capable master, which can be any value. This byte is called the *Hs master code.* (Note that this is different from normal address bytes—the low bit does not indicate read/write status.) The BUF0190x will respond to the High-speed command regardless of the value of these last three bits. The BUF0190x does not acknowledge this byte; the communication protocol prohibits acknowledgment of the Hs master code. On receiving a master code, the BUF0190x switches on its Hs mode filters, and communicates at up to 3.4MHz.

Additional high-speed transfers may be initiated without resending the Hs mode byte by generating a repeat START without a STOP. The BUF0190x switches out of Hs mode with the next STOP condition.

GENERAL CALL RESET AND POWER-UP

The BUF0190x responds to a General Call Reset, which is an address byte of 00h (0000 0000) followed by a data byte of 06h (0000 0110). The BUF0190x acknowledges both bytes. Upon receiving a General Call Reset, the BUF0190x performs a full internal reset, as though it had been powered off and then on. It always acknowledges the General Call address byte of 00h (0000 0000), but does not acknowledge any General Call data bytes other than 06h (0000 0110).

The BUF0190x automatically performs a reset upon power-up. As part of the reset, the BUF0190x is configured for the output to change to the programmed OTP memory value, or to mid-scale, '1000000000', if the OTP value has not been programmed. Table 2 provides a summary of command codes.

READ/WRITE OPERATIONS:

Read commands are performed by setting the read/write bit HIGH. Setting the read/write bit LOW performs a write transaction.

Figure 17 and Figure 18 show the timing diagrams for read and write operations.

Writing:

To write to the DAC register:

1. Send a START condition on the bus.

2. Send the device address and read/write bit = LOW. The BUF01900/BUF01901 will acknowledge this byte.

3. Send two bytes of data for the DAC register. Begin by sending the most significant byte (bits D15—D8; only bits D9 and D8 are used, and D15—D13 must *not* be 010 or 001), followed by the least significant byte (bits D7—D0). The register is updated after receiving the second byte.

4. Send a STOP condition on the bus.

The BUF0190x acknowledges each data byte. If the master terminates communication early by sending a STOP or START condition on the bus, the DAC output will not update.

Reading:

To read the register of the DAC:

1. Send a START condition on the bus.

2. Send the device address and read/write bit = HIGH. The BUF0190x will acknowledge this byte.

3. Receive two bytes of data. The first received byte is the most significant byte (bits D15—D8; only bits D9 and D8 have meaning, and bits D15—D12 will show the programming status of the OTP memory). See Table 3. The next byte is the least significant byte (bits D7—D0).

4. Acknowledge after receiving the first byte only.

5. Do not acknowledge the second byte of data or send a STOP condition on the bus.

Communication may be terminated by the master by sending a premature STOP or START condition on the bus, or by not sending the Acknowledge.

Table 2. Quick-Reference Table of Command Codes

COMMAND	CODE
General Call Reset	Address byte of 00h followed by a data byte of 06h.
High-Speed Mode	00001xxx, with SCL ≤ 400kHz; where *xxx* are bits unique to the Hs-capable master. This byte is called the Hs master code.

Table 3. OTP Memory Status

CODE (Bits D15 – D12)	OTP PROGRAMMING STATUS
0000	OTP has not been programmed.
0001	OPT has been programmed once.
0011	OTP has programmed twice.
0111	OPT has programmed three times.
1111	OTP has programmed all four times.

ACQUIRE OF OTP MEMORY

An acquire command updates the DAC output to the value stored in OTP memory. If the OTP memory has not been programmed, the DAC output code is '0000000000'.

Figure 19 shows the timing diagram for the acquire command.

Acquire Command

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The device will acknowledge this byte.
3. Send the acquire command. Bits D7—D5 must be set to 001. Bits D4—D0 do not have meaning. This byte will be acknowledged.
4. Send a STOP condition on the bus.

Writing OTP Memory

The BUF0190x is able to write to the OTP memory a maximum of four times. Writing to the OTP memory a fourth time uses all available memory and disables the ability to perform additional writes (see table 3). A reset or acquire command updates the DAC output to the most recently written OTP memory value.

When programming the OTP memory, the analog supply voltage must be between 8.5V and 18V.

Write commands are performed by setting the read/write bit LOW.

To write to OTP memory:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF0190x acknowledges this byte.
3. Send two bytes of data for the OTP memory. Begin by sending the most significant byte first (bits D15—D8, of which only bits D9 and D8 are data bits, and bits D15—D13 must be 010), followed by the least significant byte (bits D7—D0). The register updates after receiving the second byte.
4. Send a STOP condition on the bus.

The BUF0190x acknowledges each data byte. If the master terminates communication early by sending a STOP or START condition on the bus, the specified OTP register will not be updated. Writing an OTP register updates the DAC output voltage.

Programming timing is taken from the two-wire bus. Therefore, the master must provide correct timing on the bus to ensure data is successfully written into OTP memory. Figure 20 shows the timing requirements for timing when the OTP write supply and OTP write signal are active.

![Texas Instruments logo]
TEXAS INSTRUMENTS
www.ti.com

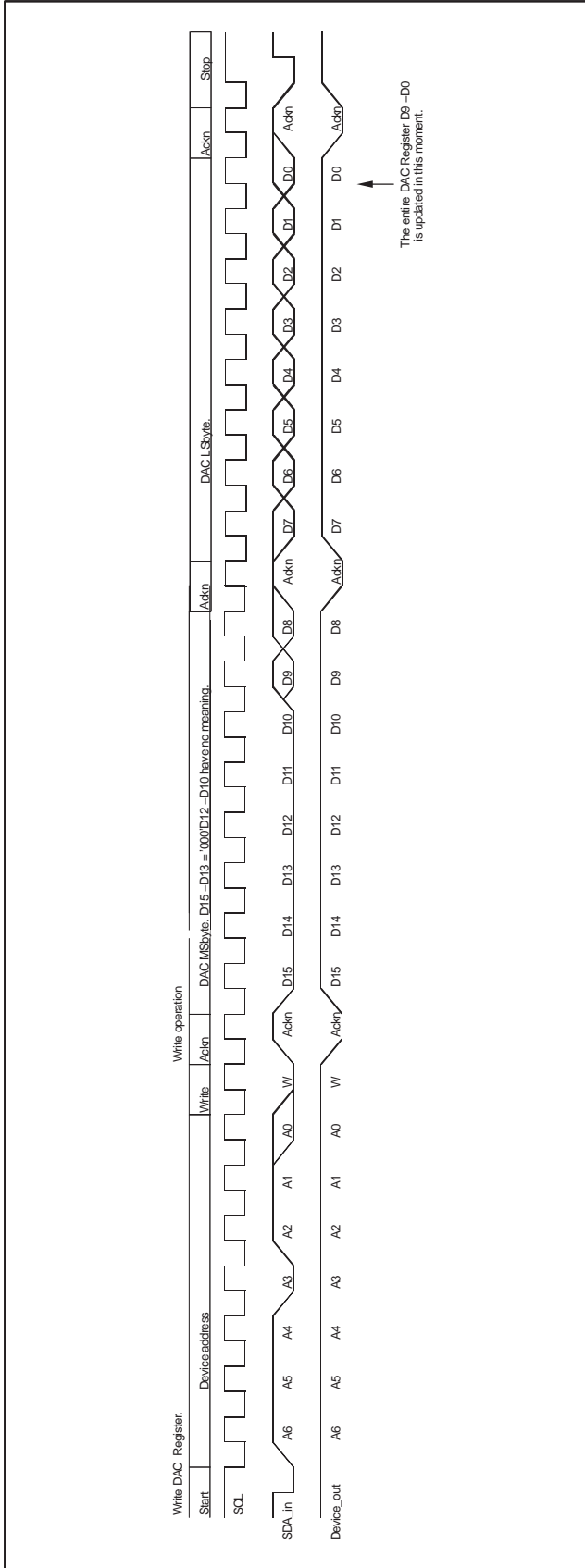SBOS337A – OCTOBER 2006 – REVISED OCTOBER 2006

Figure 17. Timing Diagram for Write DAC Register
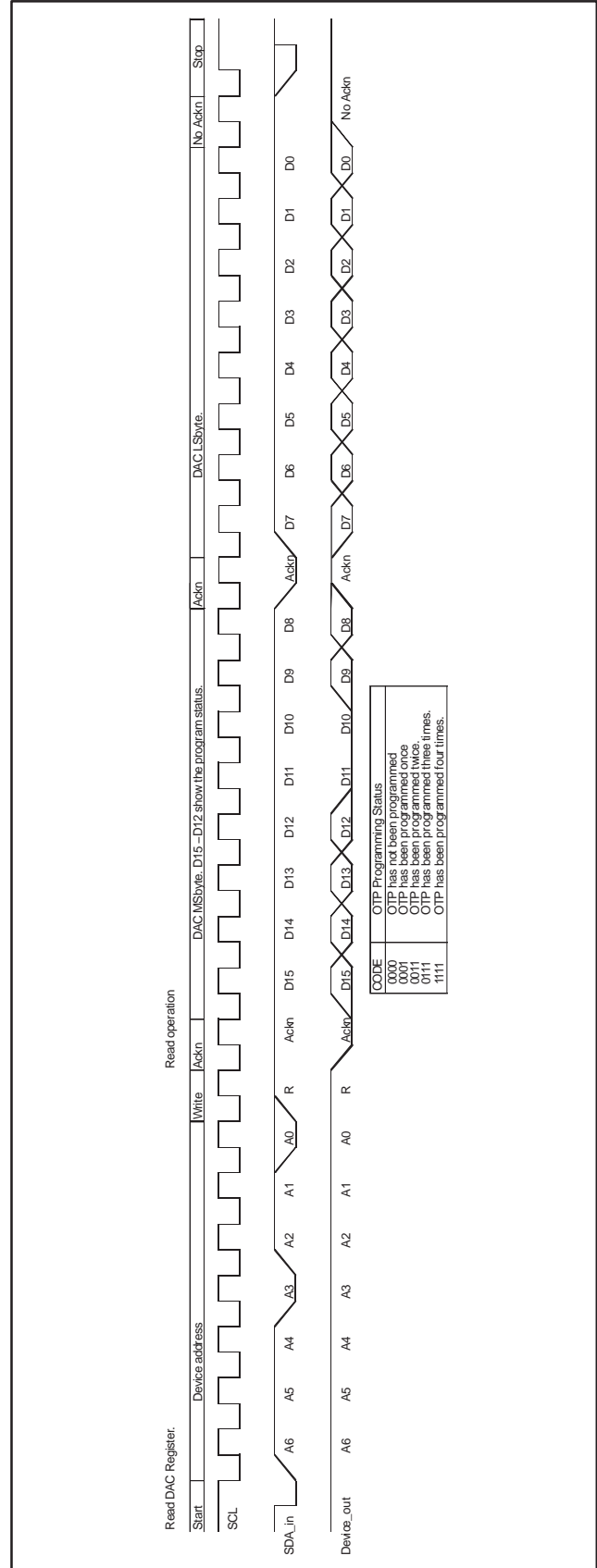

Figure 18. Timing Diagram for Read DAC Register
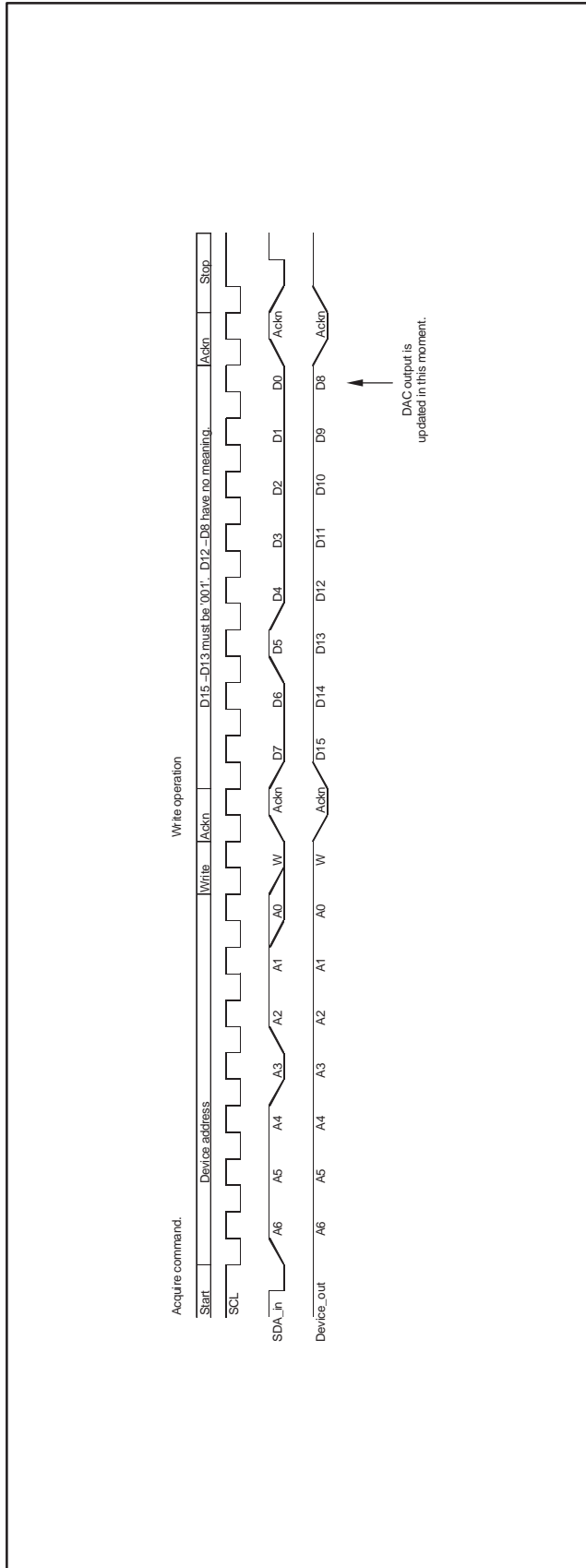
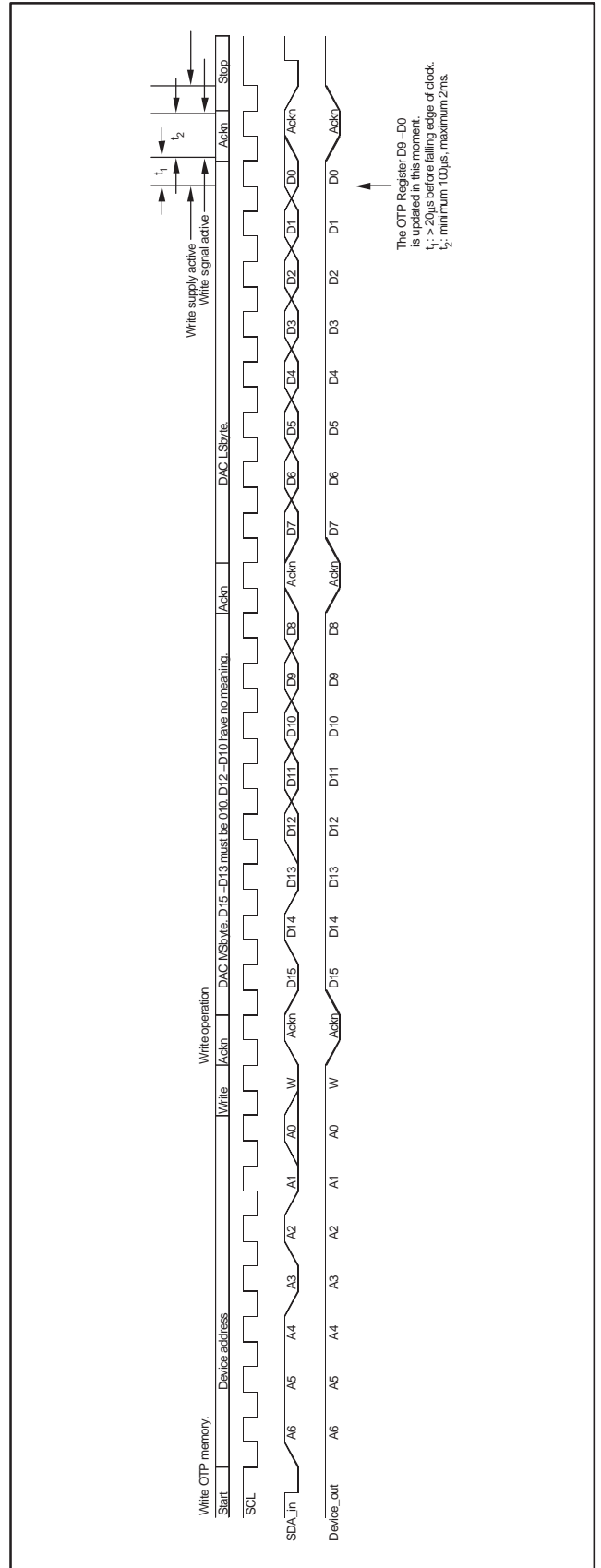**Figure 19. Timing Diagram for Acquire Command**

Figure 20. Timing Diagram for Write OTP Register

BUF01900
BUF01901

TEXAS
INSTRUMENTS
www.ti.com

SBOS337A – OCTOBER 2006 – REVISED OCTOBER 2006

V_{COM} CALIBRATION

V_{COM} CALIBRATION

The BUF0190x provides a simple, time- and cost-efficient means to adjust the flicker performance of LCD panels either manually or automatically during the final stages of the LCD panel manufacturing process.

The 10-bit adjustment resolution of the BUF0190x exceeds the typical adjustment resolution of existing V_{COM} calibrators significantly. As with a traditional V_{COM} adjustment, which uses a mechanical potentiometer and a voltage divider for adjustment (see Figure 21), the BUF0190x uses an external voltage divider that is used to set the initial V_{COM} voltage as well as the adjustment range.
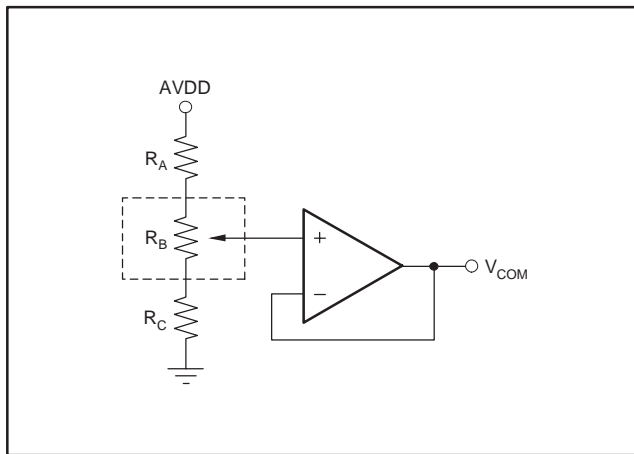

Figure 21. Traditional V_{COM} Adjustment

As Figure 22 shows, the 10-bit DAC acts as a Rail-to-Rail output voltage source with a nominal 250kΩ of output impedance. For example, at Code 000h, the lowest V_{COM} voltage is achieved since the 250kΩ impedance is now in parallel with R_2, which lowers the impedance of the lower side of the voltage divider. Consequently, code 3FFh results in the highest adjustable V_{COM} voltage.

Once the desired output level is obtained, the part can store the final setting using the non-volatile on-chip memory. See *Programming* section for detailed information.

(a) Code 00h equivalent circuit.

(b) Code 3FFh equivalent circuit.

NOTE: (1) Integrated into BUF01900 or external.
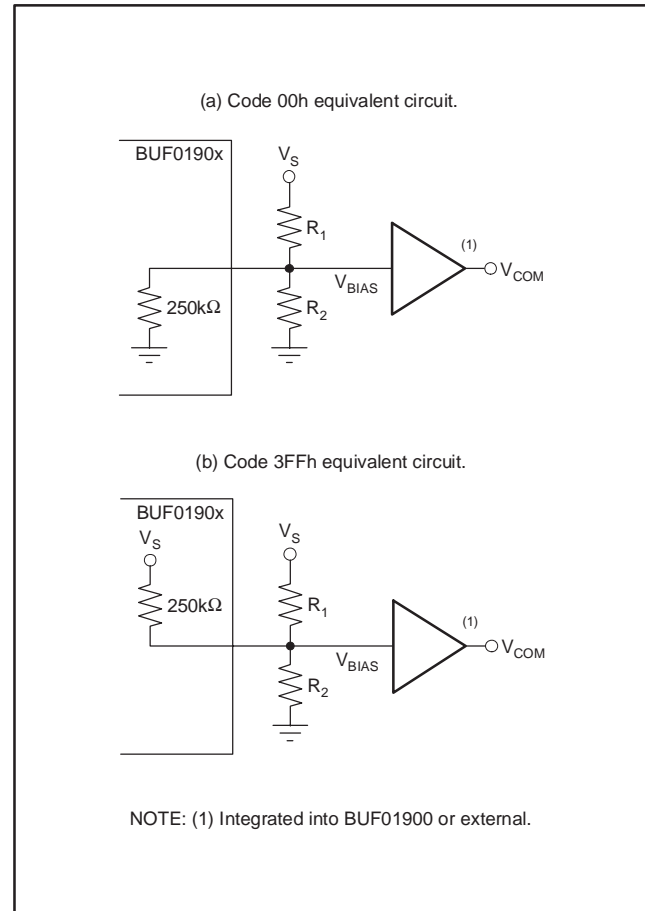
Figure 22. Simplified Block Diagram for V_{COM} Adjustment using BUF0190x

SELECTING THE ADJUSTMENT STEP SIZE

A maximum of 1024 adjustment steps can be realized with the BUF0190x, leading to very high adjustment resolution and very small step sizes. This flexibility can be advantageous during the panel development phase. In a practical production setting, however, this capability might lead to adjustment times that can be too long. A simple solution is to increase the step size between settings to more practical values for mass production. Limiting the number of adjustment steps between code 000h and code 3FFh to between 16 and 128 has been shown to typically yield acceptable adjustment results in the smallest amount of adjustment time.

EXTERNAL VOLTAGE DIVIDER RESISTOR SELECTION

The external resistive voltage-divider consisting of R_1 and R_2 (see Figure 16, Figure 17, and Figure 18) sets both the maximum value of the V_{COM} adjustment range and the initial V_{COM} voltage. Follow the steps below to calculate the correct values for R_1 and R_2

Step 1: Choose the supply voltage, (V_S)
Step 2: Set the nominal V_{COM} voltage. This voltage is the V_{COM} voltage at which the unadjusted panel should be at power-on. The default power-up DAC code is midscale.
Step 3: Choose the V_{COM} adjustment range. The adjustment range is the difference between the lowest and the highest desired V_{COM} voltage. If the default power-up code is not overwritten by software at the beginning of the adjustment cycle, the adjustment range is symmetrical around the chosen nominal V_{COM} voltage.
Step 4: Calculate the resistors based on the following formulas or simply download the Microsoft Excel™ calculator located in the product folder of BUF0190x available at www.ti.com.

$$R_1 = \frac{250k\Omega \cdot Adj\_range}{V_{COM} - 0.5 \cdot (Adj\_range)} \qquad (1)$$

$$R_2 = \frac{1}{\frac{V_S}{V_{COM}}\left(\frac{1}{R_1} + \frac{1}{500k\Omega}\right) - \frac{1}{R_1} - \frac{1}{250k\Omega}} \qquad (2)$$

CALCULATING THE V_{COM} OUTPUT VOLTAGE

With R_1 and R_2 properly set, V_{BIAS} or V_{COM} output voltage can be calculated for any digital code with the following formula:

$$V_{COM} = \frac{250k\Omega \cdot R_2 \cdot V_S + R_1 \cdot R_2 \cdot V_S (Code/1023)}{R_1 \cdot R_2 + 250k\Omega \cdot (R_1 + R_2)} \qquad (3)$$

CALCULATING THE ADJUSTMENT RESOLUTION

The resolution of the adjustment is a function of the step size. The resolution can be calculated by simply dividing the chosen adjustment range by the number of steps:

Resolution = Adj_range/steps (example: 32 steps between code 0h and code 3FFh)

DESIGN EXAMPLE

Step 1: Supply Voltage is 10V.
Step 2: Nominal V_{COM} is determined to be 4V.
Step 3: The desired total adjustment range is 1V. In the case of using the default power-up DAC code (midscale), the adjustment range for the V_{COM} voltage will be from 3.5V to 4.5V.
Step 4: Calculation of R_1 and R_2
R_1 = 71.4kΩ => choose closest 1% resistor (71.5kΩ)
R_2 = 45.5kΩ => choose closest 1% resistor (45.3kΩ)
Step 5: Appropriate number of adjustment steps between code 00h and code 3FFh is determined to be 32. This value leads to a step size of 32 codes between adjustment points, which translates into approximately 31mV voltage difference between steps.

MOTOR DRIVE CIRCUIT

The BUF01900 can be used to drive small motors directly because of the large output drive capability (> 100mA), as illustrated in Figure 23.
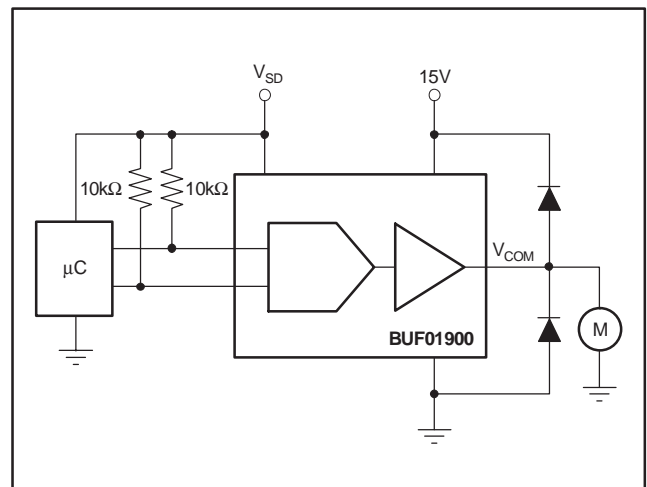

Figure 23. Motor Drive Circuit

SBOS337A – OCTOBER 2006 – REVISED OCTOBER 2006

PROGRAMMABLE POWER SUPPLY

The BUF0190x integrated buffer amplifier can drive large capacitive loads (see Typical Characteristics) and greater than 100mA of output current, making it well-suited for programmable power supplies.

Note that the BUF01900 integrated buffer has an input range that only extends to about 0.8V above GND; therefore, the programmable power supply is not able to output voltages less than approximately 0.8V.

NOTE: (1) Optional – see Typical Characteristic curves
Figure 10 through Figure 14 for load regulation performance.
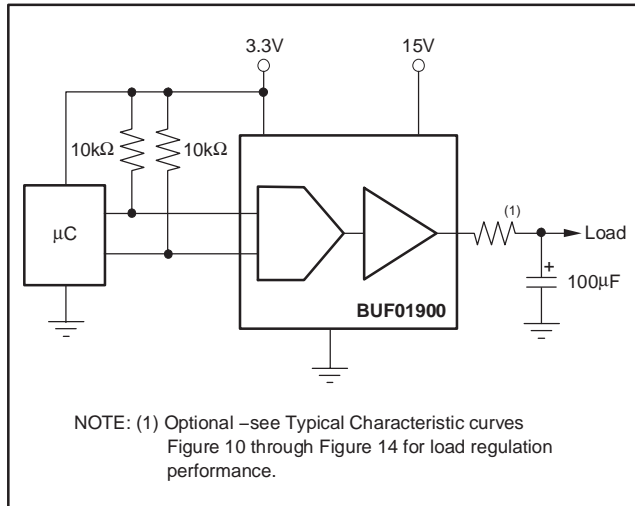
Figure 24. Programmable Power Supply

QFN/DFN THERMALLY-ENHANCED PACKAGE

The BUF0190x uses the 10-lead DFN package, a thin, thermally-enhanced package designed to eliminate the use of bulky heat sinks and slugs traditionally used in thermal packages. The DFN package can be easily mounted using standard printed circuit board (PCB) assembly techniques. See QFN/SON PCB Attachment Application Note (SLUA271) available at www.ti.com.

The thermal resistance junction to ambient ($R_{\theta JA}$) of the DFN package depends on the PCB layout. Using thermal vias and wide PCB traces improves thermal resistance. The thermal pad must be soldered to the PCB. The thermal pad on the bottom of the package should be connected to GND.

Soldering the exposed thermal pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests. Even with applications that have low-power dissipation, the exposed pad must be soldered to the PCB to provide structural integrity and long-term reliability.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BUF01900AIDRCR	NRND	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		BOO	
BUF01900AIDRCT	NRND	VSON	DRC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		BOO	
BUF01900AIPW	NRND	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		F01900	
BUF01900AIPWR	NRND	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		F01900	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BUF01900AIDRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BUF01900AIDRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BUF01900AIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BUF01900AIDRCR	VSON	DRC	10	3000	356.0	356.0	35.0
BUF01900AIDRCT	VSON	DRC	10	250	210.0	185.0	35.0
BUF01900AIPWR	TSSOP	PW	8	2000	356.0	356.0	35.0

TEXAS INSTRUMENTS

PACKAGE MATERIALS INFORMATION

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
BUF01900AIPW	PW	TSSOP	8	150	530	10.2	3600	3.5

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4226193/A

A | 3.1 / 2.9 | B

PIN 1 INDEX AREA

3.1 / 2.9

1.0 / 0.8

0.05 / 0.00

C

SEATING PLANE

0.08 | C

1.65 ± 0.1

2X (0.5)

4X (0.25)

EXPOSED THERMAL PAD

5

6

2X [2]

11

SYMM ₵

2.4 ± 0.1

1

10

8X [0.5]

PIN 1 ID (OPTIONAL)

SYMM ₵

10X 0.5 / 0.3

10X 0.30 / 0.18

(0.2) TYP

⊕	0.1 Ⓜ	C	A	B
	0.05 Ⓜ	C		

4218878/B   07/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

TEXAS INSTRUMENTS

www.ti.com

(1.65)

(0.5)

10X (0.6)

1

10X (0.24)

SYMM
₵

11

10

8X (0.5)

5

(R0.05) TYP

(2.4)

(3.4)

(0.95)

6

(⌀ 0.2) VIA
TYP

(0.25)

(0.575)

SYMM
₵

(2.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

0.07 MAX
ALL AROUND

EXPOSED METAL

SOLDER MASK
OPENING

METAL

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

EXPOSED METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4218878/B   07/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

DRC0010J

2X (1.5)

(0.5)

SYMM

EXPOSED METAL
TYP

11

10X (0.6)

1

10X (0.24)

10

(1.53)

2X
(1.06)

SYMM

(0.63)

8X (0.5)

5

6

(R0.05) TYP

4X (0.34)

4X (0.25)

(2.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B   07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
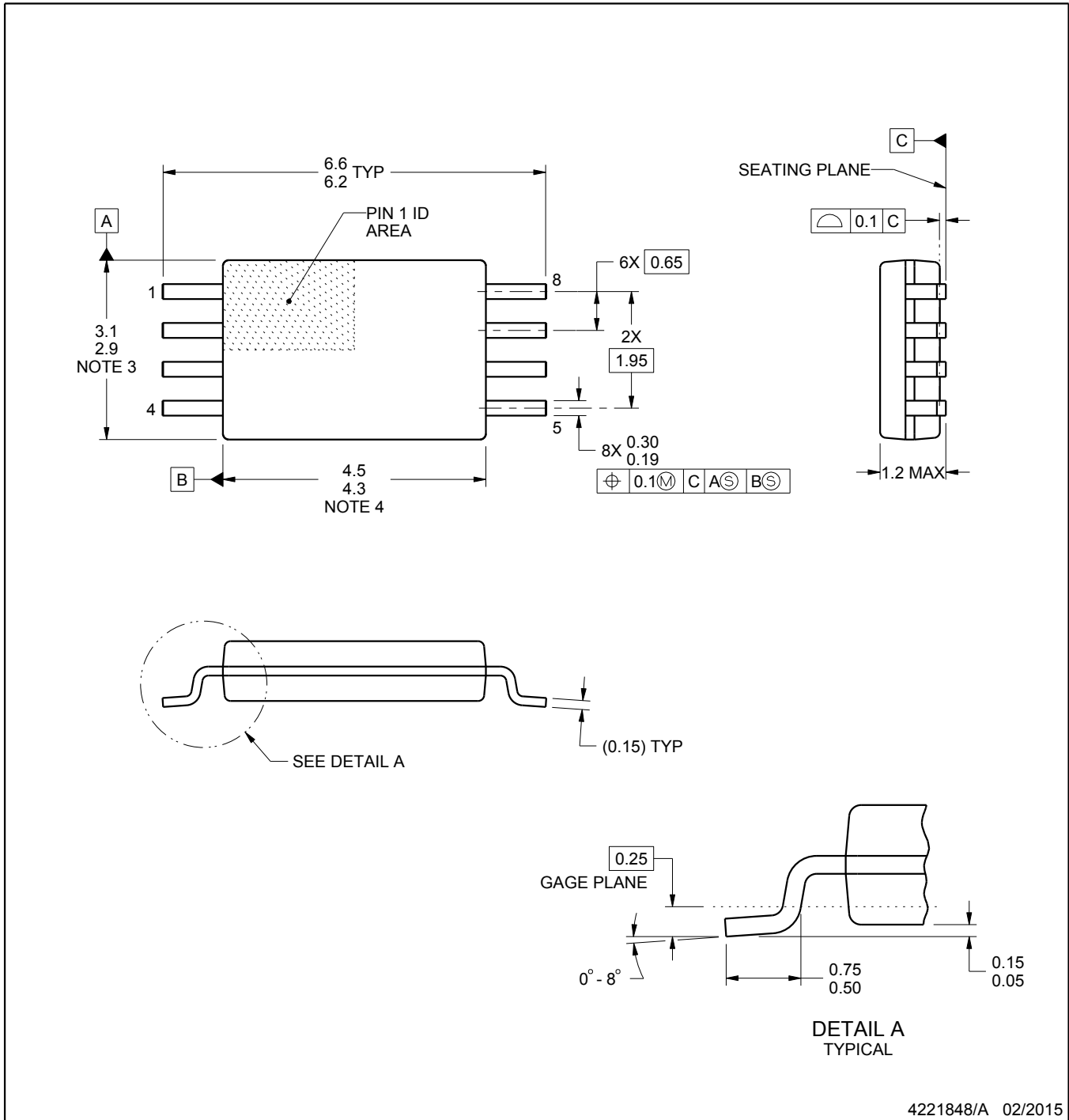   design recommendations.

6.6
6.2 TYP

A

PIN 1 ID
AREA

1

8

6X 0.65

3.1
2.9
NOTE 3

2X

1.95

4

5

B

4.5
4.3
NOTE 4

8X 0.30
0.19

⊕ 0.1 Ⓜ C AⓈ BⓈ

C

SEATING PLANE

◠ 0.1 C

1.2 MAX

SEE DETAIL A

(0.15) TYP

0.25

GAGE PLANE

0° - 8°

0.75
0.50

0.15
0.05

DETAIL A
TYPICAL

4221848/A 02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

Texas
Instruments
www.ti.com

8X (0.45)

8X (1.5)

SYMM

(R0.05) TYP

1

8

SYMM

6X (0.65)

4

5

(5.8)

LAND PATTERN EXAMPLE
SCALE:10X

SOLDER MASK OPENING

METAL

METAL UNDER SOLDER MASK

SOLDER MASK OPENING

0.05 MAX ALL AROUND

0.05 MIN ALL AROUND

NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4221848/A   02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

8X (1.5)

8X (0.45)

SYMM

(R0.05) TYP

1

8

SYMM

6X (0.65)

4

5

(5.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A   02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.