OPAx377-Q1 Low-Noise, Low Quiescent Current, Precision Automotive Grade Operational Amplifier

1 Features
- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 3A
  - Device CDM ESD Classification Level C6
- Low Noise: 7.5 nV/√Hz at 1 kHz
- 0.1-Hz to 10-Hz Noise: 0.8 μV_{PP}
- Quiescent Current: 760 μA (typical)
- Low Offset Voltage: 250 μV (typical)
- Gain Bandwidth Product: 5.5 MHz
- Rail-to-Rail Input and Output
- Single-Supply Operation
- Supply Voltage: 2.2 V to 5.5 V
- Space-Saving Packages:
  - SOT-23, VSSOP, TSSOP

2 Applications
- Active Cruise Control
- Park Assist
- Tire Pressure Monitoring
- Infotainment
- Active Filtering
- Sensor Signal Conditioning

3 Description
The OPAx377-Q1 family of operational amplifiers are wide-bandwidth CMOS amplifiers that provide very low noise, low input bias current, and low offset voltage while operating on a low quiescent current of 0.76 mA (typical).

The OPAx377-Q1 op amps are optimized for low-voltage, single-supply applications. The exceptional combination of ac and dc performance make them ideal for a wide range of applications, including small signal conditioning, audio, and active filters. In addition, these parts have a wide supply range with excellent PSRR, making them attractive for applications that run directly from batteries without regulation.

The OPA377-Q1 is available in the SOT23-5 package. The dual, OPA2377-Q1, is offered in the MSOP-8 package and the quad OPA4377-Q1 is offered in the TSSOP-14 package. All versions are specified for operation from –40°C to +125°C.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA377-Q1</td>
<td>SOT-23 (5)</td>
<td>2.90 mm × 1.60 mm</td>
</tr>
<tr>
<td>OPA2377-Q1</td>
<td>VSSOP (8)</td>
<td>3.00 mm × 3.00 mm</td>
</tr>
<tr>
<td>OPA4377-Q1</td>
<td>TSSOP (14)</td>
<td>5.00 mm × 4.40 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.
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## 4 Revision History

Changes from Original (May 2016) to Revision A

- Changed device status from *Product Preview* to *Production Data* ....................................................... 1
5 Pin Configuration and Functions

**OPA377-Q1: DBV Package**
5-Pin SOT23
Top View

Pin Functions: OPA377-Q1

<table>
<thead>
<tr>
<th>PIN</th>
<th>NO.</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>+IN</td>
<td>3</td>
<td>I</td>
<td>Noninverting input</td>
</tr>
<tr>
<td>–IN</td>
<td>4</td>
<td>I</td>
<td>Inverting input</td>
</tr>
<tr>
<td>NC</td>
<td>—</td>
<td>—</td>
<td>No internal connection (can be left floating)</td>
</tr>
<tr>
<td>OUT</td>
<td>1</td>
<td>O</td>
<td>Output</td>
</tr>
<tr>
<td>V–</td>
<td>2</td>
<td>—</td>
<td>Negative (lowest) power supply</td>
</tr>
<tr>
<td>V+</td>
<td>5</td>
<td>—</td>
<td>Positive (highest) power supply</td>
</tr>
</tbody>
</table>
## OPA2377-Q1: DGK Package

8-Pin VSSOP and SOIC

### Top View

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>–IN A</td>
<td>2</td>
<td>I Inverting input, channel A</td>
</tr>
<tr>
<td>–IN B</td>
<td>6</td>
<td>I Inverting input, channel B</td>
</tr>
<tr>
<td>+IN A</td>
<td>3</td>
<td>I Noninverting input, channel A</td>
</tr>
<tr>
<td>+IN B</td>
<td>5</td>
<td>I Noninverting input, channel B</td>
</tr>
<tr>
<td>OUT A</td>
<td>1</td>
<td>O Output, channel A</td>
</tr>
<tr>
<td>OUT B</td>
<td>7</td>
<td>O Output, channel B</td>
</tr>
<tr>
<td>V–</td>
<td>4</td>
<td>– Negative (lowest) power supply</td>
</tr>
<tr>
<td>V+</td>
<td>8</td>
<td>– Positive (highest) power supply</td>
</tr>
</tbody>
</table>
### Pin Functions: OPA4377-Q1

<table>
<thead>
<tr>
<th>PIN NAME</th>
<th>NO.</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>–IN A</td>
<td>2</td>
<td>I</td>
<td>Inverting input, channel A</td>
</tr>
<tr>
<td>–IN B</td>
<td>6</td>
<td>I</td>
<td>Inverting input, channel B</td>
</tr>
<tr>
<td>–IN C</td>
<td>9</td>
<td>I</td>
<td>Inverting input, channel C</td>
</tr>
<tr>
<td>–IN D</td>
<td>13</td>
<td>I</td>
<td>Inverting input, channel D</td>
</tr>
<tr>
<td>+IN A</td>
<td>3</td>
<td>I</td>
<td>Noninverting input, channel A</td>
</tr>
<tr>
<td>+IN B</td>
<td>5</td>
<td>I</td>
<td>Noninverting input, channel B</td>
</tr>
<tr>
<td>+IN C</td>
<td>10</td>
<td>I</td>
<td>Noninverting input, channel C</td>
</tr>
<tr>
<td>+IN D</td>
<td>12</td>
<td>I</td>
<td>Noninverting input, channel D</td>
</tr>
<tr>
<td>OUT A</td>
<td>1</td>
<td>O</td>
<td>Output, channel A</td>
</tr>
<tr>
<td>OUT B</td>
<td>7</td>
<td>O</td>
<td>Output, channel B</td>
</tr>
<tr>
<td>OUT C</td>
<td>8</td>
<td>O</td>
<td>Output, channel C</td>
</tr>
<tr>
<td>OUT D</td>
<td>14</td>
<td>O</td>
<td>Output, channel D</td>
</tr>
<tr>
<td>V–</td>
<td>11</td>
<td>—</td>
<td>Negative (lowest) power supply</td>
</tr>
<tr>
<td>V+</td>
<td>4</td>
<td>—</td>
<td>Positive (highest) power supply</td>
</tr>
</tbody>
</table>

**OPA4377-Q1: PW Package**

14-Pin TSSOP

Top View
6 Specifications

6.1 Absolute Maximum Ratings
over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_S = (V+) - (V-) )</td>
<td>7</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Signal input terminal voltage(^{(2)})</td>
<td>((V-) - 0.5)</td>
<td>((V+) + 0.5)</td>
<td>V</td>
</tr>
<tr>
<td>Signal input terminal current(^{(2)})</td>
<td>-10</td>
<td>10</td>
<td>mA</td>
</tr>
<tr>
<td>Output short-circuit current(^{(3)})</td>
<td>Continuous</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( T_A ) Operating temperature</td>
<td>-40</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>( T_J ) Junction temperature</td>
<td>150</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>( T_{stg} ) Storage temperature</td>
<td>-65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

\(^{(2)}\) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.

\(^{(3)}\) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>( V_{(ESD)} )</th>
<th>Electrostatic discharge</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human-body model (HBM), per AEC Q100-002(^{(1)})</td>
<td>±4000</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Charged-device model (CDM), per AEC Q100-011</td>
<td>±1000</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions
over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>2.2</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>( T_A ) Operating temperature</td>
<td>-40</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

6.4 Thermal Information: OPA377-Q1

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>OPA377-Q1 DBV (SOT23)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{JA} ) Junction-to-ambient thermal resistance</td>
<td>273.8</td>
<td>°C/W</td>
</tr>
<tr>
<td>( R_{JC(top)} ) Junction-to-case (top) thermal resistance</td>
<td>126.8</td>
<td>°C/W</td>
</tr>
<tr>
<td>( R_{JB} ) Junction-to-board thermal resistance</td>
<td>85.9</td>
<td>°C/W</td>
</tr>
<tr>
<td>( \psi_{JT} ) Junction-to-top characterization parameter</td>
<td>10.9</td>
<td>°C/W</td>
</tr>
<tr>
<td>( \psi_{JB} ) Junction-to-board characterization parameter</td>
<td>84.9</td>
<td>°C/W</td>
</tr>
<tr>
<td>( R_{JC(bot)} ) Junction-to-case (bottom) thermal resistance</td>
<td>n/a</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

\(^{(1)}\) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

6.5 Thermal Information: OPA2377-Q1

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>OPA2377-Q1 DGK (VSSOP)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{JA} ) Junction-to-ambient thermal resistance</td>
<td>171.2</td>
<td>°C/W</td>
</tr>
<tr>
<td>( R_{JC(top)} ) Junction-to-case (top) thermal resistance</td>
<td>63.9</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

\(^{(1)}\) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.
## Thermal Information: OPA2377-Q1 (continued)

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>OPA2377-Q1</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{JB}$ Junction-to-board thermal resistance</td>
<td>92.8 °C/W</td>
</tr>
<tr>
<td>$\psi_{JT}$ Junction-to-top characterization parameter</td>
<td>9.2 °C/W</td>
</tr>
<tr>
<td>$\psi_{JB}$ Junction-to-board characterization parameter</td>
<td>91.2 °C/W</td>
</tr>
<tr>
<td>$R_{JC(bot)}$ Junction-to-case (bottom) thermal resistance</td>
<td>n/a °C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

### 6.6 Thermal Information: OPA4377-Q1

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>OPA4377-Q1</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{JA}$ Junction-to-ambient thermal resistance</td>
<td>107.8 °C/W</td>
</tr>
<tr>
<td>$R_{JC(top)}$ Junction-to-case (top) thermal resistance</td>
<td>29.6 °C/W</td>
</tr>
<tr>
<td>$R_{JB}$ Junction-to-board thermal resistance</td>
<td>52.6 °C/W</td>
</tr>
<tr>
<td>$\psi_{JT}$ Junction-to-top characterization parameter</td>
<td>1.5 °C/W</td>
</tr>
<tr>
<td>$\psi_{JB}$ Junction-to-board characterization parameter</td>
<td>51.6 °C/W</td>
</tr>
<tr>
<td>$R_{JC(bot)}$ Junction-to-case (bottom) thermal resistance</td>
<td>n/a °C/W</td>
</tr>
</tbody>
</table>

### 6.7 Electrical Characteristics: $V_S = 2.2$ V to 5.5 V

At $T_A = 25^\circ$C, $R_L = 10$ kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OS}$ Input offset voltage</td>
<td>$V_S = 5$ V</td>
<td>0.25</td>
<td>1</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Input offset voltage versus temperature</td>
<td>At $T_A = -40^\circ$C to +125°C, $V_S = 2.2$ V to 5.5 V, $V_{CM} &lt; (V+) – 1.3$ V</td>
<td>5</td>
<td></td>
<td>µV/V</td>
<td></td>
</tr>
<tr>
<td>$dV_{OS}/dT$ Input offset voltage versus drift</td>
<td>At $T_A = -40^\circ$C to +125°C</td>
<td>0.32</td>
<td>2</td>
<td>µV/°C</td>
<td></td>
</tr>
<tr>
<td>PSRR Input offset voltage versus power supply</td>
<td>At $T_A = 25^\circ$C, $V_S = 2.2$ V to 5.5 V, $V_{CM} &lt; (V+) – 1.3$ V</td>
<td>5</td>
<td>28</td>
<td>µV/V</td>
<td></td>
</tr>
<tr>
<td>Channel separation, dc (dual, quad)</td>
<td></td>
<td>0.5</td>
<td></td>
<td>µV/V</td>
<td></td>
</tr>
<tr>
<td>$I_{IB}$ Input bias current</td>
<td></td>
<td>$\pm0.2$</td>
<td>$\pm10$</td>
<td>pA</td>
<td></td>
</tr>
<tr>
<td>Input bias current versus temperature</td>
<td>See Typical Characteristics</td>
<td></td>
<td></td>
<td>pA</td>
<td></td>
</tr>
<tr>
<td>$I_{OS}$ Input offset current</td>
<td></td>
<td>$\pm0.2$</td>
<td>$\pm10$</td>
<td>pA</td>
<td></td>
</tr>
<tr>
<td>NOISE Input voltage noise</td>
<td>$f = 0.1$ Hz to 10 Hz</td>
<td>0.8</td>
<td></td>
<td>µVpp</td>
<td></td>
</tr>
<tr>
<td>$e_{n}$ Input voltage noise density</td>
<td>$f = 1$ kHz</td>
<td>7.5</td>
<td></td>
<td>nV/√Hz</td>
<td></td>
</tr>
<tr>
<td>$i_{n}$ Input current noise density</td>
<td>$f = 1$ kHz</td>
<td>2</td>
<td></td>
<td>fA/√Hz</td>
<td></td>
</tr>
<tr>
<td>INPUT VOLTAGE RANGE $V_{CM}$ Common-mode voltage range</td>
<td>$(V-) – 0.1$</td>
<td>$(V+) + 0.1$</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMRR Common-mode rejection ratio</td>
<td>$(V-) &lt; V_{CM} &lt; (V+) – 1.3$ V</td>
<td>70</td>
<td>90</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>INPUT CAPACITANCE Differential</td>
<td></td>
<td>6.5</td>
<td></td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>Common-mode</td>
<td></td>
<td>13</td>
<td></td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>OPEN-LOOP GAIN $A_{OL}$ Open-loop voltage gain</td>
<td>$50$ mV &lt; $V_O &lt; (V+) – 50$ mV, $R_L = 10$ kΩ</td>
<td>112</td>
<td>134</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>$100$ mV &lt; $V_O &lt; (V+) – 100$ mV, $R_L = 2$ kΩ</td>
<td>126</td>
<td></td>
<td>dB</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

FREQUENCY RESPONSE, $V_S = 5.5$ V
Electrical Characteristics: $V_S = 2.2\text{ V to 5.5 V}$ (continued)

At $T_A = 25^\circ\text{C}$, $R_L = 10\ \text{k}\Omega$ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>GBW</td>
<td>Gain-bandwidth product</td>
<td>5.5</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>SR</td>
<td>Slew rate</td>
<td>G = +1</td>
<td>2</td>
<td>V/μs</td>
<td></td>
</tr>
<tr>
<td>$t_S$</td>
<td>Settling time</td>
<td>At 0.1%, 2-V step, G = +1</td>
<td>1.6</td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>At 0.01%, 2-V step, G = +1</td>
<td>2</td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td>Overload recovery time</td>
<td>$V_S \times \text{Gain} &gt; V_S$</td>
<td>0.33</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>THD+N</td>
<td>Total harmonic distortion + noise</td>
<td>$V_O = 1\text{ V}_{\text{RMS}}, G = +1, f = 1\text{ kHz}, R_L = 10\ \text{k}\Omega$</td>
<td>0.00027%</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| OUTPUT                 |                                                      |     |     |     |       |
| Voltage output swing from rail | At $T_A = 25^\circ\text{C}$, $R_L = 10\ \text{k}\Omega$ | 10  |     | 20  | mV    |
| | At $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $R_L = 10\ \text{k}\Omega$ | 40  |     |     | mV    |
| $I_{SC}$               | Short-circuit current                               |     | +30/–50 | mA  |
| $C_{LOAD}$             | Capacitive load drive                               | See Typical Characteristics |     |     |       |
| $R_O$                  | Open-loop output impedance                          | 150 |     |     | Ω     |

| POWER SUPPLY           |                                                      |     |     |     |       |
| $V_S$                  | Specified voltage                                   | 2.2 |     | 5.5 | V     |
| $I_Q$                  | Quiescent current (per amplifier)                   | At $T_A = 25^\circ\text{C}$, $I_Q = 0$, $V_S = 5.5\text{ V}$ | 0.76 | 1.05 | mA   |
|                        |                                                     | At $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ | 1.2  |     | mA   |

| TEMPERATURE            |                                                      |     |     |     |       |
| Specified temperature  |                                                      | −40 |     | +125 | °C    |
6.8 Typical Characteristics
At $T_A = 25^\circ C$, $V_S = 5\, V$, $R_L = 10\, k\Omega$ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.
Typical Characteristics (continued)

At $T_A = 25^\circ C$, $V_S = 5\, V$, $R_L = 10\, k\Omega$ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

![Figure 7. Common-Mode Rejection Ratio vs Temperature](image)

![Figure 8. Quiescent Current vs Temperature](image)

![Figure 9. Quiescent and Short-Circuit Current vs Supply Voltage](image)

![Figure 10. Short-Circuit Current vs Temperature](image)

![Figure 11. Input Bias Current vs Temperature](image)

![Figure 12. Output Voltage vs Output Current](image)
Typical Characteristics (continued)

At $T_A = 25^\circ C$, $V_S = 5 \text{ V}$, $R_L = 10 \text{ k}\Omega$ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

**Figure 13. Offset Voltage Production Distribution**

**Figure 14. Maximum Output Voltage vs Frequency**

**Figure 15. Small-Signal Overshoot vs Load Capacitance**

**Figure 16. Small-Signal Pulse Response**

**Figure 17. Large-Signal Pulse Response**

**Figure 18. Settling Time vs Closed-Loop Gain**
Typical Characteristics (continued)

At $T_A = 25^\circ C$, $V_S = 5$ V, $R_L = 10 \, k\Omega$ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

Figure 19. Channel Separation vs Frequency
Figure 20. Open-Loop Output Resistance vs Frequency
Figure 21. Input Offset Voltage vs Common-Mode Voltage
7 Detailed Description

7.1 Overview
The OPAx377-Q1 family belongs to a new generation of low-noise operational amplifiers, giving customers outstanding dc precision and ac performance. Low noise, rail-to-rail input and output, and low offset, drawing a low quiescent current, make these devices ideal for a variety of precision and portable applications. In addition, this device has a wide supply range with excellent PSRR, making it a suitable option for applications that are battery-powered without regulation.

7.2 Functional Block Diagram
7.3 Feature Description

7.3.1 Operating Characteristics

The OPAx377-Q1 family of amplifiers has parameters that are fully specified from 2.2 V to 5.5 V (±1.1 V to ±2.75 V). Many of the specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the Typical Characteristics section.

7.3.2 Common-Mode Voltage Range

The input common-mode voltage range of the OPAx377-Q1 series extends 100 mV beyond the supply rails. The offset voltage of the amplifier is low, from approximately (V−) to (V+) – 1 V, as shown in Figure 22. The offset voltage increases as common-mode voltage exceeds (V+) – 1 V. Common-mode rejection is specified from (V−) to (V+) – 1.3 V.

![Figure 22. Offset and Common-Mode Voltage](image)

7.3.3 Input and ESD Protection

The OPAx377-Q1 family incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the Absolute Maximum Ratings table.

Figure 23 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value must be kept to a minimum in noise-sensitive applications.

![Figure 23. Input Current Protection](image)
Feature Description (continued)

7.3.4 EMI Susceptibility and Input Filtering

Operational amplifiers vary in susceptibility to electromagnetic interference (EMI). If conducted EMI enters the operational amplifier, the dc offset observed at the amplifier output may shift from the nominal value while the EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The OPAx377-Q1 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. Both common-mode and differential mode filtering are provided by the input filter. The filter is designed for a cutoff frequency of approximately 75 MHz (–3 dB), with a roll-off of 20 dB per decade.

7.3.5 Capacitive Load and Stability

The OPAx377-Q1 series of amplifiers may be used in applications where driving a capacitive load is required. As with all op amps, there may be specific instances where the OPAx377-Q1 can become unstable, leading to oscillation. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier will be stable in operation. An op amp in the unity-gain (1 V/V) buffer configuration and driving a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the op amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases.

The OPAx377-Q1 in a unity-gain configuration can directly drive up to 250-pF pure capacitive load. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see the typical characteristic plot, Figure 15. In unity-gain configurations, capacitive load drive can be improved by inserting a small (10-Ω to 20-Ω) resistor, R_s, in series with the output, as shown in Figure 24. This resistor significantly reduces ringing while maintaining dc performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created, introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_s/R_L, and is generally negligible at low output current levels.

![Figure 24. Improving Capacitive Load Drive](image)

7.4 Device Functional Modes

The OPAx377-Q1 has a single functional mode and is operational when the power-supply voltage is greater than 2.2 V (±1.1 V). The maximum power supply voltage for the OPAx376-Q1 is 5.5 V (±2.75 V).
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPAX377-Q1 family of operational amplifiers is built on a precision analog CMOS technology featuring low noise and low offset voltage. The OPAX377-Q1 family delivers excellent offset voltage (250 μV, typical). Additionally, the amplifier boasts a fast slew rate, low drift, low noise, and excellent PSRR and $A_{\text{OL}}$. These 5.5-MHz CMOS op amps operate on 760 μA (typical) quiescent current.

8.2 Typical Application

Low-pass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The OPA377-Q1 is ideally suited to construct high-speed, high-precision active filters. Figure 25 shows a second-order, low-pass filter commonly encountered in signal processing applications.

8.2.1 Design Requirements

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain)
- Low-pass cutoff frequency = 25 kHz
- Second-order Chebyshev filter response with 3-dB gain peaking in the passband

8.2.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in Figure 25. Use Equation 1 to calculate the voltage transfer function.

\[
\frac{\text{Output}(s)}{\text{Input}} = \frac{-1/R_4 R_3 C_2 C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3 R_4 C_2 C_5}
\]  

This circuit produces a signal inversion. For this circuit, the gain at dc and the low-pass cutoff frequency are calculated by Equation 2:

\[
\text{Gain} = \frac{R_4}{R_1}
\]

\[
f_C = \frac{1}{2\pi} \sqrt{\frac{1}{R_3 R_4 C_2 C_5}}
\]

Software tools are readily available to simplify filter design. WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI’s vendor partners.

Figure 25. Typical Application Schematic
Typical Application (continued)

Available as a web-based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows to design, optimize, and simulate complete multi-stage active filter solutions within minutes.

8.2.3 Application Curve

Figure 26. Low-Pass Filter Transfer Function
9 Power Supply Recommendations

The OPAx377-Q1 family of devices is specified for operation from 2.2 V to 5.5 V (±1.1 V to ±2.75 V); many specifications apply from −40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the Typical Characteristics section.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.

- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to the application report, Circuit Board Layout Techniques, SLOA089.

- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.

- Place the external components as close to the device as possible. As shown in Figure 28, keeping RF and RG close to the inverting input minimizes parasitic capacitance.

- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.

- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

- Cleaning the PCB following board assembly is recommended for best performance.

10.2 Layout Example

![Figure 27. Typical Schematic for PCB Layout Example](image-url)
Layout Example (continued)

Run the input traces as far away from the supply lines as possible.

Use a low-ESR, ceramic bypass capacitor.

Place components close to the device and to each other to reduce parasitic errors.

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Figure 28. Typical PCB Layout Example
11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE
These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

11.1.1.2 DIP Adapter EVM

The DIP Adapter EVM tool provides an easy, low-cost way to prototype small surface mount ICs. The evaluation tool these TI packages: D or U (SOIC-8), PW (TSSOP-8), DGK (MSOP-8), DBV (SOT23-6, SOT23-5 and SOT23-3), DCK (SC70-6 and SC70-5), and DRL (SOT563-6). The DIP Adapter EVM may also be used with terminal strips or may be wired directly to existing circuits.

11.1.1.3 Universal Op Amp EVM

The Universal Op Amp EVM is a series of general-purpose, blank circuit boards that simplify prototyping circuits for a variety of IC package types. The evaluation module board design allows many different circuits to be constructed easily and quickly. Five models are offered, with each model intended for a specific package type. PDIP, SOIC, MSOP, TSSOP and SOT23 packages are all supported.

NOTE
These boards are unpopulated, so users must provide their own ICs. TI recommends requesting several op amp device samples when ordering the Universal Op Amp EVM.

11.1.1.4 TI Precision Designs

TI Precision Designs are analog solutions created by TI’s precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI Precision Designs are available online at http://www.ti.com/ww/en/analog/precision-designs/.

11.1.1.5 WEBENCH® Filter Designer

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI’s vendor partners.

Available as a web-based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.
11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- Circuit Board Layout Techniques, SLOA089
- Operational Amplifier Gain stability, Part 3: AC Gain-Error Analysis, SLYT383
- Operational Amplifier Gain Stability, Part 2: DC Gain-Error Analysis, SLYT374
- Op Amp Performance Analysis, SBOS054
- Shelf-Life Evaluation of Lead-Free Component Finishes, SZZA046
- Single-Supply Operation of Operational Amplifiers, SBOA059
- Tuning in Amplifiers, SBOA067
- Using Infinite-Gain, MFB Filter Topology in Fully Differential Active Filters, SLYT343

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI’s views; see TI's Terms of Use.

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

TINA-TI, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
TINA, DesignSoft are trademarks of DesignSoft, Inc.

11.5 Electrostatic Discharge Caution

⚠️ These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary.*
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## Packaging Information

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>PINS</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
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<td>DGK</td>
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<td>Level-2-260C-1 YEAR</td>
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<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>4377Q</td>
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(1) The marketing status values are defined as follows:
- **ACTIVE:** Product device recommended for new designs.
- **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.
- **TBD:** The Pb-Free/Green conversion plan has not been defined.
- **Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
- **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
- **Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and
continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA2377-Q1, OPA377-Q1, OPA4377-Q1:

- Catalog: OPA2377, OPA377, OPA4377

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
## TAPE AND REEL INFORMATION

### TAPE DIMENSIONS

![Diagram of TAPE DIMENSIONS]

<table>
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<tr>
<th>Device</th>
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<td>12.0</td>
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</table>

*Dimension designed to accommodate the component width*
*Dimension designed to accommodate the component length*
*Dimension designed to accommodate the component thickness*
*Overall width of the carrier tape*
*Pitch between successive cavity centers*

### REEL DIMENSIONS

![Diagram of REEL DIMENSIONS]

*All dimensions are nominal.*
<table>
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<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
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*All dimensions are nominal*
NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.

B. This drawing is subject to change without notice.

⚠️ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 each side.

⚠️ Body width does not include interlead flash. Interlead flash shall not exceed 0.25 each side.

E. Falls within JEDEC MO–153
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
NOTES:  
A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.  
D. Falls within JEDEC MO-178 Variation AA.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
DGK (S-PDSO-G8)  PLASTIC SMALL-OUTLINE PACKAGE

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
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