1 Features

- Wide Supply Voltage Range: 1.8 V to 18 V
- Adjustable Threshold: Down to 400 mV
- High Threshold Accuracy:
  - 0.5% Max at 25°C
  - 1.0% Max Over Temperature
- Low Quiescent Current: 5.5 µA (Typ)
- Open-Drain Output
- Internal Hysteresis: 5.5 mV (Typ)
- Temperature Range: –40°C to +125°C
- Package: Thin SOT-23-6

2 Applications

- Notebook PCs and Tablets
- Smartphones
- Digital Cameras
- Video Game Controllers
- Relays and Circuit Breakers
- Portable Medical Devices
- Door and Window Sensors
- Portable- and Battery-Powered Products

3 Description

The TLV6703 high voltage comparator operates over a 1.8-V to 18-V range. The TLV6703 has a high-accuracy comparator with an internal 400-mV reference and an open-drain output rated to 18 V for precision voltage detection. The monitored voltage can be set with the use of external resistors.

The OUT pin is driven low when the voltage at the SENSE pin drops below \(V_{IT-}\), and goes high when the voltage returns above the respective threshold \(V_{IT+}\). The comparator in the TLV6703 includes built-in hysteresis for filtering to reject brief glitches, thereby ensuring stable output operation without false triggering.

The TLV6703 is available in a Thin SOT-23-6 package and is specified over the junction temperature range of –40°C to +125°C.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLV6703</td>
<td>SOT-23-6</td>
<td>2.90 mm × 1.60 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the package option addendum at the end of the datasheet.
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4 Revision History

Changes from Original (January 2018) to Revision A Page
  • Changed Advance Information to Production Data ......................... 1

5 Device Comparison Table

Table 1. TLV67xx Integrated Comparator Family

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>CONFIGURATION</th>
<th>OPERATING VOLTAGE RANGE</th>
<th>THRESHOLD ACCURACY OVER TEMPERATURE</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLV6700</td>
<td>Window</td>
<td>1.8 V to 18 V</td>
<td>1%</td>
</tr>
<tr>
<td>TLV6703</td>
<td>Non-Inverting Single Channel</td>
<td>1.8 V to 18 V</td>
<td>1%</td>
</tr>
<tr>
<td>TLV6710</td>
<td>Window</td>
<td>1.8 V to 36 V</td>
<td>0.75%</td>
</tr>
<tr>
<td>TLV6713</td>
<td>Non-Inverting Single Channel</td>
<td>1.8 V to 36 V</td>
<td>0.75%</td>
</tr>
</tbody>
</table>
## 6 Pin Configuration and Functions

### Pin Functions

<table>
<thead>
<tr>
<th>PIN NAME</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td>2, 4, 6</td>
<td>Connect all three pins to ground.</td>
</tr>
<tr>
<td>OUT</td>
<td>1</td>
<td>SENSE comparator open-drain output. OUT is driven low when the voltage at this comparator is below (V_{IT-}). The output goes high when the sense voltage returns above the respective threshold (V_{IT+}).</td>
</tr>
<tr>
<td>SENSE</td>
<td>3</td>
<td>This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this pin drops below the threshold voltage (V_{IT-}), OUT is driven low.</td>
</tr>
<tr>
<td>VDD</td>
<td>5</td>
<td>Supply voltage input. Connect a 1.8-V to 18-V supply to VDD to power the device. Good analog design practice is to place a 0.1-µF ceramic capacitor close to this pin.</td>
</tr>
</tbody>
</table>

![DDC Package 6-Pin SOT Top View](image-url)
7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Voltage(2)</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>–0.3</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>OUT</td>
<td>–0.3</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>SENSE</td>
<td>–0.3</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>Current</td>
<td>OUT (output sink current)</td>
<td>40</td>
<td>mA</td>
</tr>
<tr>
<td>Temperature</td>
<td>Operating junction, Tj</td>
<td>–40</td>
<td>125 °C</td>
</tr>
<tr>
<td></td>
<td>Storage, Tstg</td>
<td>–65</td>
<td>150 °C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to network ground pin.

7.2 ESD Ratings

<table>
<thead>
<tr>
<th>V(ESD)</th>
<th>Electrostatic discharge</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins</td>
<td>±2500</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Charged device model (CDM), per JEDEC specification JESD22-C101, all pins</td>
<td>±1000</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Voltage</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>1.8</td>
<td></td>
<td>18</td>
<td>V</td>
</tr>
<tr>
<td>V_i</td>
<td>0</td>
<td></td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td>V_O</td>
<td>0</td>
<td></td>
<td>18</td>
<td>V</td>
</tr>
</tbody>
</table>

7.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC (1)</th>
<th>TLV6703 DDC (SOT)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_{JA}</td>
<td>204.6</td>
<td>°C/W</td>
</tr>
<tr>
<td>R_{JC(top)}</td>
<td>50.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>R_{JB}</td>
<td>54.3</td>
<td>°C/W</td>
</tr>
<tr>
<td>Ψ_{JT}</td>
<td>0.8</td>
<td>°C/W</td>
</tr>
<tr>
<td>Ψ_{JB}</td>
<td>52.8</td>
<td>°C/W</td>
</tr>
<tr>
<td>R_{JC(bot)}</td>
<td>N/A</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor an IC Package Thermal Metrics application report.

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Product Folder Links: TLV6703
### 7.5 Electrical Characteristics

Over the operating temperature range of $T_J = -40^\circ C$ to $+125^\circ C$, and $1.8 \, V < V_{DD} < 18 \, V$ (unless otherwise noted). Typical values are at $T_J = 25^\circ C$ and $V_{DD} = 5 \, V$.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{(POR)}$</td>
<td>Power-on reset voltage $(1)$</td>
<td>$V_{OL,max} = 0.2 , V$, output sink current = $15 , \mu A$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IT+}$</td>
<td>Positive-going input threshold voltage</td>
<td>$V_{DD} = 1.8 , V$ and $18 , V$, $T_J = 25^\circ C$</td>
<td>398</td>
<td>400</td>
<td>402.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 1.8 , V$ and $18 , V$, $T_J = -40^\circ C$ to $125^\circ C$</td>
<td>396</td>
<td></td>
<td>404</td>
</tr>
<tr>
<td>$V_{IT-}$</td>
<td>Negative-going input threshold voltage</td>
<td>$V_{DD} = 1.8 , V$ and $18 , V$, $T_J = 25^\circ C$</td>
<td>391.6</td>
<td>394.5</td>
<td>397.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 1.8 , V$ and $18 , V$, $T_J = -40^\circ C$ to $125^\circ C$</td>
<td>387</td>
<td></td>
<td>400</td>
</tr>
<tr>
<td>$V_{hys}$</td>
<td>Hysteresis voltage ($hys = V_{IT+} - V_{IT-}$)</td>
<td></td>
<td>5.5</td>
<td></td>
<td>12</td>
</tr>
<tr>
<td>$I_{(SENSE)}$</td>
<td>Input current (at the SENSE pin)</td>
<td>$V_{DD} = 1.8 , V$ and $18 , V$, $V_I = 6.5 , V$</td>
<td></td>
<td>-25</td>
<td>1</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low-level output voltage</td>
<td>$V_{DD} = 1.3 , V$, output sink current = $0.4 , mA$</td>
<td></td>
<td></td>
<td>250</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 1.8 , V$, output sink current = $3 , mA$</td>
<td></td>
<td></td>
<td>250</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 5 , V$, output sink current = $5 , mA$</td>
<td></td>
<td></td>
<td>250</td>
</tr>
<tr>
<td>$I_{(OD)}$</td>
<td>Open-drain output leakage-current</td>
<td>$V_{DD} = 1.8 , V$ and $18 , V$, $V_O = V_{DD}$</td>
<td></td>
<td></td>
<td>300</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 1.8 , V$, $V_O = 18 , V$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{DD}$</td>
<td>Supply current</td>
<td>$V_{DD} = 1.8 , V$, no load</td>
<td>5.5</td>
<td></td>
<td>11</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 5 , V$</td>
<td></td>
<td>6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 12 , V$</td>
<td></td>
<td>6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 18 , V$</td>
<td></td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>UVLO</td>
<td>Undervoltage lockout $(2)$</td>
<td>$V_{DD}$ failing</td>
<td>1.3</td>
<td></td>
<td>1.7</td>
</tr>
</tbody>
</table>

$(1)$ The lowest supply voltage ($V_{DD}$) at which output is active; $t_{(VDD)} > 15 \, \mu s/V$. Below $V_{(POR)}$, the output cannot be determined.

$(2)$ When $V_{DD}$ falls below UVLO, OUT is driven low. The output cannot be determined below $V_{(POR)}$. 

---

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7.6 Timing Requirements
over operating temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{pd(HL)} ) High-to-low propagation delay (^{(1)})</td>
<td>( V_{DD} = 5 ) ( V ), 10-mV input overdrive, ( R_P = 10 ) ( k\Omega ), ( V_{OH} = 0.9 \times V_{DD} ), ( V_{OL} = 400 ) ( mV ), see Figure 1</td>
<td>18</td>
<td></td>
<td></td>
<td>( \mu s )</td>
</tr>
<tr>
<td>( t_{pd(LH)} ) Low-to-high propagation delay (^{(1)})</td>
<td>( V_{DD} = 5 ) ( V ), 10-mV input overdrive, ( R_P = 10 ) ( k\Omega ), ( V_{OH} = 0.9 \times V_{DD} ), ( V_{OL} = 400 ) ( mV ), see Figure 1</td>
<td>29</td>
<td></td>
<td></td>
<td>( \mu s )</td>
</tr>
<tr>
<td>( t_{d(start)} ) Start-up delay (^{(2)})</td>
<td></td>
<td>150</td>
<td></td>
<td></td>
<td>( \mu s )</td>
</tr>
</tbody>
</table>

(1) High-to-low and low-to-high refers to the transition at the input pin (SENSE).
(2) During power on, \( V_{DD} \) must exceed 1.8 \( V \) for at least 150 \( \mu s \) before the output is in a correct state.

7.7 Switching Characteristics
over operating temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_r ) Output rise time</td>
<td>( V_{DD} = 5 ) ( V ), 10-mV input overdrive, ( R_P = 10 ) ( k\Omega ), ( V_O = (0.1 ) to ( 0.9) \times V_{DD} )</td>
<td>2.2</td>
<td></td>
<td></td>
<td>( \mu s )</td>
</tr>
<tr>
<td>( t_f ) Output fall time</td>
<td>( V_{DD} = 5 ) ( V ), 10-mV input overdrive, ( R_P = 10 ) ( k\Omega ), ( V_O = (0.1 ) to ( 0.9) \times V_{DD} )</td>
<td>0.22</td>
<td></td>
<td></td>
<td>( \mu s )</td>
</tr>
</tbody>
</table>

![Figure 1. Timing Diagram](image-url)
7.8 Typical Characteristics

at $T_J = 25^\circ C$ and $V_{DD} = 5$ V (unless otherwise noted)

---

**Figure 2.** Supply Current ($I_{DD}$) vs Supply Voltage ($V_{DD}$)

**Figure 3.** Rising Input Threshold Voltage ($V_{IT+}$) vs Temperature

**Figure 4.** Hysteresis ($V_{hys}$) vs Temperature

**Figure 5.** Propagation Delay vs Temperature (High-to-Low Transition at Sense)

**Figure 6.** Propagation Delay vs Temperature (Low-to-High Transition at Sense)

**Figure 7.** Minimum Pulse Width vs Threshold Overdrive Voltage

---
Typical Characteristics (continued)

at $T_J = 25^\circ C$ and $V_{DD} = 5$ V (unless otherwise noted)

![Graph 1: Supply Current (Idd) vs Output Sink Current](image1)

![Graph 2: Output Voltage Low (VOL) vs Output Sink Current (–40°C)](image2)

![Graph 3: Output Voltage Low (VOL) vs Output Sink Current (0°C)](image3)

![Graph 4: Output Voltage Low (VOL) vs Output Sink Current (25°C)](image4)

![Graph 5: Output Voltage Low (VOL) vs Output Sink Current (85°C)](image5)

![Graph 6: Output Voltage Low (VOL) vs Output Sink Current (125°C)](image6)
8 Detailed Description

8.1 Overview

The TLV6703 provides precision voltage detection. The TLV6703 is a wide-supply voltage range (1.8 V to 18 V) comparator with a high-accuracy rising input threshold of 400 mV (1% over temperature) and built-in hysteresis. The output is also rated to 18 V, independent of supply voltage, and can sink up to 40 mA.

The TLV6703 asserts the output signal, as shown in Table 2. To monitor any voltage above 0.4 V, set the input using an external resistor divider network. Each input pin has very low input leakage current, allowing the use of large resistor dividers without sacrificing system accuracy. Broad voltage thresholds are supported that enable the device for use in a wide array of applications.

Table 2. TLV6703 Truth Table

<table>
<thead>
<tr>
<th>CONDITION</th>
<th>OUTPUT</th>
<th>OUTPUT STATE</th>
</tr>
</thead>
<tbody>
<tr>
<td>SENSE &gt; V_{IT+}</td>
<td>OUT high</td>
<td>Output high impedance</td>
</tr>
<tr>
<td>SENSE &lt; V_{IT-}</td>
<td>OUT low</td>
<td>Output sinking</td>
</tr>
</tbody>
</table>

8.2 Functional Block Diagram

![Diagram of TLV6703 Functional Block Diagram]
8.3 Feature Description

8.3.1 Input Pin (SENSE)

The TLV6703 comparator has two inputs: one external input, and one input internally connected to the internal 400mV reference. The comparator rising threshold is trimmed to be equal to the reference voltage (400 mV). The comparator also has a built-in falling hysteresis that makes the device less sensitive to supply-rail noise and provides stable operation.

The comparator input (SENSE) is able to swing from ground to 6.5 V, regardless of the device supply voltage. Although not required in most cases, to reduce sensitivity to transients and layout parasitics for extremely noisy applications, place a 1-nF to 10-nF bypass capacitor at the comparator input.

OUT is driven to logic low when the input SENSE voltage drops below \( V_{\text{IT-}} \). When the voltage exceeds \( V_{\text{IT+}} \), the output (OUT) goes to a high-impedance state; see Figure 1.

8.3.2 Output Pin (OUT)

In a typical TLV6703 application, the output is connected to a GPIO input of the processor (such as a digital signal processor [DSP], central processing unit [CPU], field-programmable gate array [FPGA], or application-specific integrated circuit [ASIC]).

The TLV6703 device provides an open-drain output (OUT). Use a pullup resistor to hold this line high when the output goes to high impedance (not asserted). To connect the output to another device at the correct interface-voltage level, connect a pullup resistor to the proper voltage rail. The TLV6703 output can be pulled up to 18 V, independent of the device supply voltage.

Table 2 and the Input Pin (SENSE) section describe how the output is asserted or deasserted. See Figure 1 for a timing diagram that describes the relationship between threshold voltage and the respective output.

8.3.3 Immunity to Input-Pin Voltage Transients

The TLV6703 is relatively immune to short voltage transient spikes on the sense pin. Sensitivity to transients depends on both transient duration and amplitude; see Figure 7, Minimum Pulse Width vs Threshold Overdrive Voltage.

8.4 Device Functional Modes

8.4.1 Normal Operation (\( V_{\text{DD}} > \) UVLO)

When the voltage on \( V_{\text{DD}} \) is greater than 1.8 V for at least 150 µs, the OUT signal correspond to the voltage on SENSE as listed in Table 2.

8.4.2 Undervoltage Lockout (\( V_{\text{(POR)}} < V_{\text{DD}} < \) UVLO)

When the voltage on \( V_{\text{DD}} \) is less than the device UVLO voltage, and greater than the power-on reset voltage, \( V_{\text{(POR)}} \), the OUT signal is asserted regardless of the voltage on SENSE.

8.4.3 Power-On Reset (\( V_{\text{DD}} < V_{\text{(POR)}} \))

When the voltage on \( V_{\text{DD}} \) is lower than the required voltage to internally pull the asserted output to GND \( (V_{\text{(POR)}}) \), SENSE is in a high-impedance state.
9 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information
The TLV6703 device is a wide-supply voltage comparator that operates over a $V_{DD}$ range of 1.8 V to 18 V. The device has a high-accuracy comparator with an internal 400-mV reference and an open-drain output rated to 18 V for precision voltage detection. The device can be used as a voltage monitor. The monitored voltage are set with the use of external resistors.

9.1.1 $V_{PULLUP}$ to a Voltage Other Than $V_{DD}$
The output is often tied to $V_{DD}$ through a resistor. However, some applications may require the output to be pulled up to a higher or lower voltage than $V_{DD}$ to correctly interface with the reset and enable pins of other devices.

Figure 14. Interfacing to a Voltage Other Than $V_{DD}$
Application Information (continued)

9.1.2 Monitoring $V_{DD}$

Many applications monitor the same rail that is powering $V_{DD}$. In these applications the resistor divider is simply connected to the $V_{DD}$ rail.

![Diagram of monitoring the same voltage as $V_{DD}$](image)

Figure 15. Monitoring the Same Voltage as $V_{DD}$

9.1.3 Monitoring a Voltage Other Than $V_{DD}$

Some applications monitor rails other than the one that is powering $V_{DD}$. In these types of applications the resistor divider used to set the desired threshold is connected to the rail that is being monitored.

![Diagram of monitoring a voltage other than $V_{DD}$](image)

NOTE: The input can monitor a voltage greater than maximum $V_{DD}$ with the use of an external resistor divider network.

Figure 16. Monitoring a Voltage Other Than $V_{DD}$
9.2 Typical Application

The TLV6703 device is a wide-supply voltage comparator that operates over a $V_{DD}$ range of 1.8 to 18 V. The monitored voltage is set with the use of external resistors, so the device can be used either as a precision voltage monitor.

![Wide VIN Voltage Monitor](image)

Figure 17. Wide VIN Voltage Monitor

9.2.1 Design Requirements

For this design example, use the values summarized in Table 3 as the input parameters.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>DESIGN REQUIREMENT</th>
<th>DESIGN RESULT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Monitored voltage</td>
<td>12-V nominal rail with maximum falling threshold of 10%</td>
<td>$V_{MON(UV)} = 10.99$ V (8.33%)</td>
</tr>
</tbody>
</table>

9.2.2 Detailed Design Procedure

9.2.2.1 Resistor Divider Selection

The resistor divider values and target threshold voltage can be calculated by using Equation 1 to determine $V_{MON(UV)}$:

$$V_{MON(UV)} = \left( 1 + \frac{R_1}{R_2} \right) \times V_{IT-}$$

where

- $R_1$ and $R_2$ are the resistor values for the resistor divider on the SENSEx pins
- $V_{MON(UV)}$ is the target voltage at which an undervoltage condition is detected

Choose $R_{TOTAL}$ ($= R_1 + R_2$) so that the current through the divider is approximately 100 times higher than the input current at the SENSE pin. The resistors can have high values to minimize current consumption as a result of low input bias current without adding significant error to the resistive divider. For details on sizing input resistors, refer to application report SLVA450, Optimizing Resistor Dividers at a Comparator Input, available for download from www.ti.com.
9.2.2.2 Pullup Resistor Selection

To ensure the proper voltage level, the pullup resistor value is selected by ensuring that the pullup voltage divided by the resistor does not exceed the sink-current capability of the device. This confirmation is calculated by verifying that the pullup voltage minus the output-leakage current \( I_{\text{lkg(OD)}} \) multiplied by the resistor is greater than the desired logic-high voltage. These values are specified in the Electrical Characteristics.

Use Equation 2 to calculate the value of the pullup resistor.

\[
\frac{V_{\text{Hi}} - V_{\text{PU}}}{I_{\text{lkg(OD)}}} \geq R_{\text{PU}} \geq \frac{V_{\text{PU}}}{I_{O}}
\]

(2)

9.2.2.3 Input Supply Capacitor

Although an input capacitor is not required for stability, for good analog design practice, connect a 0.1-\(\mu\)F low equivalent series resistance (ESR) capacitor across the VDD and GND pins. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source.

9.2.2.4 Sense Capacitor

Although not required in most cases, for extremely noisy applications, place a 1-nF to 10-nF bypass capacitor from the comparator input (SENSE) to the GND pin for good analog design practice. This capacitor placement reduces device sensitivity to transients.

9.2.3 Application Curves

![Figure 18. Rising Input Threshold Voltage (V_{IT+}) vs Temperature](image)

9.3 Dos and Don'ts

Do connect a 0.1-\(\mu\)F decoupling capacitor from VDD to GND for best system performance.

If the monitored rail is noisy, do connect a decoupling capacitor from the comparator input (sense) to GND.

Don't use resistors for the voltage divider that cause the current through them to be less than 100 times the input current of the comparator without also accounting for the effect to the accuracy.

Don't use a pullup resistor that is too small, because the larger current sunk by the output then exceeds the desired low-level output voltage \(V_{\text{OL}}\).
10 Power-Supply Recommendations
These devices operate from an input voltage supply range between 1.8 V and 18 V.

11 Layout

11.1 Layout Guidelines
Placing a 0.1-µF capacitor close to the VDD pin to reduce the input impedance to the device is good analog design practice.

11.2 Layout Example

![Layout Example Diagram]

Figure 19. Layout Example
12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support
The DIP Adapter Evaluation Module allows conversion of the SOT-23-6 package to a standard DIP-6 pinout for ease of prototyping and bench evaluation.

12.2 Receiving Notification of Documentation Updates
To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2ETM Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks
E2E is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary
SLYZ022 — TI Glossary.
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLV6703DDCR</td>
<td>ACTIVE</td>
<td>SOT-23-THIN</td>
<td>DDC</td>
<td>6</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>1MR1</td>
<td></td>
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<tr>
<td>TLV6703DDCT</td>
<td>ACTIVE</td>
<td>SOT-23-THIN</td>
<td>DDC</td>
<td>6</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>1MR1</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE:** Product device recommended for new designs.
- **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
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<td>8.4</td>
<td>3.2</td>
<td>3.2</td>
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<td>8.0</td>
<td>Q3</td>
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<tr>
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<td>250</td>
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<td>3.2</td>
<td>3.2</td>
<td>1.4</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
</tbody>
</table>
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
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<tr>
<th>Device</th>
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<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
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<th>Height (mm)</th>
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<tbody>
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<td>200.0</td>
<td>45.0</td>
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</tbody>
</table>
NOTES:
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

7. Board assembly site may have different recommendations for stencil design.
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