Voltage-to-Frequency and Frequency-to-Voltage CONVERTER

FEATURES

- HIGH LINEARITY: 12 to 14 bits
  ±0.005% max at 10kHz FS
  ±0.03% max at 100kHz FS
  ±0.1% typ at 1MHz FS
- V/F OR F/V CONVERSION
- 6-DECADE DYNAMIC RANGE
- GAIN DRIFT: 20ppm/°C max
- OUTPUT TTL/CMOS COMPATIBLE

APPLICATIONS

- INEXPENSIVE A/D AND D/A CONVERTER
- DIGITAL PANEL METERS
- TWO-WIRE DIGITAL TRANSMISSION WITH NOISE IMMUNITY
- FM MOD/DEMOD OF TRANSDUCER SIGNALS
- PRECISION LONG TERM INTEGRATOR
- HIGH RESOLUTION OPTICAL LINK FOR ISOLATION
- AC LINE FREQUENCY MONITOR
- MOTOR SPEED MONITOR AND CONTROL

DESCRIPTION

The VFC320 monolithic voltage-to-frequency and frequency-to-voltage converter provides a simple low cost method of converting analog signals into digital pulses. The digital output is an open collector and the digital pulse train repetition rate is proportional to the amplitude of the analog input voltage. Output pulses are compatible with TTL, and CMOS logic families.

High linearity (0.005%, max at 10kHz FS) is achieved with relatively few external components. Two external resistors and two external capacitors are required to operate. Full scale frequency and input voltage are determined by a resistor in series with –In and two capacitors (one-shot timing and input amplifier integration). The other resistor is a non-critical open collector pull-up (fOUT to +VCC). The VFC320 is available in two performance grades. The VFC320 is specified for the –25°C to +85°C, range.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
ELECTRICAL CHARACTERISTICS

At $T_A = +25^\circ$C and ±15VDC power supply, unless otherwise noted.

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* Specification the same as for VFC320BP.

NOTES: (1) A 25% duty cycle at full scale (0.25mA input current) is recommended where possible to achieve best linearity. (2) Determined by $R_N$ and full scale current range constraints. (3) Adjustable to zero. See Offset and Gain Adjustment section. (4) Linearity error at any operating frequency is defined as the deviation from a straight line drawn between the full scale frequency and 0.1% of full scale frequency. See Discussion of Specifications section. (5) When offset and gain errors are nulled, at an operating temperature, the linearity error determines the final accuracy. (6) For $e_i = 0$ typical linearity errors are: 0.01% at 10kHz, 0.2% at 100kHz, 0.1% at 1MHz. (7) Exclusive of external components’ drift. (8) FSR = Full Scale Range (corresponds to full scale and full scale input voltage.) (9) Positive drift is defined to be increasing frequency with increasing temperature. (10) One pulse of new frequency plus 50ns typical.
ABSOLUTE MAXIMUM RATINGS

Supply Voltage ................................................................................... ±20V
Output Sink Current at f_OUT ............................................................... 50mA
Output Current at V_OUT ..................................................................... ±20mA
Input Voltage, −Input ......................................................................... ±V_{CC}
Input Voltage, +Input ......................................................................... ±V_{CC}
Storage Temperature Range ......................................................... −65°C to +150°C
Lead Temperature (soldering, 10s) ......................................................... +300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

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NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of “VFC320BP/2K5” will get a single 2500-piece Tape and Reel.

PIN CONFIGURATION

Top View

![Pin Configuration Diagram]
DISCUSSION OF SPECIFICATIONS

LINEARITY

Linearity is the maximum deviation of the actual transfer function from a straight line drawn between the end points (100% full scale input or frequency and 0.1% of full scale called zero.) Linearity is the most demanding measure of voltage-to-frequency converter performance, and is a function of the full scale frequency. Refer to Figure 1 to determine typical linearity error for your application. Once the full scale frequency is chosen, the linearity is a function of operating frequency as it varies between zero and full scale. Examples for 10kHz full scale are shown in Figure 2. Best linearity is achieved at lower gains (Δf_{OUT}/ΔV_{IN}) with operation as close to the chosen full scale frequency as possible.

The high linearity of the VFC320 makes the device an excellent choice for use as the front end of Analog-to-Digital (A/D) converters with 12- to 14-bit resolution, and for highly accurate transfer of analog data over long lines in noisy environments (2-wire digital transmission.)

FREQUENCY STABILITY VS TEMPERATURE

The full scale frequency drift of the VFC320 versus temperature is expressed as parts per million of full scale range per °C. As shown in Figure 3, the drift increases above 10kHz. To determine the total accuracy drift over temperature, the drift coefficients of external components (especially R_{1} and C_{1}) must be added to the drift of the VFC320.

THEORY OF OPERATION

The VFC320 monolithic voltage-to-frequency converter provides a digital pulse train output whose repetition rate is directly proportional to the analog input voltage. The circuit shown in Figure 4 is composed of an input amplifier, two comparators and a flip-flop (forming a on-shot), two switched current sinks, and an open collector output transistor stage. Essentially the input amplifier acts as an integrator that produces a two-part ramp. The first part is a function of the input voltage, and the second part is dependent on the input voltage and current sink. When a positive input voltage is applied at VIN, a current will flow through the input resistor, causing the voltage at VOUT to ramp down toward zero, according to \( \frac{dV}{dt} = \frac{V_{IN}}{R_{1}C_{1}} \). During this time the constant current sink is disabled by the switch. Note, this period is only dependent on VIN and the integrating components.

When the ramp reaches a voltage close to zero, comparator A sets the flip-flop. This closes the current sink switches as well as changing f_{OUT} from logic 0 to logic 1. The ramp now begins to ramp up, and 1mA charges through C_{1} until V_{C1} = −7.5V. Note this ramp period is dependent on the 1mA current sink, connected to the negative input of the op amp, as well as the input voltage. At this −7.5V threshold point C_{1}, comparator B resets the flip-flop, and the ramp voltage...
In the time \( t_1 + t_2 \) the integrator capacitor \( C_2 \) charges and discharges but the net voltage change is zero.

Thus \( \Delta Q = 0 = I_{IN} t_1 + (I_{IN} - I_A) t_2 \) 

So that \( I_{IN} (t_1 + t_2) = I_A t_2 \)

But since \( t_1 + t_2 = \frac{1}{f_{OUT}} \) and \( I_{IN} = \frac{V_{IN}}{R_1} \) \( \text{(4), (5)} \)

\( f_{OUT} = \frac{V_{IN}}{I_A R_2} \frac{1}{R_2} \)

In the time \( t_1 \), \( I_B \) charges the one-shot capacitor \( C_1 \) until its voltage reaches \(-7.5V\) and trips comparator B.

Thus \( t_2 = \frac{C_{IN} 7.5}{I_B} \) \( \text{(7)} \)

Using (7) in (6) yield \( f_{OUT} = \frac{V_{IN}}{7.5 R_1 C_1} \cdot \frac{I_B}{I_A} \) \( \text{(8)} \)

Since \( I_A = I_B \) the result is

\( f_{OUT} = \frac{V_{IN}}{7.5 R_1 C_1} \) \( \text{(9)} \)

Since the integrating capacitor, \( C_2 \), affects both the rising and falling segments of the ramp voltage, its tolerance and temperature coefficient do not affect the output frequency. It should, however, have a leakage current that is small compared to \( I_{IN} \), since this parameter will add directly to the gain error of the VFC. \( C_1 \), which controls the one-shot period, should be very precise since its tolerance and temperature coefficient add directly to the errors in the transfer function.
The operation of the VFC320 as a highly linear frequency-to-voltage converter, follows the same theory of operation as the voltage-to-frequency converter. \( e_1 \) and \( e_2 \) are shorted and \( F_{\text{IN}} \) is disconnected from \( V_{\text{OUT}} \). \( F_{\text{IN}} \) is then driven with a signal which is sufficient to trigger comparator A. The one-shot period will then be determined by \( C_1 \) as before, but the cycle repetition frequency will be dictated by the digital input at \( F_{\text{IN}} \).

**DUTY CYCLE**

The duty cycle (D) of the VFC is the ratio of the one-shot period (\( t_2 \)) or pulse width, PW, to the total VFC period (\( t_1 + t_2 \)). For the VFC320, \( t_2 \) is fixed and \( t_1 + t_2 \) varies as the input voltage. Thus the duty cycle, D, is a function of the input voltage. Of particular interest is the duty cycle at full scale frequency, \( D_{FS} \), which occurs at full scale input. \( D_{FS} \) is a user determined parameter which affects linearity.

\[
D_{FS} = \frac{t_2}{t_1 + t_2} = PW \cdot f_{FS}
\]

Best linearity is achieved when \( D_{FS} \) is 25%. By reducing equations (7) and (9) it can be shown that

\[
D_{FS} = \frac{V_{IN,\text{max}}}{R_1} = \frac{I_{IN,\text{max}}}{1\text{mA}}
\]

Thus \( D_{FS} = 0.25 \) corresponds to \( I_{IN,\text{max}} = 0.25\text{mA} \).

**INSTALLATION AND OPERATING INSTRUCTIONS**

**VOLTAGE-TO-FREQUENCY CONVERSION**

The VFC320 can be connected to operate as a V/F converter that will accept either positive or negative input voltages, or an input current. Refer to Figures 6 and 7.

**EXTERNAL COMPONENT SELECTION**

In general, the design sequence consists of: (1) choosing \( f_{\text{MAX}} \), (2) choosing the duty cycle at full scale \( (D_{FS} = 0.25 \text{ typically}) \), (3) determining the input resistor, \( R_1 \) (Figure 4), (4) calculating the one-shot capacitor, \( C_1 \), (5) selecting the integrator capacitor \( C_2 \), and (6) selecting the output pull-up resistor, \( R_2 \).

**Input Resistors \( R_1 \) and \( R_3 \)**

The input resistance \( (R_1 \) and \( R_3 \) in Figures 6 and 7) is calculated to set the desired input current at full scale input voltage. This is normally 0.25mA to provide a 25% duty cycle at full scale input and output. Values other than \( D_{FS} = 0.25 \) may be used but linearity will be affected.

The nominal value is \( R_1 \) is

\[
R_1 = \frac{V_{IN,\text{max}}}{0.25\text{mA}}
\]

If gain trimming is to be done, the nominal value is reduced by the tolerance of \( C_1 \) and the desired trim range. \( R_1 \) should have a very-low temperature coefficient since its drift adds directly to the errors in the transfer function.

**One-Shot Capacitor, \( C_1 \)**

This capacitor determines the duration of the one-shot pulse. From equation (9) the nominal value is

\[
C_{1,\text{NOM}} = \frac{V_{IN}}{7.5 \cdot R_1 \cdot f_{\text{OUT}}}
\]

For the usual 25% duty at \( f_{\text{MAX}} = V_{IN}/R_1 = 0.25\text{mA} \) there is approximately 15pF of residual capacitance so that the design value is

\[
C_1(pF) = \frac{33 \cdot 10^6}{f_{FS}} - 15
\]
where \( f_{FS} \) is the full scale output frequency in Hz. The temperature drift of \( C_1 \) is critical since it will add directly to the errors of the transfer function. An NPO ceramic type is recommended. Every effort should be made to minimize stray capacitance associated with \( C_1 \). It should be mounted as close to the VFC320 as possible. Figure 8 shows pulse width and full scale frequency for various values of \( C_1 \) at \( D_{FS} = 25\% \).

### Integrating Capacitor, \( C_2 \)

Since \( C_2 \) does not occur in the \( V/F \) transfer function equation (9), its tolerance and temperature stability are not important; however, leakage current in \( C_2 \) causes a gain error. A ceramic type is sufficient for most applications. The value of \( C_2 \) determines the amplitude of \( V_{OUT} \). Input amplifier saturation, noise levels for the comparators and slew rate limiting of the integrator determine a range of acceptable values:

\[
C_2 (\mu F) = \begin{cases} 
100/f_{FS}; & \text{if } f_{FS} \leq 100kHz \\
0.001; & \text{if } 100kHz < f_{FS} \leq 500kHz \\
0.0005; & \text{if } f_{FS} > 500kHz 
\end{cases} 
\]

### Output Pull Up Resistor \( R_2 \)

The open collector output can sink up to 8mA and still be TTL-compatible. Select \( R_2 \) according to this equation:

\[
R_2 \min (\Omega) = V_{PULLUP}/(8mA - I_{LOAD})
\]

A 10% carbon film resistor is suitable for use as \( R_2 \).

### Design Example

Given a full scale input of +10V, select the values of \( R_1, R_2, R_3, C_1, \) and \( C_2 \) for a 25% duty cycle at 100kHz maximum operation into one TTL load. See Figure 6.

**Selecting \( C_1 \) (\( D_{FS} = 0.25 \))**

\[
C_1 = [(33 \cdot 10^6)/f_{MAX}] - 15 \quad (13)
\]

if \( D_{FS} = 0.5 \)

\[
= [(66 \cdot 10^6)/f_{MAX}] - 15
\]

\[
= 315pF
\]

Choose a 300pF NPO ceramic capacitor with 1% to 10% tolerance.

**Selecting \( R_1 \) and \( R_3 \) (\( D_{RS} = 0.25 \))**

\[
R_1 + R_3 = V_{IN} \max /0.25mA \quad V_{IN} \max /0.5mA
\]

if \( D_{FS} = 0.5 \)

\[
= 10V/0.25mA
\]

\[
= 40k\Omega
\]

Choose 32.4k\( \Omega \) metal film resistor with 1% tolerance and \( R_3 = 10k\Omega \) cermet potentiometer.

**Selecting \( C_2 \)**

\[
C_2 = 10^2/f_{MAX}
\]

\[
= 10^2/100kHz
\]

\[
= 0.001\mu F
\]

Choose a 0.001\( \mu F \) capacitor with \( \pm 5\% \) tolerance.
Selecting $R_2$

$$R_2 = \frac{V_{\text{PULLUP}}(8\text{mA} - I_{\text{LOAD}})}{8\text{mA} - 1.6\text{mA}}$$

$$= \frac{5\text{V}}{8\text{mA} - 1.6\text{mA}} = 781\Omega$$

Choose a 750$\Omega$ 1/4-watt carbon compensation resistor with ±5% tolerance.

FREQUENCY-TO-VOLTAGE CONVERSION

To operate the VFC320 as a frequency-to-voltage converter, connect the unit as shown in Figure 9. To interface with TTL-logic, the input should be coupled through a capacitor, and the input to pin 10 biased near +2.5V. The converter will detect the falling edges of the input pulse train as the voltage at pin 10 crosses zero. Choose $C_3$ to make $t = 0.1t$ (see Figure 9). For input signals with amplitudes less than 5V, pin 10 should be biased closer to zero to insure that the input signal at pin 10 crosses the zero threshold.

Errors are nulled using $0.001 \cdot$ full scale frequency to null offset, and full scale frequency to null the gain error. The procedure is given on this page. Use equations from V/F calculations to find $R_1$, $R_3$, $R_4$, $C_1$, and $C_2$.

TYPICAL APPLICATIONS

Excellent linearity, wide dynamic range, and compatible TTL, DTL, and CMOS digital output make the VFC320 ideal for a variety of VFC applications. High accuracy allows the VFC320 to be used where absolute or exact readings must be made. It is also suitable for systems requiring high resolution up to 14 bits. Figures 10-14 show typical applications of the VFC320.
FIGURE 12. Remote Transducer Readout via Fiber Optic Link (Analog and Digital Output).

FIGURE 13. Bipolar input is accomplished by offsetting the input to the VFC with a reference voltage. Accurately matched resistors in the REF101 provide a stable half-scale output frequency at zero volts input.

FIGURE 14. Absolute value circuit with the VFC320. Op amp, D₁ and Q₁ (its base-emitter junction functioning as a diode) provide full-wave rectification of bipolar input voltages. VFC output frequency is proportional to |e₁|. The sign bit output provides indication of the input polarity.
N (R-PDIP-T**)  
16 PINS SHOWN

NOTES:  
A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. Falls within JEDEC MS-001 (20-pin package is shorter than MS-001).
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