10V Precision Voltage Reference

FEATURES

- +10V ±0.0025V OUTPUT
- VERY LOW DRIFT: 2.5ppm/°C max
- EXCELLENT STABILITY: 5ppm/1000hr typ
- EXCELLENT LINE REGULATION: 1ppm/V max
- EXCELLENT LOAD REGULATION: 10ppm/mA max
- LOW NOISE: 5μVpp typ, 0.1Hz to 10Hz
- WIDE SUPPLY RANGE: 11.4VDC to 36VDC
- LOW QUIESCENT CURRENT: 1.4mA max
- PACKAGE OPTIONS: PLASTIC DIP, SO-8

APPLICATIONS

- PRECISION-CALIBRATED VOLTAGE STANDARD
- D/A AND A/D CONVERTER REFERENCE
- PRECISION CURRENT REFERENCE
- ACCURATE COMPARATOR THRESHOLD REFERENCE
- DIGITAL VOLTMETER
- TEST EQUIPMENT
- PC-BASED INSTRUMENTATION

DESCRIPTION

The REF102 is a precision 10V voltage reference. The drift is laser-trimmed to 2.5ppm/°C max C-grade over the industrial temperature range. The REF102 achieves its precision without a heater. This results in low power, fast warm-up, excellent stability, and low noise. The output voltage is extremely insensitive to both line and load variations and can be externally adjusted with minimal effect on drift and stability. Single-supply operation from 11.4V to 36V and excellent overall specifications make the REF102 an ideal choice for demanding instrumentation and system reference applications.

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ABSOLUTE MAXIMUM RATINGS\(^{(1)}\)

<table>
<thead>
<tr>
<th>Product</th>
<th>Max Initial Error (mV)</th>
<th>Max Drift (PPM/°C)</th>
<th>Package-Lead</th>
<th>Package Designator</th>
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<td>±5</td>
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NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at www.ti.com.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATIONS

Top View

```
1 NC
2 V+
3 NC
4 Com
5 Trim
6 VOUT
7 NC
8 Noise Reduction

NC = Not Connected
```
ELECTRICAL CHARACTERISTICS

At $T_A = +25^\circ C$ and $V_S = +15V$ power supply, unless otherwise noted.

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<th>CONDITIONS</th>
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<th>REF102B</th>
<th>REF102C</th>
<th>UNITS</th>
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<td>Initial $T_A = 25^\circ C$</td>
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<td>10.01</td>
<td>9.995</td>
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<td></td>
<td>vs Temperature $^{(1)}$</td>
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<td>vs Supply (Line Regulation) $V_S = 11.4V$ to 36V</td>
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<td>1</td>
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<tr>
<td></td>
<td>vs Output Current (Load Regulation) $I_L = 0mA$ to +10mA</td>
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<td>10</td>
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<td>vs Time (Load Regulation) $I_L = 0mA$ to –5mA $T_A = +25^\circ C$</td>
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<td>Trim Range $^{(3)}$</td>
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<td>Capacitive Load, max</td>
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<td>NOISE</td>
<td>0.1Hz to 10Hz</td>
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<td>QUIESCENT CURRENT</td>
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<td>WARM-UP TIME $^{(4)}$</td>
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* Specifications same as REF102A.

NOTES:  
(1) The box method is used to specify output voltage drift vs temperature; see the Discussion of Performance section.
(2) Typically 5ppm/1000hrs after 168hr powered stabilization.
(3) Trimming the offset voltage affects drift slightly. See Installation and Operating Instructions for details.
(4) With noise reduction pin floating. See Typical Characteristics for details.
TYPICAL CHARACTERISTICS

At $T_A = +25^\circ C$, $V_\text{IN} = +15V$, unless otherwise noted.

- **POWER TURN-ON RESPONSE**
  
  - $V_{OUT}$ vs $V_{IN}$
  - Time (5µs/div)

- **POWER TURN-ON RESPONSE with 1µF $C_N$**
  
  - $V_{OUT}$ vs $V_{IN}$
  - Time (10ms/div)

- **POWER SUPPLY REJECTION vs FREQUENCY**
  
  - Power Supply Rejection (dB) vs Frequency (Hz)

- **LOAD REGULATION**
  
  - Output Voltage Change (mV) vs Output Current (mA)

- **RESPONSE TO THERMAL SHOCK**
  
  - Output Voltage Change (µV) vs Time (s)

- **QUIESCENT CURRENT vs TEMPERATURE**
  
  - Quiescent Current (mA) vs Temperature (°C)
TYPICAL CHARACTERISTICS (Cont.)

At $T_a = +25\degree C$, $V_S = +15V$, unless otherwise noted.

**THEORY OF OPERATION**

Refer to the diagram on the first page of this data sheet. The 10V output is derived from a compensated buried zener diode DZ$_1$, op amp A$_1$, and resistor network $R_1 - R_6$.

Approximately 8.2V is applied to the non-inverting input of A$_1$ by DZ$_1$, $R_1$, $R_2$, and $R_3$ are laser-trimmed to produce an exact 10V output. The zener bias current is established from the regulated output voltage through $R_4$. $R_5$ allows user-trimming of the output voltage by providing for small external adjustment of the amplifier gain. Because the temperature coefficient (TCR) of $R_5$ closely matches the TCR of $R_1$, $R_2$ and $R_3$, the voltage trim has minimal effect on the reference drift. The output voltage noise of the REF102 is dominated by the noise of the zener diode. A capacitor can be connected between the Noise Reduction pin and ground to form a low-pass filter with $R_6$ and roll off the high-frequency noise of the zener.

**DISCUSSION OF PERFORMANCE**

The REF102 is designed for applications requiring a precision voltage reference where both the initial value at room temperature and the drift over temperature are of importance to the user. Two basic methods of specifying voltage reference drift versus temperature are in common usage in the industry—the butterfly method and the box method. The REF102 is specified by the more commonly-used box method. The box is formed by the high and low specification temperatures and a diagonal, the slope of which is equal to the maximum specified drift.

Since the shape of the actual drift curve is not known, the vertical position of the box is not known, either. It is, however, bounded by $V_{UPPER\ BOUND}$ and $V_{LOWER\ BOUND}$ (see Figure 1). Figure 1 uses the REF102CU as an example. It has a drift specification of 2.5ppm/°C maximum and a specification temperature range of $-25\degree C$ to $+85\degree C$. The box height, $V_1$ to $V_2$, is 2.75mV.

**FIGURE 1. REF102CU Output Voltage Drift.**

![Noise Test Circuit](image-url)
INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CIRCUIT CONNECTION

Figure 2 shows the proper connection of the REF102. To achieve the specified performance, pay careful attention to layout. A low resistance star configuration will reduce voltage errors, noise pickup, and noise coupled from the power supply. Commons should be connected as indicated, being sure to minimize interconnection resistances.

![Figure 2. REF102 Installation.](image)

NOTES: (1) Lead resistances here of up to a few ohms have negligible effect on performance. (2) A resistance of 0.1Ω in series with these leads will cause a 1mV error when the load current is at its maximum of 10mA. This results in a 0.01% error of 10V.

FIGURE 2. REF102 Installation.

OPTIONAL OUTPUT VOLTAGE ADJUSTMENT

Optional output voltage adjustment circuits are shown in Figures 3 and 4. Trimming the output voltage will change the voltage drift by approximately 0.008ppm/°C per mV of trimmed voltage. In the circuit in Figure 3, any mismatch in TCR between the two sections of the potentiometer will also affect drift, but the effect of the $\Delta$TCR is reduced by a factor of five by the internal resistor divider. A high quality potentiometer, with good mechanical stability, such as a cermet, should be used. The circuit in Figure 3 has a minimum trim range of ±300mV. The circuit in Figure 4 has less range but provides higher resolution. The mismatch in TCR between $R_S$ and the internal resistors can introduce some slight drift. This effect is minimized if $R_S$ is kept significantly larger than the 50kΩ internal resistor. A TCR of 100ppm/°C is normally sufficient.

![Figure 3. REF102 Optional Output Voltage Adjust.](image)

Minimum range (±300mV) and minimal degradation of drift.

![Figure 4. REF102 Optional Output Voltage, Fine Adjust.](image)

Higher resolution, reduced range (typically ±25mV).
OPTIONAL NOISE REDUCTION

The high-frequency noise of the REF102 is dominated by the zener diode noise. This noise can be greatly reduced by connecting a capacitor between the Noise Reduction pin and ground. The capacitor forms a low-pass filter with $R_6$ (refer to the figure on page 1) and attenuates the high-frequency noise generated by the zener. Figure 5 shows the effect of a 1µF noise reduction capacitor on the high-frequency noise of the REF102. $R_6$ is typically 7kΩ so the filter has a −3dB frequency of about 22Hz. The result is a reduction in noise from about 800µVpp to under 200µVpp. If further noise reduction is required, use the circuit in Figure 14.

![Effect of 1µF Noise Reduction Capacitor on Broadband Noise (f_{-3dB} = 1MHz)](image)

FIGURE 5. Effect of 1µF Noise Reduction Capacitor on Broadband Noise ($f_{-3dB} = 1MHz$)

APPLICATIONS INFORMATION

High accuracy, extremely low drift, outstanding stability, and low cost make the REF102 an ideal choice for all instrumentation and system reference applications. Figures 6 through 14 show a variety of useful application circuits.

![Figure 6. −10V Reference Using a) Resistor or b) OPA227.](image)

FIGURE 6. −10V Reference Using a) Resistor or b) OPA227. See SBVA008 for more detail.
FIGURE 7. +10V Reference With Output Current Boosted to: a) −20mA < I_L < +20mA (OPA227 also improves transient immunity), b) −5mA < I_L < +100mA, and c) I_L (MAX) = I_L (TYP) +10mA, I_L (MIN) = I_L (TYP) −5mA.

FIGURE 8. Strain Gauge Conditioner for 350Ω Bridge.

See SBVA007 for more details.

FIGURE 9. ±10V Reference.

FIGURE 10. Positive Precision Current Source.
FIGURE 11. Stacked References.

FIGURE 12. ±5V Reference.

FIGURE 13. +5V and +10V Reference.


NOTES: (1) REF102s can be stacked to obtain voltages in multiples of 10V. (2) The supply voltage should be between 10n + 1.4 and 10n + 26, where n is the number of REF102s. (3) Output current of each REF102 must not exceed its rated output current of +10, −5mA. This includes the current delivered to the lower REF102.

V_{REF} = \frac{V_{O1} + V_{O2} + \ldots + V_{OUT\,N}}{N}

\sigma_N = 5\sigma_V \left( f = 0.1Hz \text{ to } 1MHz \right)

See SBVA002 for more details.
## Revision History

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<th>REVISION</th>
<th>PAGE</th>
<th>SECTION</th>
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NOTE: Page numbers for previous revisions may differ from page numbers in the current version.
### PACKAGING INFORMATION

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<th>Package Qty</th>
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<th>Lead/Ball Finish (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
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(1) The marketing status values are defined as follows:
**ACTIVE**: Product device recommended for new designs.
**LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

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Addendum-Page 1
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

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*All dimensions are nominal.*
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

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<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 variation BA.
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