1 Features

- High Supply Voltage Range: 1.8 V to 36 V
- Adjustable Threshold: Down to 400 mV
- High Threshold Accuracy:
  - 0.25% (Typ)
  - 0.75% Max Over Temperature
- Low Quiescent Current: 7 µA (Typ)
- Open-Drain Output
- Internal Hysteresis: 5.5 mV (Typ)
- Temperature Range: –40°C to +125°C
- Package: Thin SOT-23-6

2 Applications

- Notebook PCs and Tablets
- Smartphones
- Digital Cameras
- Video Game Controllers
- Relays and Circuit Breakers
- Portable Medical Devices
- Door and Window Sensors
- Portable- and Battery-Powered Products

3 Description

The TLV6713 high voltage comparator operates over a 1.8-V to 36-V range. The device has a precision comparator with an internal 400-mV reference and an open-drain output rated to 25 V for undervoltage detection. Set the monitored voltage with the use of external resistors.

OUT is driven low when the voltage at the SENSE pin drops below the negative threshold, and goes high when the voltage returns above the positive threshold. The comparator in the TLV6713 includes built-in hysteresis for noise rejection, thereby ensuring stable output operation without false triggering.

The TLV6713 is available in a Thin SOT-23-6 package and is specified over the junction temperature range of –40°C to +125°C.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLV6713</td>
<td>SOT-23  (6)</td>
<td>2.90 mm × 1.60 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the package option addendum at the end of the data sheet.

Typical Application
Table of Contents

1 Features ................................................................. 1
2 Applications ............................................................. 1
3 Description ............................................................. 1
4 Revision History ....................................................... 2
5 Device Comparison Table ............................................ 2
6 Pin Configuration and Functions .................................... 3
7 Specifications .......................................................... 4
   7.1 Absolute Maximum Ratings .................................. 4
   7.2 ESD Ratings ...................................................... 4
   7.3 Recommended Operating Conditions ...................... 4
   7.4 Thermal Information ........................................... 4
   7.5 Electrical Characteristics ..................................... 5
   7.6 Timing Requirements .......................................... 5
   7.7 Typical Characteristics ........................................ 6
8 Detailed Description .................................................. 8
   8.1 Overview .......................................................... 8
   8.2 Functional Block Diagram ..................................... 8
9 Application and Implementation .................................... 10
   9.1 Application Information ....................................... 10
   9.2 Typical Application ............................................ 11
10 Power Supply Recommendations .................................. 14
11 Layout ................................................................... 15
   11.1 Layout Guidelines .............................................. 15
   11.2 Layout Example ................................................ 15
12 Device and Documentation Support ............................... 16
   12.1 Device Support ................................................ 16
   12.2 Receiving Notification of Documentation Updates .... 16
   12.3 Community Resources ........................................ 16
   12.4 Trademarks ..................................................... 16
   12.5 Electrostatic Discharge Caution ............................ 16
   12.6 Glossary ........................................................ 16
13 Mechanical, Packaging, and Orderable Information ............ 16

4 Revision History

Changes from Revision A (April 2018) to Revision B Page

• Changed Typical Application graphic pull-up resistor text from 36V to 25V ................................................................. 1

Changes from Original (January 2018) to Revision A Page

• Changed Advance Information to Production Data ................................................................. 1

5 Device Comparison Table

Table 1. TLV67xx Integrated Comparator Family

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>CONFIGURATION</th>
<th>OPERATING VOLTAGE RANGE</th>
<th>THRESHOLD ACCURACY OVER TEMPERATURE</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLV6700</td>
<td>Window</td>
<td>1.8 V to 18 V</td>
<td>1%</td>
</tr>
<tr>
<td>TLV6703</td>
<td>Non-Inverting Single Channel</td>
<td>1.8 V to 18 V</td>
<td>1%</td>
</tr>
<tr>
<td>TLV6710</td>
<td>Window</td>
<td>1.8 V to 36 V</td>
<td>0.75%</td>
</tr>
<tr>
<td>TLV6713</td>
<td>Non-Inverting Single Channel</td>
<td>1.8 V to 36 V</td>
<td>0.75%</td>
</tr>
</tbody>
</table>
6 Pin Configuration and Functions

![DDC Package 6-Pin SOT-23-Thin Top View](image.png)

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td>2, 4, 6</td>
<td>Ground. Connect all three pins to ground.</td>
</tr>
<tr>
<td>OUT</td>
<td>1</td>
<td>O Comparator open-drain output. This pin is driven low when the voltage at this comparator is less than $V_{IT-}$. The output goes high when the sense voltage rises above $V_{IT+}$.</td>
</tr>
<tr>
<td>SENSE</td>
<td>3</td>
<td>I Comparator input. This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this pin drops below the threshold voltage $V_{IT-}$, OUT is driven low.</td>
</tr>
<tr>
<td>VDD</td>
<td>5</td>
<td>I Supply-voltage input. Connect a 1.8-V to 36-V supply to VDD to power the device. It is good analog design practice to place a 0.1-µF ceramic capacitor close to this pin.</td>
</tr>
</tbody>
</table>
7 Specifications

7.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Voltage (2)</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_DD</td>
<td>–0.3</td>
<td>40</td>
<td>V</td>
</tr>
<tr>
<td>V_OUT</td>
<td>–0.3</td>
<td>28</td>
<td></td>
</tr>
<tr>
<td>V_SENSE</td>
<td>–0.3</td>
<td>7</td>
<td></td>
</tr>
</tbody>
</table>

Current: Output pin current

<table>
<thead>
<tr>
<th>MAX</th>
<th>mA</th>
</tr>
</thead>
<tbody>
<tr>
<td>40</td>
<td></td>
</tr>
</tbody>
</table>

Temperature: Operating junction, T_J

<table>
<thead>
<tr>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>–40</td>
<td>25</td>
<td>125</td>
<td></td>
</tr>
</tbody>
</table>

Storage, T_STG

<table>
<thead>
<tr>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>–40</td>
<td>25</td>
<td>125</td>
<td></td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to network ground terminal.

7.2 ESD Ratings

<table>
<thead>
<tr>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>±2000</td>
<td>V</td>
</tr>
</tbody>
</table>

7.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_DD</td>
<td>1.8</td>
<td>36</td>
<td>V</td>
</tr>
<tr>
<td>V_SENSE</td>
<td>0</td>
<td>1.7</td>
<td>V</td>
</tr>
<tr>
<td>V_OUT</td>
<td>0</td>
<td>25</td>
<td>V</td>
</tr>
<tr>
<td>V_PULLUP</td>
<td>0</td>
<td>25</td>
<td>V</td>
</tr>
<tr>
<td>I_OUT</td>
<td>0</td>
<td>10</td>
<td>mA</td>
</tr>
<tr>
<td>T_J</td>
<td>–40</td>
<td>25</td>
<td>125</td>
</tr>
</tbody>
</table>

7.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC (1)</th>
<th>TLV6713</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>DDC (SOT-23)</td>
</tr>
<tr>
<td>R_JA</td>
<td>201.6</td>
</tr>
<tr>
<td>R_JC(top)</td>
<td>47.8</td>
</tr>
<tr>
<td>R_JB</td>
<td>51.2</td>
</tr>
<tr>
<td>V_JT</td>
<td>0.7</td>
</tr>
<tr>
<td>V_JB</td>
<td>50.8</td>
</tr>
<tr>
<td>R_JC(bot)</td>
<td>N/A</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
7.5 Electrical Characteristics

Over the operating temperature range of $T_J = -40°C$ to $+125°C$, $1.8 \, V \leq V_{DD} < 36 \, V$, and pullup resistor $R_P = 100 \, k\Omega$ (unless otherwise noted). Typical values are at $T_J = 25°C$ and $V_{DD} = 12 \, V$.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{(POR)}$ Power-on reset voltage$^{(1)}$</td>
<td>$V_{OL} \leq 0.2 , V$</td>
<td>$0.8$</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IT-}$ SENSE pin negative input threshold voltage</td>
<td>$V_{DD} = 1.8 , V$ to $36 , V$</td>
<td>$397$</td>
<td>$400$</td>
<td>$403$</td>
<td>mV</td>
</tr>
<tr>
<td>$V_{IT+}$ SENSE pin positive input threshold voltage</td>
<td>$V_{DD} = 1.8 , V$ to $36 , V$</td>
<td>$400$</td>
<td>$405.5$</td>
<td>$413$</td>
<td>mV</td>
</tr>
<tr>
<td>$V_{HYS}$ SENSE pin hysteresis voltage (HYS = $V_{IT+} - V_{IT-}$)</td>
<td>$V_{DD} = 1.8 , V$ to $36 , V$</td>
<td>$2$</td>
<td>$5.5$</td>
<td>$12$</td>
<td>mV</td>
</tr>
<tr>
<td>$V_{OL}$ Low-level output voltage</td>
<td>$V_{DD} = 1.8 , V$, $I_{OUT} = 3 , mA$</td>
<td>$130$</td>
<td></td>
<td>$250$</td>
<td>mV</td>
</tr>
<tr>
<td>$I_{IN}$ Input current (at SENSE pin)</td>
<td>$V_{DD} = 1.8 , V$ and $36 , V$, $V_{SENSE} = 6.5 , V$</td>
<td>$-25$</td>
<td>$+1$</td>
<td>$+25$</td>
<td>nA</td>
</tr>
<tr>
<td>$I_{D(\text{leak})}$ Open-drain leakage current</td>
<td>$V_{DD} = 1.8 , V$ and $36 , V$, $V_{OUT} = 25 , V$</td>
<td>$10$</td>
<td>$300$</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>$I_{DD}$ Supply current</td>
<td>$V_{DD} = 1.8 , V$ to $36 , V$</td>
<td>$8$</td>
<td>$11$</td>
<td></td>
<td>$\mu$A</td>
</tr>
<tr>
<td>UVLO Undervoltage lockout$^{(2)}$</td>
<td>$V_{DD}$ falling</td>
<td>$1.3$</td>
<td>$1.5$</td>
<td>$1.7$</td>
<td>V</td>
</tr>
</tbody>
</table>

$^{(1)}$ The lowest supply voltage ($V_{DD}$) at which output is active; $t_{r(VDD)} > 15 \, \mu$s/$V$. If less than $V_{(POR)}$, the output is undetermined.

$^{(2)}$ When $V_{DD}$ falls below UVLO, OUT is driven low. The output cannot be determined if less than $V_{(POR)}$.

7.6 Timing Requirements

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{pd(HL)}$ High-to-low propagation delay$^{(1)}$</td>
<td>$V_{DD} = 24 , V$, ±10-mV input overdrive, $R_L = 100 , k\Omega$, $V_{OH} = 0.9 \times V_{DD}$, $V_{OL} = 250 , mV$</td>
<td>$9.9$</td>
<td></td>
<td></td>
<td>$\mu$s</td>
</tr>
<tr>
<td>$t_{pd(LH)}$ Low-to-high propagation delay$^{(1)}$</td>
<td>$V_{DD} = 24 , V$, ±10-mV input overdrive, $R_L = 100 , k\Omega$, $V_{OH} = 0.9 \times V_{DD}$, $V_{OL} = 250 , mV$</td>
<td>$28.1$</td>
<td></td>
<td></td>
<td>$\mu$s</td>
</tr>
<tr>
<td>$t_{d(start)}$ Startup delay</td>
<td>$V_{DD} = 5 , V$</td>
<td>$155$</td>
<td></td>
<td></td>
<td>$\mu$s</td>
</tr>
<tr>
<td>$t_r$ Output rise time</td>
<td>$V_{DD} = 12 , V$, 10-mV input overdrive, $R_L = 100 , k\Omega$, $C_L = 10 , pF$, $V_O = (0.1 , \text{to} , 0.9) \times V_{DD}$</td>
<td>$2.7$</td>
<td></td>
<td></td>
<td>$\mu$s</td>
</tr>
<tr>
<td>$t_f$ Output fall time</td>
<td>$V_{DD} = 12 , V$, 10-mV input overdrive, $R_L = 100 , k\Omega$, $C_L = 10 , pF$, $V_O = (0.9 , \text{to} , 0.1) \times V_{DD}$</td>
<td>$0.12$</td>
<td></td>
<td></td>
<td>$\mu$s</td>
</tr>
</tbody>
</table>

$^{(1)}$ High-to-low and low-to-high refers to the transition at the input pin (SENSE).

$^{(2)}$ During power on, $V_{DD}$ must exceed $1.8 \, V$ for at least $150 \, \mu$s (typical) before the output state reflects the input condition.

![Figure 1. Timing Diagram](image-url)
7.7 Typical Characteristics

at $T_J = 25°C$ and $V_{DD} = 12$ V (unless otherwise noted)
Typical Characteristics (continued)

at $T_J = 25°C$ and $V_{DD} = 12$ V (unless otherwise noted)

**Figure 8. Propagation Delay vs Temperature**
(High-to-Low Transition at SENSE)

**Figure 9. Propagation Delay vs Temperature**
(Low-to-High Transition at SENSE)

**Figure 10. Output Voltage Low vs Output Sink Current**

**Figure 11. Output Voltage Low vs Output Sink Current**

**Figure 12. Start-up Delay vs Temperature**
8 Detailed Description

8.1 Overview
The TLV6713 combines a comparator and a precision reference for undervoltage detection. The TLV6713 features a wide supply voltage range (1.8 V to 36 V) and a high-accuracy threshold voltage of 400 mV (0.75% over temperature) with built-in hysteresis. The output is rated to 25 V and can sink up to 10 mA.

Set the input pin (SENSE) to monitor any voltage above 0.4 V by using an external resistor divider network. SENSE has very low input leakage current, allowing the use of a large resistor divider without sacrificing system accuracy. The relationship between the input and the output is shown in Table 2. Broad voltage thresholds are supported that enable the device to be used in a wide array of applications.

<table>
<thead>
<tr>
<th>CONDITION</th>
<th>OUTPUT</th>
<th>OUTPUT STATE</th>
</tr>
</thead>
<tbody>
<tr>
<td>SENSE &gt; V_{IT+}</td>
<td>OUT high</td>
<td>Output high impedance</td>
</tr>
<tr>
<td>SENSE &lt; V_{IT-}</td>
<td>OUT low</td>
<td>Output sinking</td>
</tr>
</tbody>
</table>

8.2 Functional Block Diagram

![Functional Block Diagram](image-url)
8.3 Feature Description

8.3.1 Input Pin (SENSE)

The TLV6713 combines a comparator with a precision reference voltage. The comparator has one external input and one internal input connected to the internal reference. The falling threshold on SENSE is designed and trimmed to be equal to the reference voltage (400 mV). This configuration optimizes the device accuracy. The comparator also has built-in hysteresis that proves immunity to noise and ensures stable operation.

The comparator input swings from ground to 1.7 V (7 V absolute maximum), regardless of the device supply voltage used. Although not required in most cases, it is good analog design practice to place a 1-nF to 10-nF bypass capacitor at the comparator input for noisy applications to reduce sensitivity to transient voltage changes on the monitored signal.

For the comparator, the output (OUT) is driven to logic low when the input SENSE voltage drops below $V_{IT-}$. When the voltage exceeds $V_{IT+}$, OUT goes to a high-impedance state; see Figure 1.

8.3.2 Output Pin (OUT)

In a typical TLV6713 application, the output is connected to a GPIO input of the processor (such as a digital signal processor [DSP], central processing unit [CPU], field-programmable gate array [FPGA], or application-specific integrated circuit [ASIC]).

The TLV6713 provides an open-drain output (OUT) rated to 25 V, independent of supply voltage, and can sink up to 40 mA. A pullup resistor is required to hold the line high when the output goes to a high-impedance state. Connect this pullup resistor to a voltage rail that meets the logic requirements of the downstream device. To ensure the proper voltage level, give some consideration when choosing the pullup resistor value. The pullup resistor value is determined by $V_{OL}$, output capacitive loading, and the open-drain leakage current ($I_{D(leak)}$). These values are specified in the Electrical Characteristics table.

Table 2 and Input Pin (SENSE) describe how the output is asserted or high impedance. See Figure 1 for a timing diagram that describes the relationship between threshold voltage and the respective output.

8.4 Device Functional Modes

8.4.1 Normal Operation ($V_{DD} > UVLO$)

When the voltage on VDD is greater than 1.8 V for at least 155 µs, the OUT signal corresponds to the voltage on SENSE, as listed in Table 2.

8.4.2 Undervoltage Lockout ($V_{(POR)} < V_{DD} < UVLO$)

When the voltage on VDD is less than the device UVLO voltage, and greater than the power-on reset voltage, $V_{(POR)}$, the OUT signal is asserted regardless of the voltage on SENSE.

8.4.3 Power On Reset ($V_{DD} < V_{(POR)}$)

When the voltage on VDD is lower than the required voltage to internally pull the asserted output to GND ($V_{(POR)}$), OUT is in a high-impedance state.
9 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information
The TLV6713 is used as a precision voltage supervisor in several different configurations. The monitored voltage \( V_{\text{MON}} \), VDD voltage, and output pullup voltage can be independent voltages or connected in any configuration. The following sections show the connection configurations and the voltage limitations for each configuration.

9.1.1 Input and Output Configurations
Figure 13 and Figure 14 show examples of the various input and output configurations.

![Figure 13. Monitoring the Same Voltage as VDD](image-url)
Application Information (continued)

![Diagram of TLV6713 circuit](image)

**Figure 14. Monitoring a Voltage Other than **$V_{DD}$**)**

9.1.2 Immunity to Input Pin Voltage Transients

The TLV6713 is immune to short voltage transient spikes on the input pin. Sensitivity to transients depends on both transient duration and amplitude; see **Figure 3, Minimum Pulse Duration vs Threshold Overdrive Voltage**.

9.2 Typical Application

![Diagram of 24-V, 10% Comparator](image)

**Figure 15. 24-V, 10% Comparator**
Typical Application (continued)

9.2.1 Design Requirements

This typical voltage detector application is designed to meet the parameters listed in Table 3:

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>DESIGN REQUIREMENT</th>
<th>DESIGN RESULT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Monitored voltage</td>
<td>24-V nominal, falling ((V_{\text{MON(UV)}})) threshold 10% nominal (21.6 V)</td>
<td>(V_{\text{MON(UV)}} = 21.8 \text{ V} \pm 2.7%)</td>
</tr>
<tr>
<td>Output logic voltage</td>
<td>3.3-V CMOS</td>
<td>3.3-V CMOS</td>
</tr>
<tr>
<td>Maximum current consumption</td>
<td>30 µA</td>
<td>24 µA</td>
</tr>
</tbody>
</table>

9.2.2 Detailed Design Procedure

9.2.2.1 Resistor Divider Selection

The resistor divider values and target threshold voltage can be calculated by using Equation 1 to determine \(V_{\text{MON(UV)}}\):

\[
V_{\text{MON(UV)}} = \left(1 + \frac{R1}{R2}\right) \times V_{\text{IT}}.
\]

where

- \(R1\) and \(R2\) are the resistor values for the resistor divider on the SENSE pin
- \(V_{\text{MON(UV)}}\) is the target voltage at which an undervoltage condition is detected

Choose an \(R_{\text{TOTAL}} = R1 + R2\) so that the current through the divider is approximately 100 times higher than the input current at the SENSE pin. Use resistors with high values to minimize current consumption (as a result of low input bias current) without adding significant error to the resistive divider. For details on sizing input resistors, refer to Optimizing Resistor Dividers at a Comparator Input, available for download from www.ti.com.

9.2.2.2 Pullup Resistor Selection

To ensure the proper logic-high voltage level (\(V_{\text{HI}}\)), select a pullup resistor value where the pullup voltage divided by the pullup resistor value does not exceed the sink-current capability of the device. Confirm this voltage level by verifying that the pullup voltage minus the open-drain leakage current (\(I_{\text{D(leak)}}\)) multiplied by the resistor is greater than the desired \(V_{\text{HI}}\). These values are specified in the Electrical Characteristics.

Use Equation 2 to calculate the value of the pullup resistor.

\[
\frac{V_{\text{HI}} - V_{\text{pullup}}}{I_{\text{D(leak)}}} \leq RP \leq \frac{V_{\text{pullup}}}{I_{\text{OUT}}}
\]

9.2.2.3 Input Supply Capacitor

Although an input capacitor is not required for stability, for good analog design practice, connect a 0.1-µF low equivalent series resistance (ESR) capacitor across the VDD and GND pins. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source.
9.2.3 Application Curve

![Application Curve Diagram](image)

Figure 16. 24-V Window Monitor Output Response
10 Power Supply Recommendations

The TLV6713 has a 40-V absolute maximum rating on the VDD pin, with a recommended maximum operating condition of 36 V. If the voltage supply that provides power to VDD is susceptible to any large voltage transient that may exceed 40 V, or if the supply exhibits high voltage slew rates greater than 1 V/µs, then place an RC filter between the supply and VDD to filter any high-frequency transient surges on the VDD pin. In these cases, a 100-Ω resistor and 0.01-µF capacitor are required, as shown in Figure 17.

![Figure 17. Using a RC Filter to Remove High-Frequency Disturbances on VDD](image)
11 Layout

11.1 Layout Guidelines

- Place R2 and R2 close to the device to minimize noise coupling into the SENSE node.
- Place the VDD decoupling capacitor close to the device.
- Avoid using long traces for the VDD supply node. The VDD capacitor (C\text{VDD}), along with parasitic inductance from the supply to the capacitor, might form an LC tank and create ringing with peak voltages above the maximum VDD voltage. If long traces are unavoidable, see Figure 17 for an example of filtering VDD.

11.2 Layout Example

![Recommended Layout Diagram](image-url)

Figure 18. Recommended Layout
12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support
The DIP Adapter Evaluation Module allows conversion of the SOT-23-6 package to a standard DIP-6 pinout for ease of prototyping and bench evaluation.

12.2 Receiving Notification of Documentation Updates
To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** Ti's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** Ti's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks
E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary
SLYZ022 — Ti Glossary.
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLV6713DDCR</td>
<td>ACTIVE</td>
<td>SOT-23-THIN</td>
<td>DDC</td>
<td>6</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>1II1</td>
<td>Samples</td>
</tr>
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<td>-40 to 125</td>
<td>1II1</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
**TAPE AND REEL INFORMATION**

*All dimensions are nominal*

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<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLV6713DDCR</td>
<td>SOT-23-THIN</td>
<td>DDC</td>
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<td>180.0</td>
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<td>3.2</td>
<td>1.4</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
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<td>DDC</td>
<td>6</td>
<td>250</td>
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<td>8.0</td>
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</tr>
<tr>
<td>Device</td>
<td>Package Type</td>
<td>Package Drawing</td>
<td>Pins</td>
<td>SPQ</td>
<td>Length (mm)</td>
<td>Width (mm)</td>
<td>Height (mm)</td>
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</tr>
</tbody>
</table>

*All dimensions are nominal*
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.

5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
design recommendations.
7. Board assembly site may have different recommendations for stencil design.
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