TPS746 1-A High Accuracy Adjustable LDO With Power-Good in a Small Size Package

1 Features

- Input Voltage Range: 1.5 V to 6.0 V
- Adjustable Output Voltage:
  - 0.55 V to 5.5 V
- Very Low Dropout:
  - 225 mV (max) at 1 A (3.3 V<sub>OUT</sub>)
- High Output Accuracy:
  - 0.7%, Typical
  - 1%, Maximum Over Temperature (85°C)
- Open-Drain Power-Good Output
- Power-Good Rising Delay:
  - TPS746: 165 µs
  - TPS746B: 5 ms
- I<sub>Q</sub>: 25 µA (Typical)
- Built-In Soft-Start With Monotonic V<sub>OUT</sub> Rise
- Package:
  - 2-mm × 2-mm 6-Pin WSON (DRV)
- Active Output Discharge

2 Applications

- Set-Top Boxes, Gaming Consoles
- Home Theater and Entertainment
- Desktops, Notebooks, Ultrabooks
- Printers
- Servers
- Thermostat and Lighting Controls
- Electronic Point of Sale (EPOS)

3 Description

The TPS746 is an adjustable 1-A low-dropout (LDO) regulator with power-good functionality. This device is available in a small, 6-pin, 2-mm × 2-mm WSON package and consumes very low quiescent current and provides fast line and load transient performance. The TPS746 features an ultra-low dropout of 225 mV at 1 A that can help improve the power efficiency of the system.

The TPS746 is optimized for a wide variety of applications by supporting an input voltage range from 1.5 V to 6.0 V and an externally adjustable output range of 0.55 V to 5.5 V. The low output voltage enables this LDO to power the modern microcontrollers with lower core voltages. Additionally, the TPS746 has a low I<sub>Q</sub> with enable functionality to minimize standby power. This device features an internal soft-start to lower the inrush current, which provides a controlled voltage to the load and minimizes the input voltage drop during start up.

The TPS746 has a power-good (PG) output that monitors the voltage at the feedback pin to indicate the status of the output voltage. The EN input and PG output can be used for sequencing multiple power sources in the system.

The TPS746 is stable with small ceramic output capacitors, allowing for a small overall solution size. A precision band-gap and error amplifier provides a high accuracy of 0.7% max at 25°C and 1% max over temperature (85°C). This device includes integrated thermal shutdown, current limit, and undervoltage lockout (UVLO) features. The TPS746 has an internal foldback current limit that helps reduce the thermal dissipation during short-circuit events.

Device Information<sup>(1)</sup>

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS746</td>
<td>WSON (6)</td>
<td>2.00 mm × 2.00 mm</td>
</tr>
</tbody>
</table>

<sup>(1)</sup> For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
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4 Revision History

Changes from Original (April 2018) to Revision A

Page

• Changed document status from Advanced information to Production Data ................................................. 1
5 Pin Configuration and Functions

Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>PG</td>
<td>5</td>
<td>Output</td>
</tr>
<tr>
<td>EN</td>
<td>4</td>
<td>Input</td>
</tr>
<tr>
<td>FB</td>
<td>2</td>
<td>—</td>
</tr>
<tr>
<td>GND</td>
<td>3</td>
<td>—</td>
</tr>
<tr>
<td>IN</td>
<td>6</td>
<td>Input</td>
</tr>
<tr>
<td>OUT</td>
<td>1</td>
<td>Output</td>
</tr>
<tr>
<td>Pad</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

6 Specifications

6.1 Absolute Maximum Ratings
over operating free-air temperature range (unless otherwise noted) \(^{(1)}\)

<table>
<thead>
<tr>
<th>I/O</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage, (V_{\text{IN}})</td>
<td>0.3</td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td>Enable voltage, (V_{\text{EN}})</td>
<td>0.3</td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td>Power-good, (V_{\text{PG}})</td>
<td>0.3</td>
<td>6.0</td>
<td>V</td>
</tr>
<tr>
<td>Output voltage, (V_{\text{OUT}})</td>
<td>0.3</td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td>Power-good current</td>
<td>±10 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating junction temp., (T_{J})</td>
<td>-40</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temp., (T_{\text{stg}})</td>
<td>-65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

\(^{(2)}\) The absolute maximum rating is \(V_{\text{EN}} + 0.3\) V or 6.0 V, whichever is smaller.
6.2 ESD Ratings

<table>
<thead>
<tr>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td>±500</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$</td>
<td>Input voltage</td>
<td>1.5</td>
<td>6.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{OUT}$</td>
<td>Output voltage</td>
<td>0.55</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{OUT}$</td>
<td>Output current</td>
<td>0</td>
<td>1</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>$C_{IN}$</td>
<td>Input capacitor</td>
<td>1</td>
<td></td>
<td>µF</td>
<td></td>
</tr>
<tr>
<td>$C_{OUT}$</td>
<td>Output capacitor</td>
<td>1</td>
<td>220</td>
<td>µF</td>
<td></td>
</tr>
<tr>
<td>$V_{EN}$</td>
<td>Enable voltage</td>
<td>0</td>
<td>6.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{EN}$</td>
<td>Enable toggle frequency</td>
<td>10</td>
<td>kHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{PG}$</td>
<td>PG voltage</td>
<td>0</td>
<td>6.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$T_J$</td>
<td>Junction temperature</td>
<td>−40</td>
<td>125</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

*Minimum derated capacitance of 0.47 µF is required for stability.*

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>TPS746 DRV (WSON)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{\theta JA}$</td>
<td>80.3</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{\theta JC}$(top)</td>
<td>98.7</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{\theta JB}$</td>
<td>44.8</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\psi_{JT}$</td>
<td>6.1</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\psi_{JB}$</td>
<td>45.0</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{\theta JC}$(bot)</td>
<td>20.8</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{FB}$</td>
<td>Feedback voltage</td>
<td>$T_J = 25^\circ C$</td>
<td>−0.7%</td>
<td>0.7%</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_J = 25^\circ C$, $-40^\circ C \leq T_J \leq +85^\circ C$</td>
<td>−1%</td>
<td>1%</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$-40^\circ C \leq T_J \leq +125^\circ C$</td>
<td>−1.5%</td>
<td>1.5%</td>
<td></td>
</tr>
<tr>
<td>$V_{OUT}$</td>
<td>Output voltage</td>
<td>$V_{OUT} = V_{OUT}(\text{NOM}) + 0.5 \text{ V or } 1.5 \text{ V (whichever is greater)}$, $I_{OUT} = 1 \text{ mA}$</td>
<td>2</td>
<td>7.5</td>
<td>mV</td>
</tr>
<tr>
<td>$I_{GND}$</td>
<td>Ground current</td>
<td>$I_{GND} = 0 \text{ mA}$, $T_J = 25^\circ C$, $-40^\circ C \leq T_J \leq +125^\circ C$</td>
<td>10</td>
<td>25</td>
<td>31</td>
</tr>
</tbody>
</table>

(1) When the device is connected to external feedback resistors at the FB pin, external resistor tolerances are not included.

(2) $V_{IN} = 1.5 \text{ V for } V_{OUT} < 1.0 \text{ V}$
Electrical Characteristics (continued)

at operating temperature range (T_J = –40°C to 125°C), V_IN = V_OUT(NOM) + 0.5 V or 1.5 V (whichever is greater), I_OUT = 1 mA, V_EN = V_IN, and C_IN = C_OUT = 1 μF, unless otherwise noted. All typical values at T_J = 25°C.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_SHDN</td>
<td>Shutdown current V_EN ≤ 0.3 V, 1.5 V ≤ V_IN ≤ 6.0 V</td>
<td></td>
<td>0.1</td>
<td>1</td>
<td>μA</td>
</tr>
<tr>
<td>I_FB</td>
<td>Feedback pin current</td>
<td>0.01</td>
<td>0.1</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>I_CL</td>
<td>Output current limit V_IN = V_OUT(NOM) + 1.0 V</td>
<td></td>
<td>0.65</td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0.8</td>
<td>0.9</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0.9</td>
<td>1.0</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.0</td>
<td>1.2</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.2</td>
<td>1.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.5</td>
<td>1.8</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.8</td>
<td>2.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.5</td>
<td>3.3</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3.3</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>I_VIN = 50 mA f = 1 kHz</td>
<td></td>
<td>50</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>I_VIN = 50 mA f = 100 kHz</td>
<td></td>
<td>45</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>I_VIN = 50 mA f = 1 MHz</td>
<td></td>
<td>30</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ISP</td>
<td>Short-circuit current limit V_IN = V_OUT(NOM) + 1.0 V</td>
<td></td>
<td>896</td>
<td>1050</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>765</td>
<td>920</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>700</td>
<td>850</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>600</td>
<td>750</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>464</td>
<td>585</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>332</td>
<td>440</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>264</td>
<td>360</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>193</td>
<td>270</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>161</td>
<td>225</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>Dropout voltage V_IN = V_OUT(NOM) + 1 V</td>
<td></td>
<td>1.21</td>
<td>1.33</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>I_IN = 50 mA f = 1 kHz</td>
<td></td>
<td>1.17</td>
<td>1.29</td>
<td></td>
</tr>
<tr>
<td></td>
<td>I_IN = 50 mA f = 100 kHz</td>
<td></td>
<td>40</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>I_IN = 50 mA f = 1 MHz</td>
<td></td>
<td>500</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>V_IN rising f = 1 kHz</td>
<td></td>
<td>53</td>
<td></td>
<td>μVRMS</td>
</tr>
<tr>
<td></td>
<td>V_IN falling f = 1 kHz</td>
<td></td>
<td>45</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>V_IN hysteresis f = 1 MHz</td>
<td></td>
<td>30</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>V_IN = V_OUT(NOM) x 95%</td>
<td></td>
<td>30</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>From EN low-to-high transition to V_OUT = V_OUT(NOM) x 95%</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>EN pin high voltage V_EN = V_IN = 6.0 V</td>
<td>1.0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>EN pin low voltage V_EN = 6.0 V</td>
<td>0.3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Enable pin current V_IN = V_EN = 6.0 V</td>
<td>10</td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td>Pulldown resistance V_IN = 6.0 V</td>
<td>95</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>PG high threshold V_OUT increasing</td>
<td>89</td>
<td>94</td>
<td>95</td>
<td>%V_OUT</td>
</tr>
<tr>
<td></td>
<td>PG low threshold V_OUT decreasing</td>
<td>87</td>
<td>92</td>
<td>93</td>
<td>%V_OUT</td>
</tr>
<tr>
<td></td>
<td>V_IN ≥ 1.5 V, I_SINK = 1 mA</td>
<td>300</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>V_IN ≥ 2.75 V, I_SINK = 2 mA</td>
<td>300</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>PG pin leakage current V_OUT &gt; PG_HTH, V_PG = 6.0 V</td>
<td>300</td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td>Thermal shutdown, temperature increasing</td>
<td>170</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>Reset, temperature decreasing</td>
<td>155</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
6.6 Timing Requirements

at operating temperature range \((T_J = -40°C \text{ to } 125°C)\), \(V_{IN} = V_{OUT(NOM)} + 0.5 \text{ V or } 1.5 \text{ V (whichever is greater)}\), \(I_{OUT} = 1 \text{ mA}, \ V_{EN} = V_{IN}\), and \(C_{IN} = C_{OUT} = 1 \mu F\), unless otherwise noted. All typical values at \(T_J = 25°C\).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(t_{PGDH})</td>
<td>PG delay time rising (^{(1)})</td>
<td>Time from 92% (V_{OUT}) to 20% of PG</td>
<td>TPS746</td>
<td>135</td>
<td>165</td>
</tr>
<tr>
<td>(t_{PGDH})</td>
<td>PG delay time rising (^{(1)})</td>
<td>Time from 92% (V_{OUT}) to 20% of PG.</td>
<td>TPS746B</td>
<td>4.5</td>
<td>5.0</td>
</tr>
<tr>
<td>(t_{PGDL})</td>
<td>PG delay time falling (^{(1)})</td>
<td>Time from 90% (V_{OUT}) to 80% of PG</td>
<td></td>
<td>1.5</td>
<td>7</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Output overdrive = 10%
6.7 Typical Characteristics

at operating temperature range $T_J = 25^\circ C$, $V_{IN} = V_{OUT(NOM)} + 0.5$ V or 1.5 V (whichever is greater), $I_{OUT} = 1$ mA, $V_{EN} = V_{IN}$, and $C_{IN} = C_{OUT} = 1 \mu F$ (unless otherwise noted)
Typical Characteristics (continued)

at operating temperature range $T_J = 25°C$, $V_{IN} = V_{OUT(NOM)} + 0.5$ V or 1.5 V (whichever is greater), $I_{OUT} = 1$ mA, $V_{EN} = V_{IN}$, and $C_{IN} = C_{OUT} = 1 \mu F$ (unless otherwise noted)
Typical Characteristics (continued)

at operating temperature range $T_J = 25^\circ C$, $V_{IN} = V_{OUT(NOM)} + 0.5$ V or 1.5 V (whichever is greater), $I_{OUT} = 1$ mA, $V_{EN} = V_{IN}$, and $C_{IN} = C_{OUT} = 1$ $\mu$F (unless otherwise noted)
Typical Characteristics (continued)

at operating temperature range $T_J = 25^\circ$C, $V_{IN} = V_{OUT(NOM)} + 0.5$ V or 1.5 V (whichever is greater), $I_{OUT} = 1$ mA, $V_{EN} = V_{IN}$, and $C_{IN} = C_{OUT} = 1 \mu$F (unless otherwise noted)
Typical Characteristics (continued)

at operating temperature range $T_J = 25^\circ C$, $V_{IN} = V_{OUT(NOM)} + 0.5 \text{ V} \text{ or } 1.5 \text{ V}$ (whichever is greater), $I_{OUT} = 1 \text{ mA}$, $V_{EN} = V_{IN}$, and $C_{IN} = C_{OUT} = 1 \mu F$ (unless otherwise noted).

$V_{OUT} = 3.3 \text{ V}$, $I_{OUT} = 1 \text{ mA}$, $V_{IN}$ slew rate = $1 \text{ V/\mu s}$

$V_{OUT} = 0.55 \text{ V}$, $V_{IN} = 2 \text{ V}$, $I_{OUT}$ slew rate = $1 \text{ A/\mu s}$

$V_{OUT} = 5 \text{ V}$, $V_{IN} = 5.5 \text{ V}$, $I_{OUT}$ slew rate = $1 \text{ A/\mu s}$

$V_{OUT} = 3.3 \text{ V}$, $V_{IN} = 3.8 \text{ V}$, $I_{OUT}$ slew rate = $1 \text{ A/\mu s}$

$V_{IN} = 3.8 \text{ V}$, $V_{OUT} = 3.3 \text{ V}$

$V_{OUT} = 3.3 \text{ V}$, $V_{IN} = 3.8 \text{ V}$, $I_{OUT}$ slew rate = $1 \text{ A/\mu s}$

$V_{IN} = 3.8 \text{ V}$, $V_{OUT} = 3.3 \text{ V}$, $I_{OUT} = 1 \text{ mA}$

$V_{IN} = 3.8 \text{ V}$, $V_{OUT} = 3.3 \text{ V}$, $I_{OUT} = 1 \text{ mA}$
Typical Characteristics (continued)

at operating temperature range $T_J = 25°C$, $V_{IN} = V_{OUT(NOM)} + 0.5\ V$ or $1.5\ V$ (whichever is greater), $I_{OUT} = 1\ mA$, $V_{EN} = V_{IN}$, and $C_E = C_{OUT} = 1\ \mu F$ (unless otherwise noted).

Figure 31. PSRR vs Frequency and $V_{IN}$

Figure 32. PSRR vs Frequency and $V_{IN}$

Figure 33. PSRR vs Frequency and $V_{IN}$

Figure 34. PSRR vs Frequency and $V_{IN}$

Figure 35. PSRR vs Frequency

Figure 36. PSRR vs Frequency
Typical Characteristics (continued)

at operating temperature range $T_J = 25°C$, $V_{IN} = V_{OUT(NOM)} + 0.5$ V or 1.5 V (whichever is greater), $I_{OUT} = 1$ mA, $V_{EN} = V_{IN}$, and $C_{IN} = C_{OUT} = 1 \mu$F (unless otherwise noted)

Figure 37. PSRR vs Frequency and $C_{OUT}$

$V_{IN} = 3.8$ V, $V_{OUT} = 3.3$ V, $I_{OUT} = 500$ mA

Figure 38. PSRR vs Frequency and $C_{FF}$

$V_{IN} = 3.8$ V, $V_{OUT} = 3.3$ V, $I_{OUT} = 500$ mA

Figure 39. PSRR vs Frequency and $I_{LOAD}$

$V_{IN} = 3.8$ V, $V_{OUT} = 3.3$ V, $C_{OUT} = 2.2$ $\mu$F

Figure 40. Output Spectral Noise Density

$V_{IN} = 3.8$ V, $V_{OUT} = 3.3$ V, $C_{OUT} = 4.7$ $\mu$F

Figure 41. Output Spectral Noise Density

$V_{IN} = 3.8$ V, $V_{OUT} = 3.3$ V, $C_{OUT} = 2.2$ $\mu$F, $V_{RMS}$ BW = 10 Hz to 100 kHz

Figure 42. Output Spectral Noise Density vs Frequency and $C_{FF}$

$V_{IN} = 3.8$ V, $V_{OUT} = 3.3$ V, $I_{OUT} = 500$ mA, $C_{OUT} = 2.2$ $\mu$F, $V_{RMS}$ BW = 10 Hz to 100 kHz
Typical Characteristics (continued)

at operating temperature range $T_J = 25^\circ C$, $V_{IN} = V_{OUT(NOM)} + 0.5 \text{ V or } 1.5 \text{ V (whichever is greater)}$, $I_{OUT} = 1 \text{ mA}$, $V_{EN} = V_{IN}$, and $C_{IN} = C_{OUT} = 1 \mu\text{F}$ (unless otherwise noted).

![Graph](image)

Figure 43. Output Spectral Noise Density vs Frequency and $C_{OUT}$

![Graph](image)

Figure 44. Output Spectral Noise Density vs Frequency

$V_{IN} = 3.8 \text{ V}, V_{OUT} = 3.3 \text{ V}, I_{OUT} = 100 \text{ mA}, C_{FF} = 0 \mu\text{F}$, $V_{RMS} \text{ BW = 10 Hz to 100 kHz}$

$I_{OUT} = 500 \text{ mA}, C_{OUT} = 2.2 \mu\text{F}, V_{RMS} \text{ BW = 10 Hz to 100 kHz}$
7 Detailed Description

7.1 Overview

The TPS746 is a next-generation, low-dropout regulator (LDO). This device consumes low quiescent current and delivers excellent line and load transient performance. These characteristics, combined with low noise and good PSRR with low dropout voltage, make this device ideal for portable consumer applications.

This regulator offers foldback current limit, shutdown, and thermal protection. The operating junction temperature for this device is –40°C to +125°C.

7.2 Functional Block Diagram

7.3 Feature Description

7.3.1 Undervoltage Lockout (UVLO)

The TPS746 uses an undervoltage lockout (UVLO) circuit that disables the output until the input voltage is greater than the rising UVLO voltage (V_UVLO). This circuit ensures that the device does not exhibit any unpredictable behavior when the supply voltage is lower than the operational range of the internal circuitry. When V_IN is less than V_UVLO, the output is connected to ground with a pulldown resistor (R_PULLDOWN).

7.3.2 Shutdown

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed V_EN(HI). Turn off the device by forcing the EN pin to drop below V_EN(LO). If shutdown capability is not required, connect EN to IN.

The TPS746 has an internal pulldown MOSFET that connects an R_PULLDOWN resistor to ground when the device is disabled. The discharge time after disabling depends on the output capacitance (C_OUT) and the load resistance (R_L) in parallel with the pulldown resistor (R_PULLDOWN). Equation 1 calculates the time constant:

\[ \tau = \frac{R_{\text{PULLDOWN}} \times R_L}{R_{\text{PULLDOWN}} + R_L} \]  

(1)
Feature Description (continued)

7.3.3 Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brickwall-foldback scheme. The current limit transitions from a brickwall scheme to a foldback scheme at the foldback voltage \( V_{\text{FOLDBACK}} \). In a high-load current fault with the output voltage above \( V_{\text{FOLDBACK}} \), the brickwall scheme limits the output current to the current limit \( I_{\text{CL}} \). When the voltage drops below \( V_{\text{FOLDBACK}} \), a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit \( I_{\text{SC}} \). \( I_{\text{CL}} \) and \( I_{\text{SC}} \) are listed in the Electrical Characteristics table.

For this device, \( V_{\text{FOLDBACK}} = 0.4 \times V_{\text{OUT(NOM)}} \).

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brickwall current limit, the pass transistor dissipates power \( [(V_{\text{IN}} - V_{\text{OUT}}) \times I_{\text{CL}}] \). When the device output is shorted and the output is below \( V_{\text{FOLDBACK}} \), the pass transistor dissipates power \( [(V_{\text{IN}} - V_{\text{OUT}}) \times I_{\text{SC}}] \). If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the Know Your Limits application report.

Figure 45 shows a diagram of the foldback current limit.

![Figure 45. Foldback Current Limit](image)

7.3.4 Thermal Shutdown

Thermal shutdown protection disables the output when the junction temperature rises to approximately 170°C. Disabling the device eliminates the power dissipated by the device, allowing the device to cool. When the junction temperature cools to approximately 155°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the LDO from damage as a result of overheating.

Activating the thermal shutdown feature usually indicates excessive power dissipation as a result of the product of the \( (V_{\text{IN}} - V_{\text{OUT}}) \) voltage and the load current. For reliable operation, limit junction temperature to 125°C maximum. To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.
Feature Description (continued)

The TPS746 internal protection circuitry protects against overload conditions but is not intended to be activated in normal operation. Continuously running the TPS746 into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

7.4.1 Device Functional Mode Comparison

The Device Functional Mode Comparison table shows the conditions that lead to the different modes of operation. See the Electrical Characteristics table for parameter values.

<table>
<thead>
<tr>
<th>OPERATING MODE</th>
<th>PARAMETER</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal operation</td>
<td>V_{IN} &gt; V_{OUT(nom)} + V_{DO} and V_{IN} &gt; V_{IN(min)}</td>
</tr>
<tr>
<td>Dropout operation</td>
<td>V_{IN(min)} &lt; V_{IN} &lt; V_{OUT(nom)} + V_{DO}</td>
</tr>
<tr>
<td>Disabled (any true condition ...</td>
<td>V_{IN} &lt; V_{UVLO}</td>
</tr>
</tbody>
</table>

7.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage (V_{OUT(nom)} + V_{DO})
- The output current is less than the current limit (I_{OUT} < I_{CL})
- The device junction temperature is less than the thermal shutdown temperature (T_{J} < T_{SD})
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

7.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, V_{IN} < V_{OUT(NOM)} + V_{DO}, directly after being in a normal regulation state, but not during startup), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage (V_{OUT(NOM)} + V_{DO}), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

7.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the enable pin to less than the maximum EN pin low-level input voltage (see the Electrical Characteristics table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Adjustable Device Feedback Resistors

Figure 46 shows that the output voltage of the TPS746 can be adjusted from 0.55 V to 5.5 V by using a resistor divider network.

![Figure 46. Adjustable Operation](image)

The adjustable-version device requires external feedback divider resistors to set the output voltage. \( V_{OUT} \) is set using the feedback divider resistors, \( R_1 \) and \( R_2 \), according to the following equation:

\[
V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right)
\]  

(2)

For this device, \( V_{FB} = 0.55 \text{ V} \).

To ignore the FB pin current error term in the \( V_{OUT} \) equation, set the feedback divider current to 100x the FB pin current listed in the Electrical Characteristics table. This setting provides the maximum feedback divider series resistance, as shown in the following equation:

\[
R_1 + R_2 \leq \frac{V_{OUT}}{(I_{FB} \times 100)}
\]

(3)

For this device, \( I_{FB} = 10 \text{ nA} \).

8.1.2 Input and Output Capacitor Selection

The TPS746 requires an output capacitance of 0.47 \( \mu \text{F} \) or larger for stability. Use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature. When choosing a capacitor for a specific application, pay attention to the dc bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. For best performance, the maximum recommended output capacitance is 220 \( \mu \text{F} \).

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. Some input supplies have a high impedance, thus placing the input capacitor on the input supply helps reduce the input impedance. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the input supply has a high impedance over a large range of frequencies, several input capacitors can be used in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast, rise-time load transients are anticipated, or if the device is located several inches from the input power source.
Application Information (continued)

8.1.3 Dropout Voltage

The TPS746 uses a PMOS pass transistor to achieve low dropout. When \((V_{IN} - V_{OUT})\) is less than the dropout voltage \((V_{DO})\), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the \(R_{DS(ON)}\) of the PMOS pass element. \(V_{DO}\) scales approximately with output current because the PMOS device behaves like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as \((V_{IN} - V_{OUT})\) approaches dropout operation.

8.1.4 Exiting Dropout

Some applications have transients that place the LDO into dropout, such as slower ramps on \(V_{IN}\) during start-up. As with other LDOs, the output may overshoot on recovery from these conditions. A ramping input supply causes an LDO to overshoot on start-up, as shown in Figure 47, when the slew rate and voltage levels are in the correct range. Use an enable signal to avoid this condition.

![Figure 47. Startup Into Dropout](image)

Line transients out of dropout can also cause overshoot on the output of the regulator. These overshoots are caused by the error amplifier having to drive the gate capacitance of the pass element and bring the gate back to the correct voltage for proper regulation. Figure 48 illustrates what is happening internally with the gate voltage and how overshoot can be caused during operation. When the LDO is placed in dropout, the gate voltage \((V_{GS})\) is pulled all the way down to ground to give the pass device the lowest on-resistance as possible. However, if a line transient occurs when the device is in dropout, the loop is not in regulation and can cause the output to overshoot until the loop responds and the output current pulls the output voltage back down into regulation. If these transients are not acceptable, then continue to add input capacitance in the system until the transient is slow enough to reduce the overshoot.
Application Information (continued)

8.1.5 Reverse Current

As with most LDOs, excessive reverse current can damage this device. Reverse current flows through the body diode on the pass element instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device, as a result of one of the following conditions:

- Degradation caused by electromigration
- Excessive heat dissipation
- Potential for a latch-up condition

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} > V_{IN} + 0.3\,\text{V}$:

- If the device has a large $C_{OUT}$ and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply
Application Information (continued)

If reverse current flow is expected in the application, external protection must be used to protect the device. Figure 49 shows one approach of protecting the device.

![Figure 49. Example Circuit for Reverse Current Protection Using a Schottky Diode](image)

8.1.6 Power Dissipation ($P_D$)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Equation 4 calculates power dissipation ($P_D$).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$  \hspace{1cm} (4)

**NOTE**

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature ($T_A$) for the device. According to Equation 5, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{JUA}$) of the combined PCB and device package and the temperature of the ambient air ($T_A$).

$$T_J = T_A + (R_{JUA} \times P_D)$$  \hspace{1cm} (5)

Thermal resistance ($R_{JUA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the Thermal Information table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

8.1.7 Power-Good Function

The power-good circuit monitors the voltage at the feedback pin to indicate the status of the output voltage. When the output voltage falls below the PG threshold voltage ($PG_{LTH}$), the PG pin open-drain output engages and pulls the PG pin close to GND. When the output voltage exceeds $PG_{HTH}$, the PG pin becomes high impedance. By connecting a pullup resistor to an external supply, any downstream device can receive power-good as a logic signal that can be used for sequencing. Make sure that the external pullup supply voltage results in a valid logic signal for the receiving device. Using a pullup resistor from 10 kΩ to 100 kΩ is recommended.
Application Information (continued)

When using a feed-forward capacitor ($C_{FF}$), the time constant for the LDO startup is increased whereas the power-good output time constant stays the same, possibly resulting in an invalid status of the power-good output. To avoid this issue, and to receive a valid PG output, make sure that the time constant of both the LDO startup and the power-good output match, which can be done by adding a capacitor in parallel with the power-good pullup resistor. For more information, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application report.

The state of PG is only valid when the device operates above the minimum input voltage of the device and power-good is asserted, regardless of the output voltage state when the input voltage falls below the UVLO threshold minus the UVLO hysteresis. When the input voltage falls below approximately 0.8 V, there is not enough gate drive voltage to keep the open-drain, power-good device turned on and the power-good output pulled high. Connecting the power-good pullup resistor to the output voltage can help minimize this effect.

### 8.2 Feed-Forward Capacitor ($C_{FF}$)

For the adjustable-voltage version device, a feed-forward capacitor ($C_{FF}$) can be connected from the OUT pin to the FB pin. $C_{FF}$ improves transient, noise, and PSRR performance, but is not required for regulator stability. Recommended $C_{FF}$ values are listed in the *Recommended Operating Conditions* table. A higher capacitance $C_{FF}$ can be used; however, the startup time increases. For a detailed description of $C_{FF}$ tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application report.
8.3 Typical Application

Figure 50 shows the typical application circuit for the TPS746. Input and output capacitances must be at least 1 µF.

![Typical Application Circuit](image)

Figure 50. TPS746 Typical Application

8.3.1 Design Requirements

Use the parameters listed in Table 2 for typical linear regulator applications.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>DESIGN REQUIREMENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
<td>3.8 V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>3.3 V, ±1%</td>
</tr>
<tr>
<td>Input current</td>
<td>1 A (maximum)</td>
</tr>
<tr>
<td>Output load</td>
<td>1-A DC</td>
</tr>
<tr>
<td>Maximum ambient temperature</td>
<td>70°C</td>
</tr>
</tbody>
</table>

8.3.2 Detailed Design Procedure

Input and output capacitors are required to achieve the output voltage transient requirements. Capacitance values of 2.2 µF are selected to give the maximum output capacitance in a small, low-cost package; see the Input and Output Capacitor Selection section for details.

Figure 46 illustrates the output voltage of the TPS746. Set the output voltage using the resistor divider; see the section for details.

8.3.2.1 Input Current

During normal operation, the input current to the LDO is approximately equal to the output current of the LDO. During startup, the input current is higher as a result of the inrush current charging the output capacitor. Use Equation 6 to calculate the current through the input.

\[
I_{\text{in}(t)} = \left( \frac{C_{\text{out}} \times dV_{\text{out}}(t)}{dt} \right) + \left( \frac{V_{\text{out}}(t)}{R_{\text{LOAD}}} \right)
\]

where:
- \( V_{\text{out}}(t) \) is the instantaneous output voltage of the turn-on ramp
- \( dV_{\text{out}}(t) / dt \) is the slope of the \( V_{\text{out}} \) ramp
- \( R_{\text{LOAD}} \) is the resistive load impedance

8.3.2.2 Thermal Dissipation

The junction temperature can be determined using the junction-to-ambient thermal resistance (\( R_{\text{jua}} \)) and the total power dissipation (\( P_{\text{D}} \)). Use Equation 7 to calculate the power dissipation. Multiply \( P_{\text{D}} \) by \( R_{\text{jua}} \) as Equation 8 shows and add the ambient temperature (\( T_{\text{A}} \)) to calculate the junction temperature (\( T_{\text{J}} \)).

\[
P_{\text{D}} = (I_{\text{GND}} + I_{\text{OUT}}) \times (V_{\text{IN}} - V_{\text{OUT}})
\]

\[
T_{\text{J}} = R_{\text{jua}} \times P_{\text{D}} + T_{\text{A}}
\]
Calculate the maximum ambient temperature as Equation 9 shows if the \( T_{J(MAX)} \) value does not exceed 125°C. Equation 10 calculates the maximum ambient temperature with a value of 84.85°C.

\[
T_{A(MAX)} = T_{J(MAX)} - R_{\text{UA}} \times P_D \\
T_{A(MAX)} = 125°C - 80.3°C/\text{W} \times (3.8 \text{ V} - 3.3 \text{ V}) \times (1 \text{ A}) = 84.85°C
\]  

**8.3.3 Application Curve**

\( V_{IN} = 3.8 \text{ V}, \ V_{OUT} = 3.3 \text{ V}, \ C_{OUT} = 2.2 \ \mu \text{F} \)

Figure 51. PSRR vs Frequency and \( I_{LOAD} \)
9 Power Supply Recommendations

Connect a low output impedance power supply directly to the IN pin of the TPS746.

10 Layout

10.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections in order to optimize thermal performance.
- Place thermal vias around the device to distribute heat.
- Do not place a thermal via directly beneath the thermal pad of the DRV package. A via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.

10.2 Layout Example

![Layout Example for the DRV Package](image)

**Figure 52. Layout Example for the DRV Package**
11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation
For related documentation see the following:

Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator application report

11.2 Receiving Notification of Documentation Updates
To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary
SLYZ022 — TI Glossary.
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS74601PBDRVR</td>
<td>ACTIVE</td>
<td>WSON</td>
<td>DRV</td>
<td>6</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>1MFH</td>
</tr>
<tr>
<td>TPS74601PBDRVT</td>
<td>ACTIVE</td>
<td>WSON</td>
<td>DRV</td>
<td>6</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>1MFH</td>
</tr>
<tr>
<td>TPS74601PDRVR</td>
<td>ACTIVE</td>
<td>WSON</td>
<td>DRV</td>
<td>6</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>1MDH</td>
</tr>
<tr>
<td>TPS74601PDRVT</td>
<td>ACTIVE</td>
<td>WSON</td>
<td>DRV</td>
<td>6</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>1MDH</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead/Ball Finish** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS746:

• Automotive: TPS746-Q1

NOTE: Qualified Version Definitions:

• Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
## TAPE AND REEL INFORMATION

### TAPE DIMENSIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin 1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS74601PBDRVR</td>
<td>WSON</td>
<td>DRV</td>
<td>6</td>
<td>3000</td>
<td>180.0</td>
<td>8.4</td>
<td>2.3</td>
<td>2.3</td>
<td>1.15</td>
<td>4.0</td>
<td>8.0</td>
<td>Q2</td>
</tr>
<tr>
<td>TPS74601PBDRVT</td>
<td>WSON</td>
<td>DRV</td>
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<td>4.0</td>
<td>8.0</td>
<td>Q2</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.*

---

### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

### REEL DIMENSIONS

- **Reel Diameter**
- **Reel Width W1**

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- **Sprocket Holes**
- **User Direction of Feed**
- **Pocket Quadrants**

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*www.ti.com 2-Dec-2018*
**PACKAGE MATERIALS INFORMATION**

**TAPE AND REEL BOX DIMENSIONS**

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
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<th>Height (mm)</th>
</tr>
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<td>WSON</td>
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<td>6</td>
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<td>185.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
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