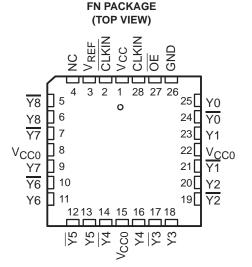
SCAS321G - SEPTEMBER 1993 - REVISED AUGUST 1999

- Low-Output Skew for Clock-Distribution Applications
- Differential Low-Voltage Pseudo-ECL (LVPECL)-Compatible Inputs and Outputs
- Distributes Differential Clock Inputs to Nine Differential Clock Outputs
- Output Reference Voltage, V_{REF}, Allows Distribution From a Single-Ended Clock Input
- Single-Ended LVPECL-Compatible Output Enable
- Packaged in Plastic Chip Carrier

description

The differential LVPECL clock-driver circuit distributes one pair of differential LVPECL clock inputs (CLKIN, $\overline{\text{CLKIN}}$) to nine pairs of differential clock (Y, $\overline{\text{Y}}$) outputs with minimum skew for clock distribution. It is specifically designed for driving $50-\Omega$ transmission lines.



NC - No internal connection

When the output-enable (\overline{OE}) is low, the nine differential outputs switch at the same frequency as the differential clock inputs. When \overline{OE} is high, the nine differential outputs are in static states (Y outputs are in the low state, \overline{Y} outputs are in the high state).

The V_{RFF} output can be strapped to the CLKIN input for a single-ended CLKIN input.

The CDC111 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

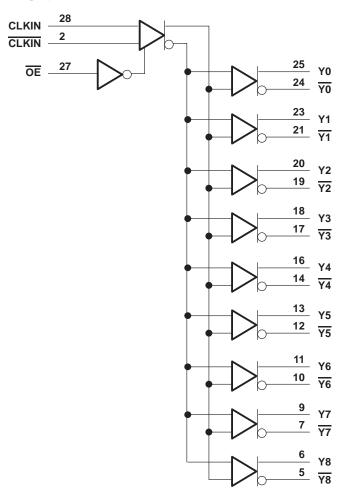
	INPUTS	OUTI	OUTPUTS		
CLKIN	CLKIN	OE	Yn	Yn	
Х	Х	Н	L	Н	
L	Н	L	L	Н	
Н	L	L	Н	L	
L	V_{REF}	L	L	Н	
Н	V_{REF}	L	Н	L	
VREF	L	L	Н	L	
VREF	Н	L	L	Н	



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, V _O (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	–18 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	–50 mA
Continuous current through V _{CC} or GND	$\dots \dots \pm 80 \text{ mA}$
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 2)	525 mW
Storage temperature range, T _{stg}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. The maximum package power dissipation is calculated using a juction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.



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recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
Vсс	Supply voltage		3	3.6	V
V	High level input voltage	V _{CC} = 3 V to 3.6 V	V _{CC} -1.165	V _{CC} -0.88	V
ViH	High-level input voltage	2.135	2.420	V	
.,	V _{CC} = 3 V to 3.6 V		V _{CC} -1.81	V _{CC} -1.475	V
VIL	Low-level input voltage	V _{CC} = 3.3 V	1.49	1.825	V
TA	Operating free-air temperature		0	70	°C
fclock	Input frequency			500	MHz

NOTE 3: V_{CC} = V_{CCO}

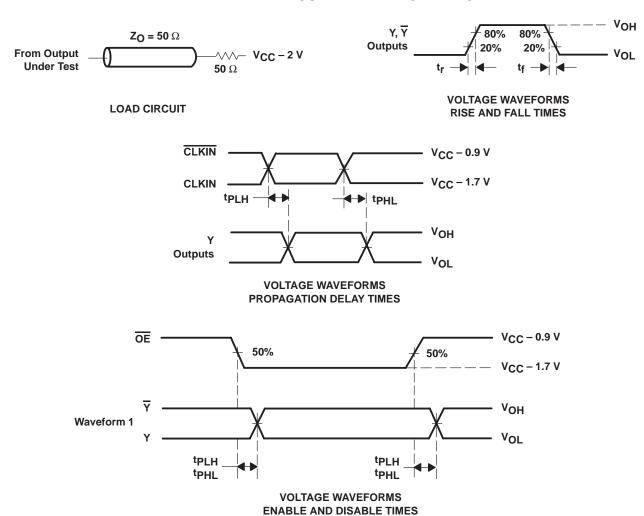
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
\/	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	V _{CC} -1.38	V _{CC} -1.26	V
VREF	V _{CC} = 3.3 V	1.92	2.04	V
Vall	V _{CC} = 3 V to 3.6 V	V _{CC} -1.025	V _{CC} -0.88	V
VOH	V _{CC} = 3.3 V	2.275	2.42	V
Val	V _{CC} = 3 V to 3.6 V	V _{CC} -1.81	V _{CC} -1.62	V
VOL	V _{CC} = 3.3 V	1.49	1.68	V
lį	$V_{I} = 2.4 \text{ V},$ $V_{CC} = 3.6 \text{ V}$		150	μΑ
Icc	$I_{O} = 0,$ $V_{CC} = 3.6 V$		80	mA

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
^t PLH	CLKIN, CLKIN	Y, \overline{Y}	450	600	nc
^t PHL	CLNIN, CLNIN	Υ, Υ	450	600	ps
t _{PHL}	ŌĒ	Y, \overline{Y}		900	ps
t _{sk(o)}		Y, \overline{Y}		50	ps
tsk(pr)		Y, \overline{Y}		150	ps
t _r		Y, \overline{Y}	200	600	ps
t _f		Y, \overline{Y}	200	600	ps

PARAMETER MEASUREMENT INFORMATION



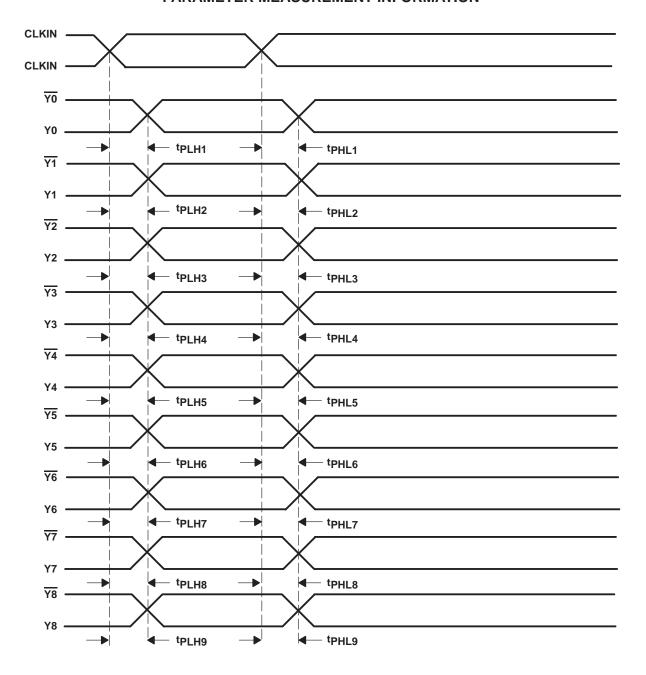
NOTES: A. All input pulses are supplied by generators having the following characteristics: PRR \leq 45 MHz, $Z_Q = 50~\Omega$, $t_f \leq$ 1 ns. $t_f \leq$ 1 ns.

- B. Waveform 1 is for a Y output with internal conditions such that the output is high except when disabled by the output control, and for a Y output with internal conditions such that the output is low except when disabled by the output control.
- C. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output skew, $t_{Sk(0)}$, is calculated as the greater of:

- The difference between the fastest and slowest t_{PLHn} (n = 1, 2, . . . 9)
- The difference between the fastest and slowest t_{PHLn} (n = 1, 2, . . . 9)
- B. Process skew, t_{Sk(pr)}, is calculated as the greater of:

 The difference between the fastest and slowest t_{PLHn} (n = 1, 2, ... 9)

 The difference between the fastest and slowest t_{PHLn} (n = 1, 2, ... 9) across multiple devices

Figure 2. Waveforms for Calculation of $t_{sk(o)}$, $t_{sk(pr)}$







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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CDC111FN	ACTIVE	PLCC	FN	28	37	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDC111FNR	ACTIVE	PLCC	FN	28	750	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDC111FNRG4	ACTIVE	PLCC	FN	28	750	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
CDC111FN	Obsolete	Production	PLCC (FN) 28	-	-	Call TI	Call TI	0 to 70	CDC111FN

⁽¹⁾ Status: For more details on status, see our product life cycle.

- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

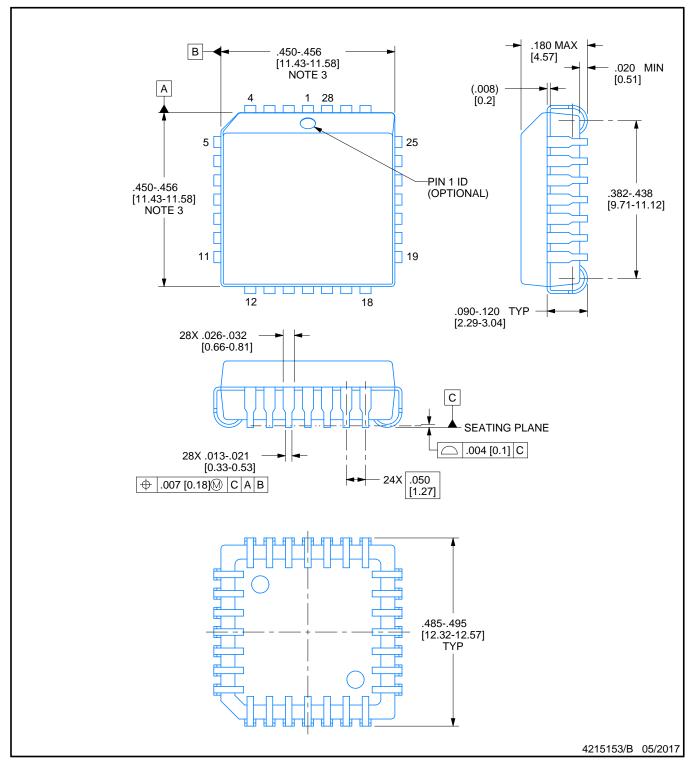


Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

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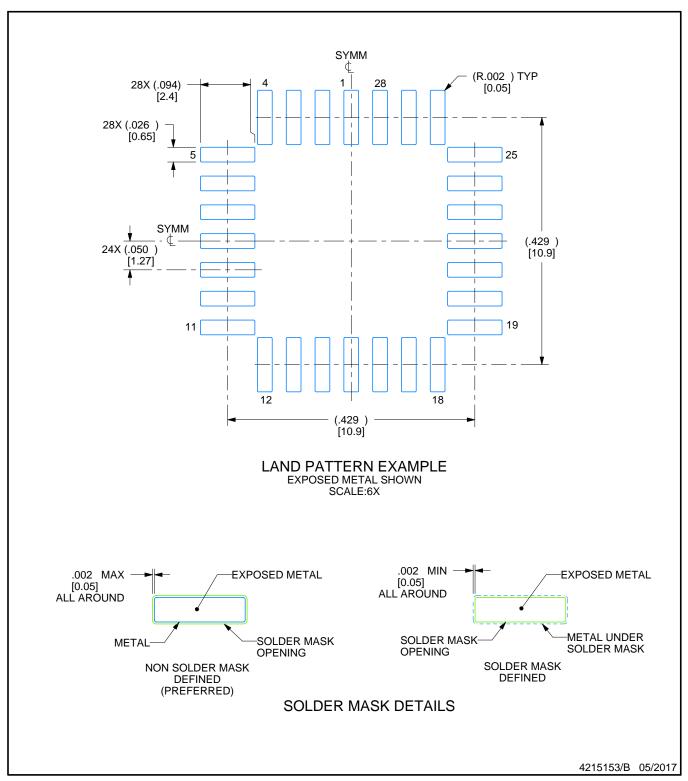




NOTES:

- 1. All linear dimensions are in inches. Any dimensions in brackets are in millimeters. Any dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. Dimension does not include mold protrusion. Maximum allowable mold protrusion .01 in [0.25 mm] per side. 4. Reference JEDEC registration MS-018.



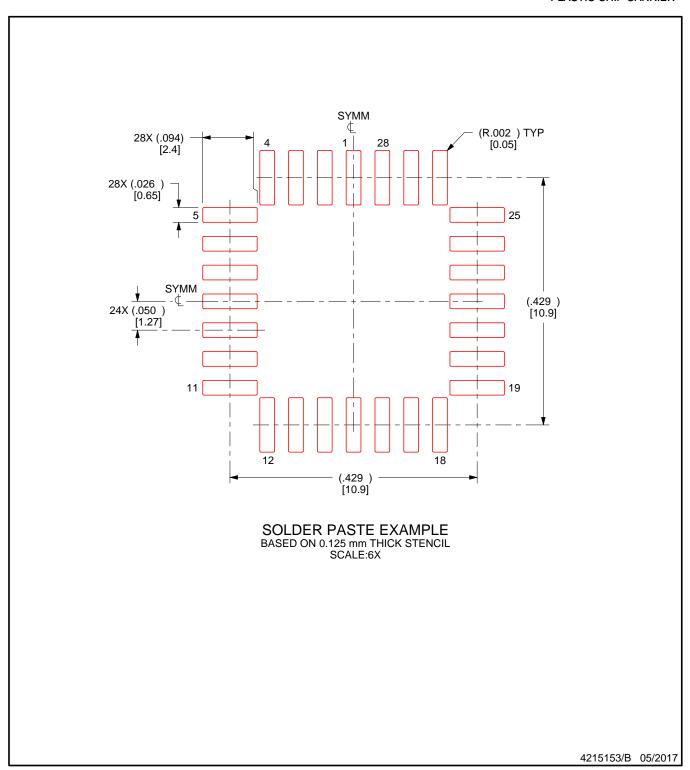


NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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