

Clock Buffer/Clock Multiplier With Optional SSC

Check for Samples: [CDCS503-Q1](#)

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Test Guidance With the Following Results:
 - Device Temperature Grade 2
 - -40°C to 105°C Ambient Operating Temperature Range
 - Device HBM ESD Classification Level H2
 - Device CDM ESD Classification Level C3B
- Part of a Family of Easy to Use Clock Generator Devices With Optional Spread Spectrum Clocking (SSC)
- Clock Multiplier With Selectable Output Frequency and Selectable SSC
- SSC Controllable Through Two External Pins
 - $\pm 0\%$, $\pm 0.5\%$, $\pm 1\%$, $\pm 2\%$ Center Spread
- Frequency Multiplication Selectable Between x1 or x4 With One External Control Pin

- Output Disable Through Control Pin
- Single 3.3 V Device Power Supply
- Wide Temperature Range -40°C to 105°C
- Low Space Consumption 8-Pin TSSOP Package

APPLICATIONS

- Automotive Applications Requiring EMI Reduction Through SSC and/or Clock Multiplication

IN	1	8	VDD
SSC_SEL 0	2	7	OE
SSC_SEL 1	3	6	OUT
GND	4	5	FS

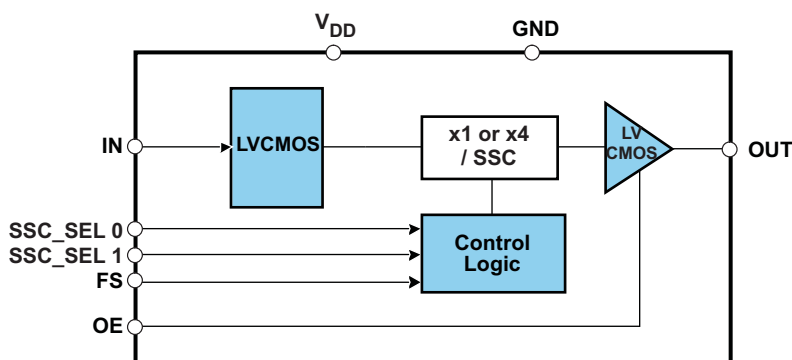


Figure 1. BLOCK DIAGRAM



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DESCRIPTION

The CDCS503-Q1 device is a spread spectrum capable, LVCMOS input clock buffer with selectable frequency multiplication.

It shares major functionality with the CDCS502 but uses a LVCMOS input stage instead of the crystal input stage of the CDCS502, and the CDCS503-Q1 has an output enable pin.

The device accepts a 3.3-V LVCMOS signal at the input.

The input signal is processed by a phased-locked loop (PLL), whose output frequency is either equal to the input frequency or multiplied by the factor of four.

The PLL is also able to spread the clock signal by $\pm 0\%$, $\pm 0.5\%$, $\pm 1\%$ or $\pm 2\%$ centered around the output clock frequency with a triangular modulation.

By this, the device can generate output frequencies between 8 MHz and 108 MHz with or without SSC.

A separate control pin can be used to enable or disable the output. The CDCS503-Q1 device operates in a 3.3-V environment.

It is characterized for operation from -40°C to 105°C , and available in an 8-pin TSSOP package.

Table 1. FUNCTION TABLE

OE	FS	SSC_SEL 0	SSC_SEL 1	SSC AMOUNT	$f_{\text{OUT}}/f_{\text{IN}}$	f_{OUT} at $f_{\text{in}} = 27 \text{ MHz}$
0	x	x	x	x	x	3-state
1	0	0	0	$\pm 0.00\%$	1	27 MHz
1	0	0	1	$\pm 0.50\%$	1	27 MHz
1	0	1	0	$\pm 1.00\%$	1	27 MHz
1	0	1	1	$\pm 2.00\%$	1	27 MHz
1	1	0	0	$\pm 0.00\%$	4	108 MHz
1	1	0	1	$\pm 0.50\%$	4	108 MHz
1	1	1	0	$\pm 1.00\%$	4	108 MHz
1	1	1	1	$\pm 2.00\%$	4	108 MHz

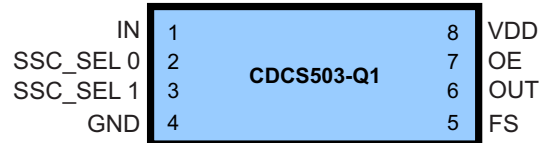


This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DEVICE INFORMATION

PACKAGE



PIN FUNCTIONS

SIGNAL	PIN	TYPE	DESCRIPTION
IN	1	I	LVC MOS clock input
OUT	6	O	LVC MOS clock output
SSC_SEL 0, 1	2, 3	I	Spread selection pins, internal pullup
OE	7	I	Output enable, internal pullup
FS	5	I	Frequency multiplication selection, internal pullup
VDD	8	Power	3.3-V power supply
GND	4	Ground	Ground

ORDERING INFORMATION

T _A	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 105°C	TSSOP 2000	CDCS503TPWRQ1	CS503Q

PACKAGE THERMAL RESISTANCE FOR TSSOP (PW) PACKAGE

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

PW 8-PIN TSSOP				THERMAL AIRFLOW (CFM)				UNIT
				0	150	250	500	
R _{θJA}	High K			149	142	138	132	°C/W
	Low K			230	185	170	150	
R _{θJC}	High K	65						°C/W
	Low K	69						

(1) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		CDCS503TPWRQ1	UNIT
		PW (8 PINS)	
θ _{JA}	Junction-to-ambient thermal resistance	179.9	°C/W
θ _{JCTop}	Junction-to-case (top) thermal resistance	64.9	
θ _{JB}	Junction-to-board thermal resistance	108.7	
ψ _{JT}	Junction-to-top characterization parameter	9	
ψ _{JB}	Junction-to-board characterization parameter	107	
θ _{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
V_{DD}	Supply voltage range	–0.5 to 4.6	V
V_{IN}	Input voltage range	–0.5 to 4.6	V
V_{out}	Output voltage range	–0.5 to 4.6	V
I_{IN}	Input current ($V_I < 0$, $V_I > V_{DD}$)	20	mA
I_{out}	Continuous output current	50	mA
T_{ST}	Storage temperature range	–65 to 150	°C
T_J	Maximum junction temperature	125	°C
ESD Rating	Human-body model (HBM) AEC-Q100 classification level H2	1.5	kV
	Charged-device model (CDM) AEC-Q100 classification level C3B	750	V

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V _{DD}	Supply voltage		3		3.6	V
f _{IN}	Input frequency	FS = 0	8		32	MHz
		FS = 1	8		27	
V _{IL}	Low-level input voltage LVCMOS				0.3 V _{DD}	V
V _{IH}	High-level input voltage LVCMOS		0.7 V _{DD}			V
V _I	Input voltage threshold LVCMOS			0.5 V _{DD}		V
C _L	Output load test LVCMOS				15	pF
I _{OH} /I _{OL}	Output current				±12	mA
T _A	Operating free-air temperature		–40		105	°C

DEVICE CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{DD}	f _{out} = 20 MHz; FS = 0, no SSC		19		mA
	f _{out} = 70 MHz; FS = 1, SSC = 2%		22		
f _{OUT}	FS = 0	8		32	MHz
	FS = 1	32		108	
I _{IH}	V _I = V _{DD} ; V _{DD} = 3.6 V			10	μA
I _{IL}	V _I = 0 V; V _{DD} = 3.6 V			–10	μA
V _{OH}	I _{OH} = –0.1 mA	2.9			V
	I _{OH} = –8 mA	2.4			
	I _{OH} = –12 mA	2.2			
V _{OL}	I _{OL} = 0.1 mA			0.1	V
	I _{OL} = 8 mA			0.5	
	I _{OL} = 12 mA			0.8	
I _{OZ}	OE = Low	–2		2	μA
t _{JIT(C-C)}	f _{out} = 108 MHz; FS = 1, SSC = 1%, 10000 Cycles		110		ps
t _r /t _f	20%–80%		0.75		ns
O _{dc}		45%		55%	
f _{MOD}			30		kHz

(1) Measured with Test Load, see [Figure 3](#).

(2) Not production tested.

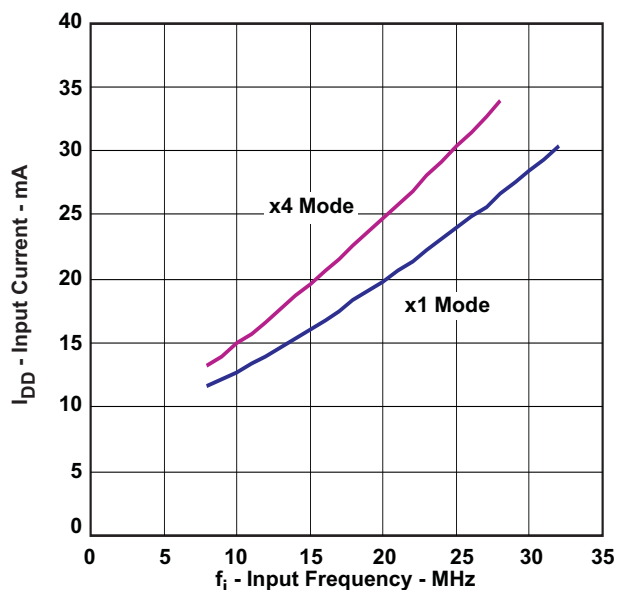


Figure 2. I_{DD} vs Input Frequency, $V_{CC} = 3.3\text{ V}$, SSC = 2%, Output Loaded With Test Load

APPLICATION INFORMATION

SSC MODULATION

The exact implementation of the SSC modulation plays a vital role for the EMI reduction. The CDCS503-Q1 device uses a triangular modulation scheme implemented in a way that the modulation frequency depends on the VCO frequency of the internal PLL and the spread amount is independent from the VCO frequency.

The modulation frequency can be calculated by using one of the below formulas chosen by frequency multiplication mode.

$$\text{FS} = 0: f_{\text{mod}} = f_{\text{IN}} / 708$$

$$\text{FS} = 1: f_{\text{mod}} = f_{\text{IN}} / 620$$

PARAMETER MEASUREMENT INFORMATION

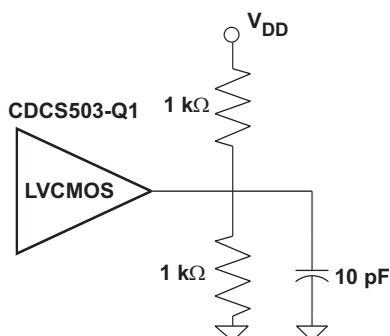


Figure 3. Test Load

PARAMETER MEASUREMENT INFORMATION (continued)

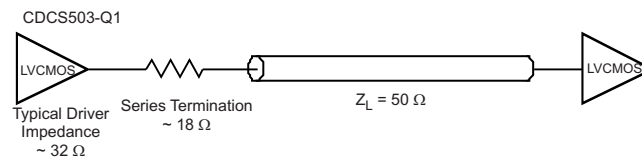


Figure 4. Load for 50-Ω Board Environment

REVISION HISTORY

Changes from Revision A (June 2012) to Revision B	Page
• Changed AEC Q100 Qualified to AEC Q100 Test Guidance in FAD.	1

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CDCS503TPWRQ1	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	CS503Q
CDCS503TPWRQ1.B	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	CS503Q

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF CDCS503-Q1 :

- Catalog : [CDCS503](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCS503TPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCS503TPWRQ1	TSSOP	PW	8	2000	353.0	353.0	32.0

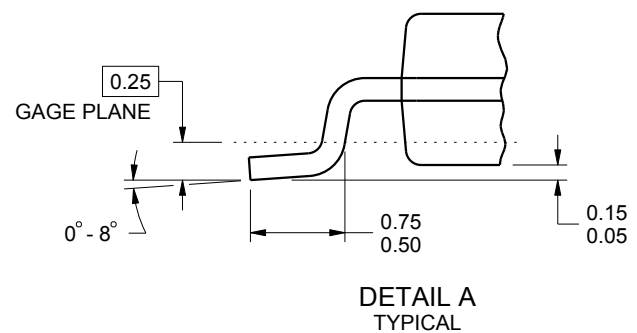
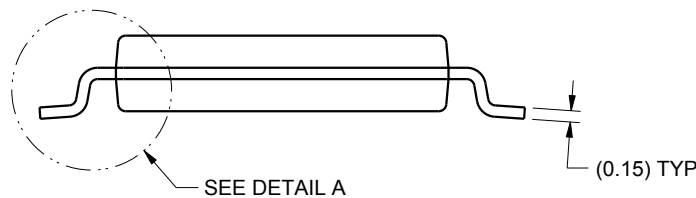
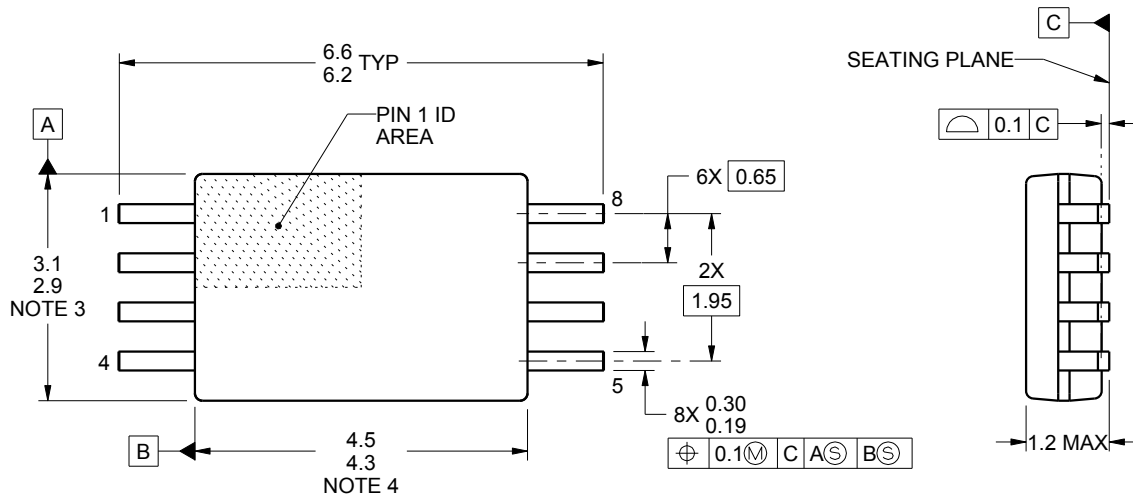
PW0008A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



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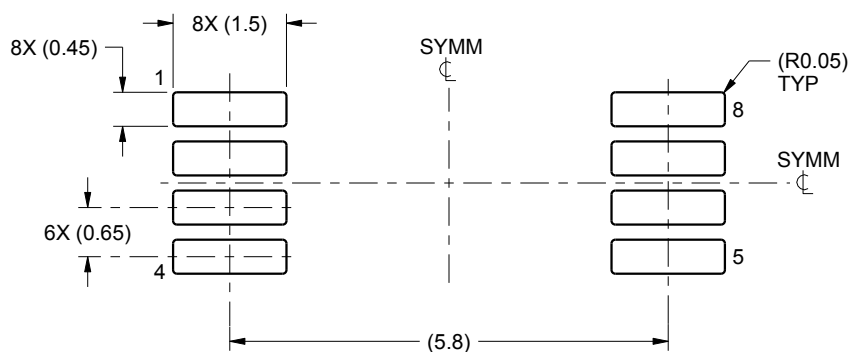
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

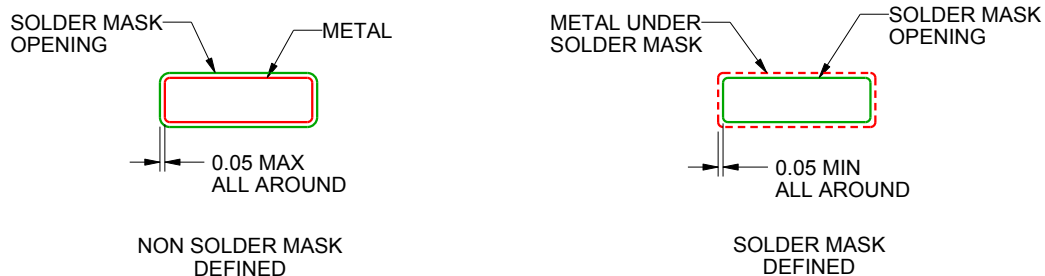
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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