SN54LVT8986, SN74LVT8986
3.3-V LINKING ADDRESSABLE SCAN PORTS
MULTIDROP-ADDRESSABLE IEEE STD 1149.1 (JTAG) TAP TRANSCEIVERS

SCBS759E – OCTOBER 2002 – REVISED MAY 2007

FEATURES

- **Members of the Texas Instruments (TI) Family of JTAG Scan-Support Products**
- **Extend Scan Access From Board Level to Higher Level of System Integration**
- **Three IEEE Std 1149.1-Compatible Configurable Secondary Scan Paths to One Primary Scan Path**
- **Multiple Devices Can Be Cascaded to Link 24 Secondary Scan Paths to One Primary Scan Path**
- **Simple (Linking Shadow) Protocol Is Used to Connect the Primary Test Access Port (TAP) to Secondary TAPs. This Single Protocol Is Used to Address and Configure the Secondary Scan Path.**
- **LASP (8986) and ASP (8996) Can Be Configured on the Same Backplane Using Similar Shadow Protocols**
- **Linking Shadow Protocols Can Occur in Any of Test Logic Reset, Run Test/Idle, Pause DR, Pause IR TAP States to Provide Board-to-Board and Built In Self Test**
- **Bypass ($\overline{BYP_5}$–$\overline{BYP_0}$) Forces Primary to Configured Secondary Paths Without Use of Linking Shadow Protocols**
- **Connect ($\overline{CON_2}$–$\overline{CON_0}$) Provides Indication of Primary-to-Secondary Paths Connections**
- **Secondary TAPs Can Be Configured at High Impedance Via the $\overline{OE}$ Input to Allow an Alternate Test Master to Take Control of the Secondary TAPs**
- **High-Drive Outputs (–32 mA I_{OH}, 64 mA I_{OL}) Support Backplane Interface at Primary Outputs and High Fanout at Secondary Outputs**
- **While Powered at 3.3 V, Both Primary and Secondary TAPs Are Fully 5 V Tolerant for Interfacing 5 V and/or 3.3 V Masters and Targets**
- **Package Options Include Plastic BGA (GGV) and LQFP (PM) Packages and Ceramic Quad Flat (HV) Packages Using 25-mil Center-to-Center Spacing**

DESCRIPTION/ORDERING INFORMATION

The 'LVT8986 linking addressable scan ports (LASPs) are members of the TI family of IEEE Std 1149.1 (JTAG) scan-support products. The scan-support product family facilitates testing of fully boundary-scannable devices. The LASP applies linking shadow protocols through the test access port (TAP) to extend scan access to the system level and divide scan chains at the board level.

The LASP consists of a primary TAP for interfacing to the backplane IEEE Std 1149.1 serial-bus signals (PTDI, PTMS, PTCK, PTDO, $\overline{PRTST}$) and three secondary TAPs for interfacing to the board-level IEEE Std 1149.1 serial-bus signals. Each secondary TAP consists of signals $STDI_x$, $STMS_x$, $STCK_x$, $STDO_x$, and $\overline{STRST_x}$. Conceptually, the LASP is a gateway device that can be used to connect a set of primary TAP signals to a set of secondary TAP signals – for example, to interface backplane TAP signals to a board-level TAP. The LASP provides all signal buffering that might be required at these two interfaces. Primary-to-secondary TAP connections can be configured with the help of linking shadow protocol or protocol bypass ($\overline{BYP_5}$–$\overline{BYP_0}$) inputs. All possible configurations are tabulated in Function Tables 1, 2, and 3.

ORDERING INFORMATION

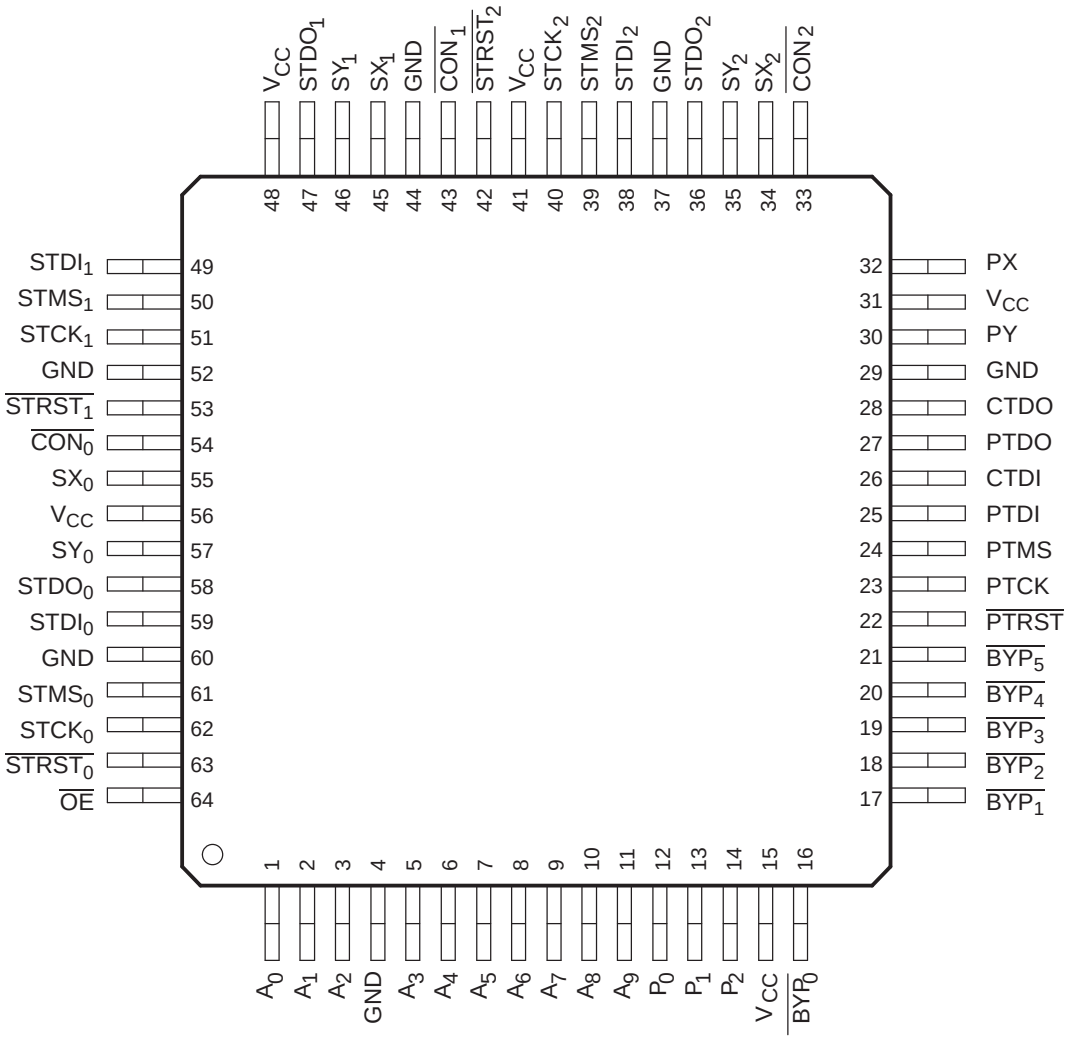
T_A	PACKAGE(1)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PBGA – GGV	SN74LVT8986GGV	LVT8986
	PBGA – ZGV	SN74LVT8986ZGV	LVT8986
	LQFP – PM	SN74LVT8986PM	LVT8986
–55°C to 125°C	CFP – HV	SNJ54LVT8986HV	SNJ54LVT8986HV

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

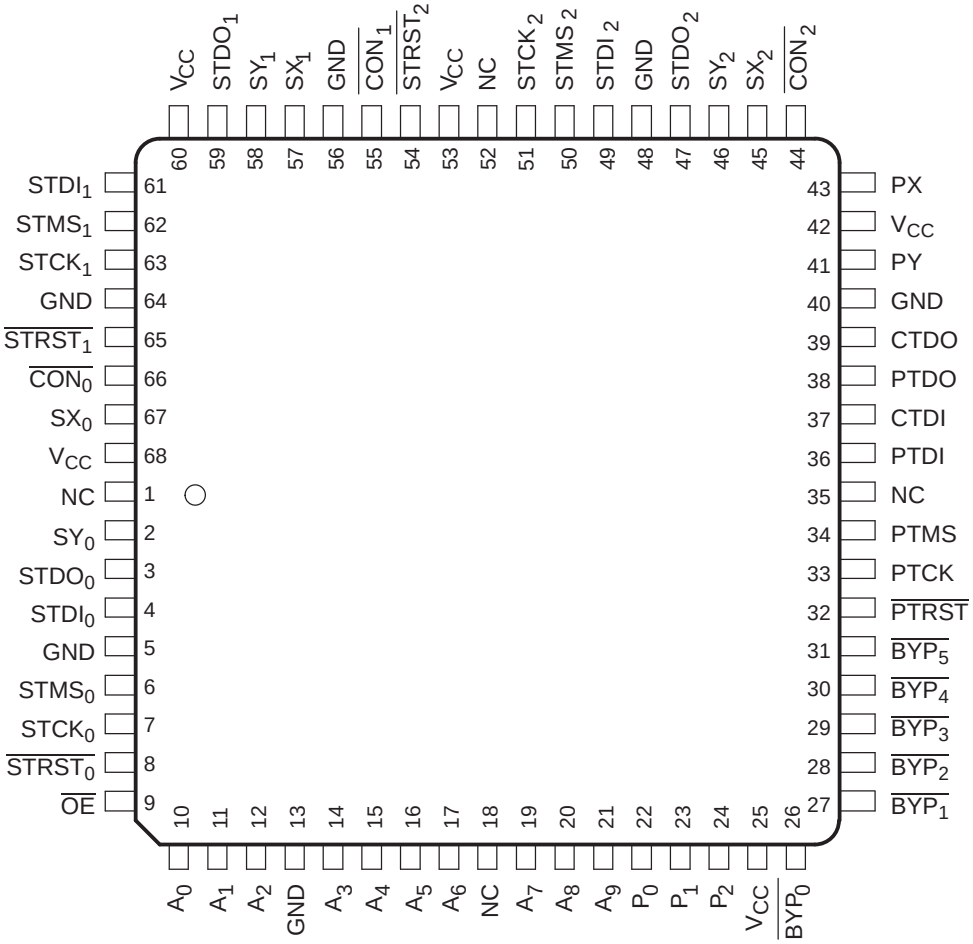
GGV PACKAGE (TOP VIEW)

	1	2	3	4	5	6	7	8
A	A_0	$\overline{STRST_0}$	GND	$STDO_0$	SX_O	GND	$STMS_1$	$STDI_1$
B	A_1	$\overline{OE}$	$STMS_0$	SY_0	V_{CC}	$STCK_1$	V_{CC}	$STDO_1$
C	GND	A_2	$STCK_0$	$STDI_0$	$\overline{CON_0}$	SY_1	GND	SX_1
D	A_5	A_6	A_4	A_3	$\overline{STRST_1}$	$\overline{CON_1}$	V_{CC}	$\overline{STRST_2}$
E	A_8	A_7	A_9	$\overline{BYP_5}$	GND	$STDI_2$	$STCK_2$	$STMS_2$
F	P_0	P_1	P_2	$\overline{PTRST}$	PTDO	PY	SY_2	$STDO_2$
G	V_{CC}	$\overline{BYP_0}$	$\overline{BYP_3}$	PTMS	PTDI	GND	PX	SX_2
H	$\overline{BYP_1}$	$\overline{BYP_2}$	$\overline{BYP_4}$	PTCK	CTDI	CTDO	V_{CC}	$\overline{CON_2}$

SN74LVT8986 . . . PM PACKAGE
(TOP VIEW)



SN54LVT8986 . . . HV PACKAGE
(TOP VIEW)



NC − No internal connection

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

Most operations of the LASP are synchronous to the primary test clock (PTCK) input. PTCK always is buffered directly onto the secondary test clock ($STCK_2$–$STCK_0$) outputs. Upon power up of the device, the LASP assumes a condition in which the primary TAP is disconnected from the secondary TAPs (unless the bypass signals are used, as shown in Function Tables 1 and 2). This reset condition also can be entered by asserting the primary test reset ($\overline{PTRST}$) input or by using the linking shadow protocol. $\overline{PTRST}$ always is buffered directly onto the secondary test reset ($\overline{STRST_2}$–$\overline{STRST_0}$) outputs, ensuring that the LASP and its associated secondary TAPs can be reset simultaneously. The primary test data output (PTDO) can be configured to receive secondary test data inputs ($STDI_2$–$STDI_0$). Secondary test data outputs ($STDO_2$–$STDO_0$) can be configured to receive either the primary test data input (PTDI), $STDI_2$–$STDI_0$, or the cascade test data input (CTDI). Cascade test data output (CTDO) can be configured to receive either of $STDI_2$–$STDI_0$, or CTDI. CTDI and CTDO facilitate cascading multiple LASPs, which is explained in the latter part of this section. Similarly, secondary test-mode select ($STMS_2$–$STMS_0$) outputs can be configured to receive the primary test-mode select (PTMS) input. When any secondary TAP is disconnected, its respective STDO is at high impedance. Upon disconnecting the secondary TAP, the corresponding STMS holds its last low or high level, allowing the secondary TAP to be held in its last stable state.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

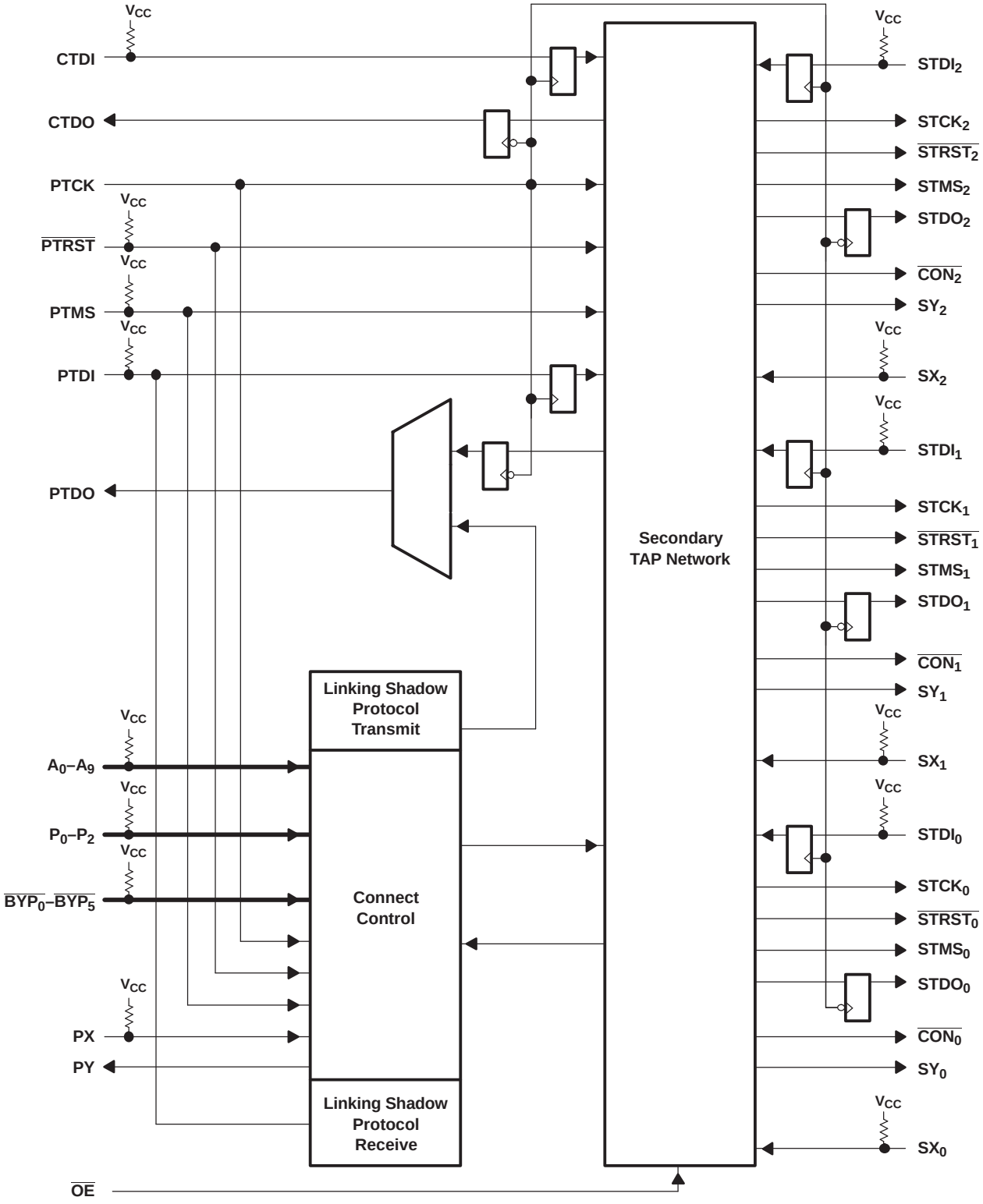
The address (A_9–A_0) inputs to the LASP are used to identify the LASP. The position (P_2–P_0) inputs to the LASP are used to identify the position of the LASP within a cascade chain when multiple LASPs are cascaded. Up to 8 LASPs can be cascaded to link a maximum of 24 secondary scan paths to 1 primary scan path.

In a system, primary-to-secondary connection is based on linking shadow protocols that are received and acknowledged on PTDI and PTDO, respectively. These protocols can occur in any of the stable TAP states, other than Shift-DR or Shift-IR (i.e., Test-Logic-Reset, Run-Test/Idle, Pause-DR or Pause-IR). The essential nature of the protocols is to receive/transmit an address, position the LASP in the cascade chain that is being configured, and configuration of secondary TAPs via a serial bit-pair signaling scheme. When address and position bits received serially at PTDI match those at the parallel address (A_9–A_0) inputs and position (P_2–P_0) inputs respectively, the secondary TAPs are configured per the configuration bits received during the linking shadow protocol, then LASP serially retransmits the entire linking shadow protocol as an acknowledgment and assumes the connected (ON) status. If the received address or position does not match that at the address (A_9–A_0) inputs or position (P_2–P_0) inputs, the LASP immediately assumes the disconnected (OFF) status, without acknowledgment.

The LASP also supports three dedicated addresses that can be received globally (that is, to which all LASPs respond) during shadow protocols. Receipt of the dedicated disconnect address (DSA) causes the LASP to disconnect in the same fashion as a nonmatching address. Reservation of this address for global use ensures that at least one address is available to disconnect all receiving LASPs. The DSA is especially useful when the secondary TAPs of multiple LASPs are to be left in different stable states. Receipt of the reset address (RSA) causes the LASP to assume the reset condition. Receipt of the test-synchronization address (TSA) causes the LASP to assume a connect status (MULTICAST) in which PTDO is at high impedance, but the configuration of the secondary TAPs are maintained to allow simultaneous operation of the secondary TAPs of multiple LASPs. This is useful for multicast TAP-state movement, simultaneous test operation, such as in Run-Test/Idle state, and scanning of common test data into multiple like scan chains. The MULTICAST status may also be useful for concurrent in-system programming (ISP) of common modules. The TSA is valid only when received in the Pause-DR or Pause-IR TAP states. Refer to Table 9 for different address mapping.

Alternatively, primary-to-secondary connection can be selected by asserting a low level at the bypass ($\overline{BYP_5}$) input. The remaining bypass ($\overline{BYP_4}$–$\overline{BYP_0}$) inputs are used for configuring the secondary TAPs as shown in Table 1 and Table 2. This operation is asynchronous to PTCK and is independent of PTRST and/or power-up reset. This bypassing feature is especially useful in the board-test environment because it allows board-level automated test equipment (ATE) to treat the LASP as a simple transceiver. When $\overline{BYP_5}$ is high, the LASP is free to respond to linking shadow protocols. Otherwise, when $\overline{BYP_5}$ is low, linking shadow protocols are ignored. Whether the connected status is achieved by use of linking shadow protocol or by use of bypass inputs, this status is indicated by a low level at the connect ($\overline{CON_2}$–$\overline{CON_0}$) outputs. Likewise, when the secondary TAP is disconnected from the primary TAP, the corresponding $\overline{CON}$ output is high. Each secondary TAP has a pass-through input and output consisting of SX_2–SX_0 and SY_2–SY_0, respectively. Similarly, the primary TAP also has a pass-through input and output consisting of PX and PY, respectively. Pass-through input PX drives the SY outputs of the secondary TAPs that are connected to the primary TAP. Disconnected secondary TAPs have their SY outputs at high impedance. Pass-through inputs SY_2–SY_0 of the connected secondary TAPs are logically ANDed and drive the PY output. Refer to Table 4-7 for pass-through input/output operation.

FUNCTIONAL BLOCK DIAGRAM



FUNCTION TABLE 1
(Primary-to-Secondary Connect Status)

INPUTS							LINKING SHADOW PROTOCOL RESULT	PRIMARY-TO-SECONDARY CONNECT STATUS	OUTPUTS		
$\overline{BYP_5}$	$\overline{BYP_4}$	$\overline{BYP_3}$	$\overline{BYP_2}$	$\overline{BYP_1}$	$\overline{BYP_0}$	$\overline{PTRST}$			$\overline{CON_2}$	$\overline{CON_1}$	$\overline{CON_0}$
L	X	X	H	H	H	L	–	BYP/TRST	H	H	H
L	X	X	H	H	L	L	–	BYP/TRST	H	H	L
L	X	X	H	L	H	L	–	BYP/TRST	H	L	H
L	X	X	H	L	L	L	–	BYP/TRST	H	L	L
L	X	X	L	H	H	L	–	BYP/TRST	L	H	H
L	X	X	L	H	L	L	–	BYP/TRST	L	H	L
L	X	X	L	L	H	L	–	BYP/TRST	L	L	H
L	X	X	L	L	L	L	–	BYP/TRST	L	L	L
L	X	X	H	H	H	H	–	BYP	H	H	H
L	X	X	H	H	L	H	–	BYP	H	H	L
L	X	X	H	L	H	H	–	BYP	H	L	H
L	X	X	H	L	L	H	–	BYP	H	L	L
L	X	X	L	H	H	H	–	BYP	L	H	H
L	X	X	L	H	L	H	–	BYP	L	H	L
L	X	X	L	L	H	H	–	BYP	L	L	H
L	X	X	L	L	L	H	–	BYP	L	L	L
H	X	X	X	X	X	L	–	TRST	H	H	H
H	X	X	X	X	X	H	RESET	RESET	H	H	H
H	X	X	X	X	X	H	MATCH	ON	See Function Table 3		
H	X	X	X	X	X	H	NO MATCH	OFF	H	H	H
H	X	X	X	X	X	H	HARD ERROR	OFF	H	H	H
H	X	X	X	X	X	H	DISCONNECT	OFF	H	H	H
H	X	X	X	X	X	H	TEST SYNCHRONIZATION	MULTICAST	See Note (1)		

(1) The result of receipt of the test synchronization address (TSA) on a secondary TAP, whose TAP state is Pause-DR or Pause-IR, is ON and the corresponding $\overline{CON}$ output is set low. The result of receipt of the TSA on a secondary TAP whose TAP state is Test-Logic-Reset or Run-Test-Idle is disconnect, and the corresponding $\overline{CON}$ output is set high.

FUNCTION TABLE 2
(Secondary TAP Configuration Using Bypass Inputs)

INPUTS		LINKING SHADOW PROTOCOL RESULT	OUTPUTS									
$\overline{BYP_{5-0}}$	$\overline{PTRST}$		$\overline{STRST}$ 2–0	STCK 2–0	$STMS_2$	$STMS_1$	$STMS_0$	$STDO_2$	$STDO_1$	$STDO_0$	PTDO	CTDO
L L L H H H	L		L	PTCK	H(1)	H(1)	H(1)	Z	Z	Z	Z	CTDI
L L L H H L	L		L	PTCK	H(1)	H(1)	H(1)	Z	Z	PTDI	$STDI_0$	$STDI_0$
L L L H L H	L		L	PTCK	H(1)	H(1)	H(1)	Z	PTDI	Z	$STDI_1$	$STDI_1$
L L L H L L	L		L	PTCK	H(1)	H(1)	H(1)	Z	$STDI_0$	PTDI	$STDI_1$	$STDI_1$
L L L L H H	L		L	PTCK	H(1)	H(1)	H(1)	PTDI	Z	Z	$STDI_2$	$STDI_2$
L L L L H L	L		L	PTCK	H(1)	H(1)	H(1)	$STDI_0$	Z	PTDI	$STDI_2$	$STDI_2$
L L L L L H	L		L	PTCK	H(1)	H(1)	H(1)	$STDI_1$	PTDI	Z	$STDI_2$	$STDI_2$
L L L L L L	L		L	PTCK	H(1)	H(1)	H(1)	$STDI_1$	$STDI_0$	PTDI	$STDI_2$	$STDI_2$
L L H H H H	L		L	PTCK	H(1)	H(1)	H(1)	Z	Z	Z	Z	CTDI
L L H H H L	L		L	PTCK	H(1)	H(1)	H(1)	Z	Z	PTDI	Z	$STDI_0$
L L H H L H	L		L	PTCK	H(1)	H(1)	H(1)	Z	PTDI	Z	Z	$STDI_1$
L L H H L L	L		L	PTCK	H(1)	H(1)	H(1)	Z	$STDI_0$	PTDI	Z	$STDI_1$
L L H L H H	L		L	PTCK	H(1)	H(1)	H(1)	PTDI	Z	Z	Z	$STDI_2$
L L H L H L	L		L	PTCK	H(1)	H(1)	H(1)	$STDI_0$	Z	PTDI	Z	$STDI_2$
L L H L L H	L		L	PTCK	H(1)	H(1)	H(1)	$STDI_1$	PTDI	Z	Z	$STDI_2$
L L H L L L	L		L	PTCK	H(1)	H(1)	H(1)	$STDI_1$	$STDI_0$	PTDI	Z	$STDI_2$
L H L H H H	L		L	PTCK	H(1)	H(1)	H(1)	Z	Z	Z	Z	CTDI
L H L H H L	L		L	PTCK	H(1)	H(1)	H(1)	Z	Z	CTDI	$STDI_0$	$STDI_0$
L H L H L H	L		L	PTCK	H(1)	H(1)	H(1)	Z	CTDI	Z	$STDI_1$	$STDI_1$
L H L H L L	L		L	PTCK	H(1)	H(1)	H(1)	Z	$STDI_0$	CTDI	$STDI_1$	$STDI_1$
L H L L H H	L		L	PTCK	H(1)	H(1)	H(1)	CTDI	Z	Z	$STDI_2$	$STDI_2$
L H L L H L	L		L	PTCK	H(1)	H(1)	H(1)	$STDI_0$	Z	CTDI	$STDI_2$	$STDI_2$
L H L L L H	L		L	PTCK	H(1)	H(1)	H(1)	$STDI_1$	CTDI	Z	$STDI_2$	$STDI_2$
L H L L L L	L		L	PTCK	H(1)	H(1)	H(1)	$STDI_1$	$STDI_0$	CTDI	$STDI_2$	$STDI_2$
L H H H H H	L		L	PTCK	H(1)	H(1)	H(1)	Z	Z	Z	Z	CTDI
L H H H H L	L		L	PTCK	H(1)	H(1)	H(1)	Z	Z	CTDI	Z	$STDI_0$
L H H H L H	L		L	PTCK	H(1)	H(1)	H(1)	Z	CTDI	Z	Z	$STDI_1$
L H H H L L	L		L	PTCK	H(1)	H(1)	H(1)	Z	$STDI_0$	CTDI	Z	$STDI_1$
L H H L H H	L		L	PTCK	H(1)	H(1)	H(1)	CTDI	Z	Z	Z	$STDI_2$
L H H L H L	L		L	PTCK	H(1)	H(1)	H(1)	$STDI_0$	Z	CTDI	Z	$STDI_2$
L H H L L H	L		L	PTCK	H(1)	H(1)	H(1)	$STDI_1$	CTDI	Z	Z	$STDI_2$
L H H L L L	L		L	PTCK	H(1)	H(1)	H(1)	$STDI_1$	$STDI_0$	CTDI	Z	$STDI_2$
L L L H H H	H		H	PTCK	$STMS_2$(2)	$STMS_1$(2)	$STMS_0$(2)	Z	Z	Z	Z	CTDI
L L L H H L	H		H	PTCK	$STMS_2$(2)	$STMS_1$(2)	PTMS	Z	Z	PTDI	$STDI_0$	$STDI_0$
L L L H L H	H		H	PTCK	$STMS_2$(2)	PTMS	$STMS_0$(2)	Z	PTDI	Z	$STDI_1$	$STDI_1$
L L L H L L	H		H	PTCK	$STMS_2$(2)	PTMS	PTMS	Z	$STDI_0$	PTDI	$STDI_1$	$STDI_1$

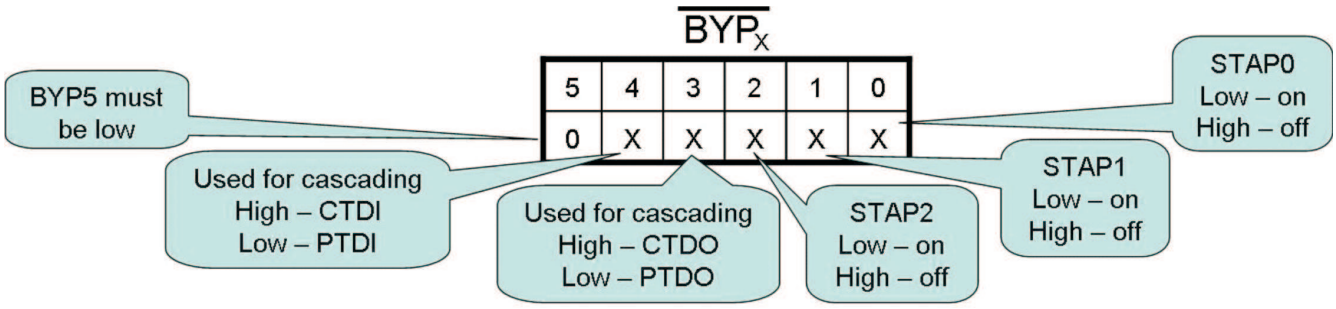
(1) In normal operation of IEEE Std 1149.1-compliant architectures, it is recommended that TMS be high prior to release of $\overline{STRST}$. The $\overline{BYP}$/$\overline{STRST}$ connect status ensures that this condition is met at STMS, regardless of the applied PTMS. Also, it is recommended that STMS be kept high for a minimum duration of five PTCK cycles following assertion of $\overline{PTRST}$, either by maintaining $\overline{PTRST}$ low or by setting PTMS high. This ensures that devices with and without $\overline{STRST}$ inputs are moved to their Test-Logic-Reset TAP states. It is expected that, in normal application, this condition occurs only when $\overline{BYP_5}$ is fixed at the low state. In such a case, upon release of $\overline{PTRST}$, the LASP immediately resumes the BYP connect status.

(2) STMS level before steady-state conditions were established

FUNCTION TABLE 2
(Secondary TAP Configuration Using Bypass Inputs)(Continued)

INPUTS		LINKING SHADOW PROTOCOL RESULT	OUTPUTS									
$\overline{BYP_{5-0}}$	$\overline{PTRST}$		$\overline{STRST}$ 20	STCK 2–0	$STMS_2$	$STMS_1$	$STMS_0$	$STDO_2$	$STDO_1$	$STDO_0$	PTDO	CTDO
L L L L H H	H		H(1)	PTCK	PTMS	$STMS_1$(2)	$STMS_0$(2)	PTDI	Z	Z	$STDI_2$	$STDI_2$
L L L L H L	H		H	PTCK	PTMS	$STMS_1$(2)	PTMS	$STDI_0$	Z	PTDI	$STDI_2$	$STDI_2$
L L L L L H	H		H	PTCK	PTMS	PTMS	$STMS_0$(2)	$STDI_1$	PTDI	Z	$STDI_2$	$STDI_2$
L L L L L L	H		H	PTCK	PTMS	PTMS	PTMS	$STDI_1$	$STDI_0$	PTDI	$STDI_2$	$STDI_2$
L L H H H H	H		H	PTCK	$STMS_2$(3)	$STMS_1$(3)	$STMS_0$(3)	Z	Z	Z	Z	CTDI
L L H H H L	H		H	PTCK	$STMS_2$(3)	$STMS_1$(3)	PTMS	Z	Z	PTDI	Z	$STDI_0$
L L H H L H	H		H	PTCK	$STMS_2$(3)	PTMS	$STMS_0$(3)	Z	PTDI	Z	Z	$STDI_1$
L L H H L L	H		H	PTCK	$STMS_2$(3)	PTMS	PTMS	Z	$STDI_0$	PTDI	Z	$STDI_1$
L L H L H H	H		H	PTCK	PTMS	$STMS_1$(3)	$STMS_0$(3)	PTDI	Z	Z	Z	$STDI_2$
L L H L H L	H		H	PTCK	PTMS	$STMS_1$(3)	PTMS	$STDI_0$	Z	PTDI	Z	$STDI_2$
L L H L L H	H		H	PTCK	PTMS	PTMS	$STMS_0$(3)	$STDI_1$	PTDI	Z	Z	$STDI_2$
L L H L L L	H		H	PTCK	PTMS	PTMS	PTMS	$STDI_1$	$STDI_0$	PTDI	Z	$STDI_2$
L H L H H H	H		H	PTCK	$STMS_2$(3)	$STMS_1$(3)	$STMS_0$(3)	Z	Z	Z	Z	CTDI
L H L H H L	H		H	PTCK	$STMS_2$(3)	$STMS_1$(3)	PTMS	Z	Z	CTDI	$STDI_0$	$STDI_0$
L H L H L H	H		H	PTCK	$STMS_2$(3)	PTMS	$STMS_0$(3)	Z	CTDI	Z	$STDI_1$	$STDI_1$
L H L H L L	H		H	PTCK	$STMS_2$(3)	PTMS	PTMS	Z	$STDI_0$	CTDI	$STDI_1$	$STDI_1$
L H L L H H	H		H	PTCK	PTMS	$STMS_1$(3)	$STMS_0$(3)	CTDI	Z	Z	$STDI_2$	$STDI_2$
L H L L H L	H		H	PTCK	PTMS	$STMS_1$(3)	PTMS	$STDI_0$	Z	CTDI	$STDI_2$	$STDI_2$
L H L L L H	H		H	PTCK	PTMS	PTMS	$STMS_0$(3)	$STDI_1$	CTDI	Z	$STDI_2$	$STDI_2$
L H L L L L	H		H	PTCK	PTMS	PTMS	PTMS	$STDI_1$	$STDI_0$	CTDI	$STDI_2$	$STDI_2$
L H H H H H	H		H	PTCK	$STMS_2$(3)	$STMS_1$(3)	$STMS_0$(3)	Z	Z	Z	Z	CTDI
L H H H H L	H		H	PTCK	$STMS_2$(3)	$STMS_1$(3)	PTMS	Z	Z	CTDI	Z	$STDI_0$
L H H H L H	H		H	PTCK	$STMS_2$(3)	PTMS	$STMS_0$(3)	Z	CTDI	Z	Z	$STDI_1$
L H H H L L	H		H	PTCK	$STMS_2$(3)	PTMS	PTMS	Z	$STDI_0$	CTDI	Z	$STDI_1$
L H H L H H	H		H	PTCK	PTMS	$STMS_1$(3)	$STMS_0$(3)	CTDI	Z	Z	Z	$STDI_2$
L H H L H L	H		H	PTCK	PTMS	$STMS_1$(3)	PTMS	$STDI_0$	Z	CTDI	Z	$STDI_2$
L H H L L H	H		H	PTCK	PTMS	PTMS	$STMS_0$(3)	$STDI_1$	CTDI	Z	Z	$STDI_2$
L H H L L L	H		H	PTCK	PTMS	PTMS	PTMS	$STDI_1$	$STDI_0$	CTDI	Z	$STDI_2$
H X X X X X	L		L	PTCK	H	H	H	Z	Z	Z	Z	H
H X X X X X	H	RESET	H	PTCK	H	H	H	Z	Z	Z	Z	CTDI
H X X X X X	H	MATCH	H	PTCK	See Function Table 3							
H X X X X X	H	NO MATCH	H	PTCK	$STMS_2$(3)	$STMS_1$(3)	$STMS_0$(3)	Z	Z	Z	Z	CTDI
H X X X X X	H	HARD ERROR(4)	H	PTCK	$STMS_2$(3)	$STMS_1$(3)	$STMS_0$(3)	Z	Z	Z	Z	CTDI
H X X X X X	H	DISCONNECT	H	PTCK	$STMS_2$(3)	$STMS_1$(3)	$STMS_0$(3)	Z	Z	Z	Z	CTDI
H X X X X X	H	TEST SYNCHRONIZATION	H	PTCK	PTMS(5)	PTMS(5)	PTMS(5)	PTDI(5)	PTDI(5)	PTDI(5)	Z	CTDI

(1) In normal operation of IEEE Std 1149.1-compliant architectures, it is recommended that TMS be high prior to release of TRST. The BYP/TRST connect status ensures that this condition is met at STMS, regardless of the applied PTMS. Also, it is recommended that STMS be kept high for a minimum duration of five PTCK cycles following assertion of PTRST, either by maintaining PTRST low or by setting PTMS high. This ensures that devices with and without TRST inputs are moved to their Test-Logic-Reset TAP states. It is expected that, in normal application, this condition occurs only when BYP5 is fixed at the low state. In such a case, upon release of PTRST, the LASP immediately resumes the BYP connect status.
(2) STMS level before steady-state conditions were established
(3) STMS level before steady-state conditions were established
(4) The linking shadow protocol is well defined. Some variations in the protocol are tolerated (see protocol errors). Those that are not tolerated produce the result HARD ERROR and cause disconnect, as indicated.
(5) PTDI and PTMS are connected to STDO and STMS, respectively, only on those secondary TAPs whose TAP state is Pause-DR or Pause-IR while PTDO is high impedance. The result of linking shadow protocol on a secondary TAP whose state is Test-Logic-Reset or Run-Test-Idle is DISCONNECT.


$\overline{BYP_X}$
5
4
3
2
1
0
0
X
X
X
X
X
BYP5 must be low
Used for cascading High – CTDI Low – PTDI
Used for cascading High – CTDO Low – PTDO
STAP2 Low – on High – off
STAP1 Low – on High – off
STAP0 Low – on High – off

FUNCTION TABLE 3
(Secondary TAP Configuration Using Linking Shadow Protocol)

POSITION	CONFIG BITS 2–0	$\overline{STRST}$ 2–0	STCK 2–0	$STMS_2$	$STMS_1$	$STMS_0$	$STDO_2$	$STDO_1$	$STDO_0$	PTDO	CTDO	$\overline{CON_2}$	$\overline{CON_1}$	$\overline{CON_0}$
Single device	H H H	H	PTCK	$STMS_2$(1)	$STMS_1$(1)	$STMS_0$(1)	Z	Z	Z	Z	CTDI	H	H	H
	H H L	H	PTCK	$STMS_2$(1)	$STMS_1$(1)	PTMS	Z	Z	PTDI	$STDI_0$	$STDI_0$	H	H	L
	H L H	H	PTCK	$STMS_2$(1)	PTMS	$STMS_0$(1)	Z	PTDI	Z	$STDI_1$	$STDI_1$	H	L	H
	H L L	H	PTCK	$STMS_2$(1)	PTMS	PTMS	Z	$STDI_0$	PTDI	$STDI_1$	$STDI_1$	H	L	L
	L H H	H	PTCK	PTMS	$STMS_1$(1)	$STMS_0$(1)	PTDI	Z	Z	$STDI_2$	$STDI_2$	L	H	H
	L H L	H	PTCK	PTMS	$STMS_1$(1)	PTMS	$STDI_0$	Z	PTDI	$STDI_2$	$STDI_2$	L	H	L
	L L H	H	PTCK	PTMS	PTMS	$STMS_0$(1)	$STDI_1$	PTDI	Z	$STDI_2$	$STDI_2$	L	L	H
	L L L	H	PTCK	PTMS	PTMS	PTMS	$STDI_1$	$STDI_0$	PTDI	$STDI_2$	$STDI_2$	L	L	L
First device in cascade chain	H H H	H	PTCK	$STMS_2$(1)	$STMS_1$(1)	$STMS_0$(1)	Z	Z	Z	Z	CTDI	H	H	H
	H H L	H	PTCK	$STMS_2$(1)	$STMS_1$(1)	PTMS	Z	Z	PTDI	Z	$STDI_0$	H	H	L
	H L H	H	PTCK	$STMS_2$(1)	PTMS	$STMS_0$(1)	Z	PTDI	Z	Z	$STDI_1$	H	L	H
	H L L	H	PTCK	$STMS_2$(1)	PTMS	PTMS	Z	$STDI_0$	PTDI	Z	$STDI_1$	H	L	L
	L H H	H	PTCK	PTMS	$STMS_1$(1)	$STMS_0$(1)	PTDI	Z	Z	Z	$STDI_2$	L	H	H
	L H L	H	PTCK	PTMS	$STMS_1$(1)	PTMS	$STDI_0$	Z	PTDI	Z	$STDI_2$	L	H	L
	L L H	H	PTCK	PTMS	PTMS	$STMS_0$(1)	$STDI_1$	PTDI	Z	Z	$STDI_2$	L	L	H
	L L L	H	PTCK	PTMS	PTMS	PTMS	$STDI_1$	$STDI_0$	PTDI	Z	$STDI_2$	L	L	L
Nor first and not last device in cascade chain	H H H	H	PTCK	$STMS_2$(1)	$STMS_1$(1)	$STMS_0$(1)	Z	Z	Z	Z	CTDI	H	H	H
	H H L	H	PTCK	$STMS_2$(1)	$STMS_1$(1)	PTMS	Z	Z	CTDI	Z	$STDI_0$	H	H	L
	H L H	H	PTCK	$STMS_2$(1)	PTMS	$STMS_0$(1)	Z	CTDI	Z	Z	$STDI_1$	H	L	H
	H L L	H	PTCK	$STMS_2$(1)	PTMS	PTMS	Z	$STDI_0$	CTDI	Z	$STDI_1$	H	L	L
	L H H	H	PTCK	PTMS	$STMS_1$(1)	$STMS_0$(1)	CTDI	Z	Z	Z	$STDI_2$	L	H	H
	L H L	H	PTCK	PTMS	$STMS_1$(1)	PTMS	$STDI_0$	Z	PTDI	Z	$STDI_2$	L	H	L
	L L H	H	PTCK	PTMS	PTMS	$STMS_0$(1)	$STDI_1$	CTDI	Z	Z	$STDI_2$	L	L	H
	L L L	H	PTCK	PTMS	PTMS	PTMS	$STDI_1$	$STDI_0$	PTDI	Z	$STDI_2$	L	L	L
Last device in cascade chain	H H H	H	PTCK	$STMS_2$(1)	$STMS_1$(1)	$STMS_0$(1)	Z	Z	Z	Z	CTDI	H	H	H
	H H L	H	PTCK	$STMS_2$(1)	$STMS_1$(1)	PTMS	Z	Z	CTDI	$STDI_0$	$STDI_0$	H	H	L
	H L H	H	PTCK	$STMS_2$(1)	PTMS	$STMS_0$(1)	Z	CTDI	Z	$STDI_1$	$STDI_1$	H	L	H
	H L L	H	PTCK	$STMS_2$(1)	PTMS	PTMS	Z	$STDI_0$	CTDI	$STDI_1$	$STDI_1$	H	L	L
	L H H	H	PTCK	PTMS	$STMS_1$(1)	$STMS_0$(1)	CTDI	Z	Z	$STDI_2$	$STDI_2$	L	H	H
	L H L	H	PTCK	PTMS	$STMS_1$(1)	PTMS	$STDI_0$	Z	PTDI	$STDI_2$	$STDI_2$	L	H	L
	L L H	H	PTCK	PTMS	PTMS	$STMS_0$(1)	$STDI_1$	CTDI	Z	$STDI_2$	$STDI_2$	L	L	H
	L L L	H	PTCK	PTMS	PTMS	PTMS	$STDI_1$	$STDI_0$	PTDI	$STDI_2$	$STDI_2$	L	L	L

(1) STMS level before steady-state conditions were established

In order to provide the ability to cascade multiple LASPs, pad bits are used to reduce propagation delays that reduce the allowable test clock speed. These pad bits are located along the internal scan path of the LASP and, therefore, must be accommodated in the boundary-scan test program. The number of these bits ranges from one to four. The number and location completely depends on the configuration of the LASP. In Function Table 4, each LASP relative position and configuration scan path uses a (1) to indicate a pad bit in the path.

FUNCTION TABLE 4
(Pad Bits)

CASCADE POSITION	STAP0	STAP1	STAP2	SCAN-PATH CONFIGURATION	NO. OF PAD BITS
Single Device	Inactive	Inactive	Inactive	None	0
Single Device	Active	Inactive	Inactive	PTDI-(1)-STAP0-(1)-PTDO	2
Single Device	Inactive	Active	Inactive	PTDI-(1)-STAP1-(1)-PTDO	2
Single Device	Active	Active	Inactive	PTDI-(1)-STAP0-(1)-STAP1-(1)-PTDO	3
Single Device	Inactive	Inactive	Active	PTDI-(1)-STAP2-(1)-PTDO	2
Single Device	Active	Inactive	Active	PTDI-(1)-STAP0-(1)-STAP2-(1)-PTDO	3
Single Device	Inactive	Active	Active	PTDI-(1)-STAP1-(1)-STAP2-(1)-PTDO	3
Single Device	Active	Active	Active	PTDI-(1)-STAP0-(1)-STAP1-(1)-STAP2-(1)-PTDO	4
First Device	Inactive	Inactive	Inactive	None	0
First Device	Active	Inactive	Inactive	PTDI-(1)-STAP0-(1)-CTDO	2
First Device	Inactive	Active	Inactive	PTDI-(1)-STAP1-(1)-CTDO	2
First Device	Active	Active	Inactive	PTDI-(1)-STAP0-(1)-STAP1-(1)-CTDO	3
First Device	Inactive	Inactive	Active	PTDI-(1)-STAP2-(1)-CTDO	2
First Device	Active	Inactive	Active	PTDI-(1)-STAP0-(1)-STAP2-(1)-CTDO	3
First Device	Inactive	Active	Active	PTDI-(1)-STAP1-(1)-STAP2-(1)-CTDO	3
First Device	Active	Active	Active	PTDI-(1)-STAP0-(1)-STAP1-(1)-STAP2-(1)-CTDO	4
Last Device	Inactive	Inactive	Inactive	None	0
Last Device	Active	Inactive	Inactive	CTDI-(1)-STAP0-(1)-PTDO	2
Last Device	Inactive	Active	Inactive	CTDI-(1)-STAP1-(1)-PTDO	2
Last Device	Active	Active	Inactive	CTDI-(1)-STAP0-(1)-STAP1-(1)-PTDO	3
Last Device	Inactive	Inactive	Active	CTDI-(1)-STAP2-(1)-PTDO	2
Last Device	Active	Inactive	Active	CTDI-(1)-STAP0-(1)-STAP2-(1)-PTDO	3
Last Device	Inactive	Active	Active	CTDI-(1)-STAP1-(1)-STAP2-(1)-PTDO	3
Last Device	Active	Active	Active	CTDI-(1)-STAP0-(1)-STAP1-(1)-STAP2-(1)-PTDO	4
Middle Device	Inactive	Inactive	Inactive	CTDI-(1)-CTDO	1
Middle Device	Active	Inactive	Inactive	CTDI-(1)-STAP0-(1)-CTDO	2
Middle Device	Inactive	Active	Inactive	CTDI-(1)-STAP1-(1)-CTDO	2
Middle Device	Active	Active	Inactive	CTDI-(1)-STAP0-(1)-STAP1-(1)-CTDO	3
Middle Device	Inactive	Inactive	Active	CTDI-(1)-STAP2-(1)-CTDO	2
Middle Device	Active	Inactive	Active	CTDI-(1)-STAP0-(1)-STAP2-(1)-CTDO	3
Middle Device	Inactive	Active	Active	CTDI-(1)-STAP1-(1)-STAP2-(1)-CTDO	3
Middle Device	Active	Active	Active	CTDI-(1)-STAP0-(1)-STAP1-(1)-STAP2-(1)-CTDO	4

FUNCTION TABLE 5
(SY_x Output Configuration Using Bypass Inputs)

$\overline{BYP_5}$–$\overline{BYP_0}$	SY_2	SY_1	SY_0
L X X H H H	Z	Z	Z
L X X H H L	Z	Z	PX
L X X H L H	Z	PX	Z
L X X H L L	Z	PX	PX
L X X L H H	PX	Z	Z
L X X L H L	PX	Z	PX
L X X L L H	PX	PX	Z
L X X L L L	PX	PX	PX
H X X X X X	As requested by linking shadow protocol (see Function Table 6)		

FUNCTION TABLE 6
(SY_x Output Configuration Using Linking Shadow Protocol)

$\overline{CON_2}$–$\overline{CON_0}$	SY_2	SY_1	SY_0
H H H	Z	Z	Z
H H L	Z	Z	PX
H L H	Z	PX	Z
H L L	Z	PX	PX
L H H	PX	Z	Z
L H L	PX	Z	PX
L L H	PX	PX	Z
L L L	PX	PX	PX

FUNCTION TABLE 7
(PY Output Configuration Using Bypass Inputs)

$\overline{BYP_5}$–$\overline{BYP_0}$	PY
L X X H H H	Z
L X X H H L	SX_0
L X X H L H	SX_1
L X X H L L	SX_1 and SX_0
L X X L H H	SX_2
L X X L H L	SX_2 and SX_0
L X X L L H	SX_2 and SX_1
L X X L L L	SX_2 and SX_1 and SX_0
H X X X X X	As requested by linking shadow protocol (see Function Table 6)

FUNCTION TABLE 8
(PY Output Configuration Using Linking Shadow Protocol)

$\overline{CON}_2$–$\overline{CON}_0$	PY
H H H	Z
H H L	SX_0
H L H	SX_1
H L L	SX_1 and SX_0
L H H	SX_2
L H L	SX_2 and SX_0
L L H	SX_2 and SX_1
L L L	SX_2 and SX_1 and SX_0

TERMINAL FUNCTIONS

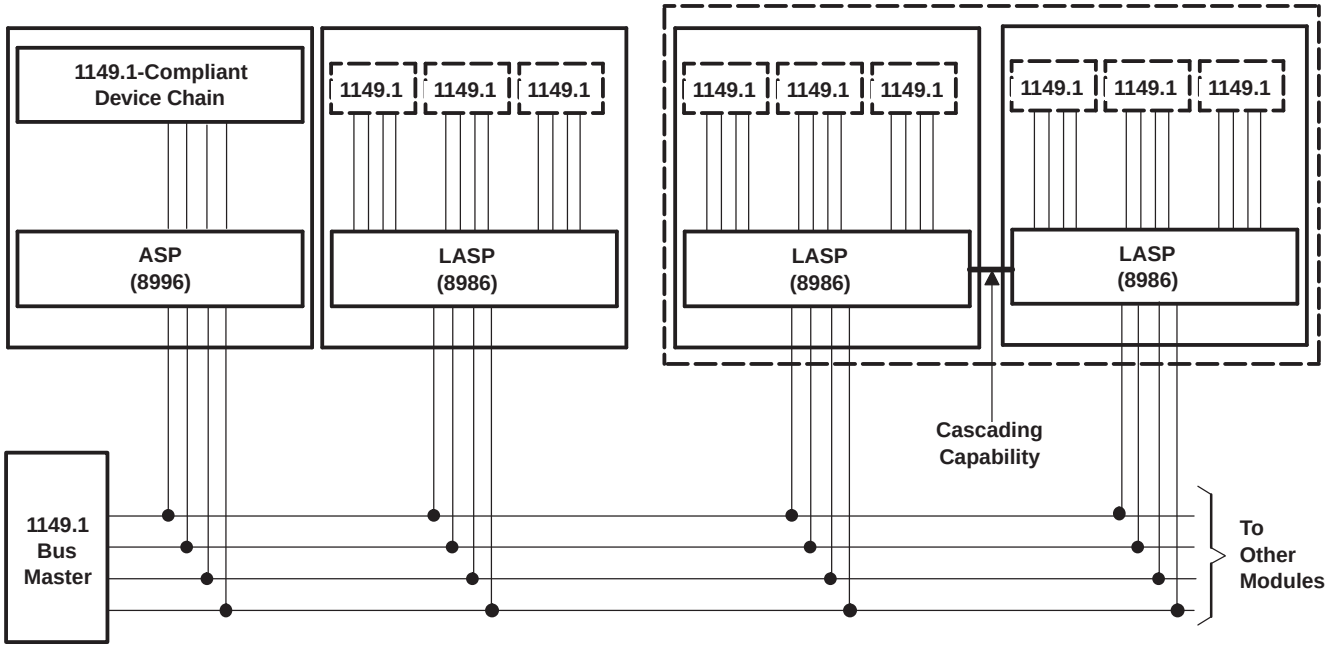
TERMINAL NAME	DESCRIPTION
A_9–A_0	Address (inputs). The LASP compares addresses received via linking shadow protocol against the value at A_9–A_0 to determine address match. The bit order is from most significant to least significant. An internal pullup at each A_9–A_0 terminal forces the terminal to a high level if it has no external connection.
P_2–P_0	Position (inputs). The LASP compares position received via linking shadow protocol against the value at P_2–P_0 to determine position match. The bit order is from most significant to least significant. An internal pullup at each P_2–P_0 terminal forces the terminal to a high level if it has no external connection.
$\overline{BYP}_5$–$\overline{BYP}_0$	Bypass (inputs). A low input at $\overline{BYP}_5$ forces the LASP into BYP or BYP/TRST status, depending on $\overline{PTRST}$ being high or low, respectively. While $\overline{BYP}_5$ is low, linking shadow protocols are ignored and the remaining bypass $\overline{BYP}_4$–$\overline{BYP}_0$ inputs are used for configuring the secondary scan ports as shown in Tables 1 and 2. Otherwise, while $\overline{BYP}_5$ is high, the LASP is free to respond to linking shadow protocols. An internal pullup forces $\overline{BYP}_5$–$\overline{BYP}_0$ to a high level if it has no external connection.
$\overline{CON}_2$–$\overline{CON}_0$	Connect indicators (outputs). The LASP indicates secondary-scan-port activity (resulting from BYP, BYP/TRST, MULTICAST, or ON status) by forcing the corresponding $\overline{CON}$ bit to be low. Inactivity (resulting from OFF, RESET, or TRST status) is indicated when the corresponding $\overline{CON}$ bit is high. This output is synchronous to the falling edge of PTCK.
PTCK	Primary test clock. PTCK receives the TCK signal required by IEEE Std 1149.1. The LASP always buffers PTCK to $STCK_2$–$STCK_0$. Linking shadow protocols are received/acknowledged synchronously to PTCK and connect-status changes invoked by the linking shadow protocol are made synchronously to PTCK.
PTDI	Primary test data input. PTDI receives the TDI signal required by IEEE Std 1149.1. During appropriate TAP states, the LASP monitors PTDI for linking shadow protocols. During linking shadow protocols, data at PTDI is captured on the rising edge of PTCK. When a valid linking shadow protocol is received in this fashion, the LASP compares the received address and position against the A_9–A_0 and P_2–P_0 inputs, respectively. If the LASP detects a match, it outputs an acknowledgment, then connects its primary TAP terminals to its secondary TAP terminals. Under BYP, BYP/TRST, MULTICAST, or ON status, the LASP buffers the PTDI signal to $STDO_2$–$STDO_0$, depending on the state of $\overline{BYP}_4$–$\overline{BYP}_0$ pins or the configuration requested during linking shadow protocol. An internal pullup forces PTDI to a high level if it has no external connection.
PTDO	Primary test data output. PTDO transmits the TDO signal required by IEEE Std 1149.1. During linking shadow protocols, the LASP transmits any required acknowledgment via the PTDO. Under BYP, BYP/TRST, or ON status, the LASP buffers the PTDO signal from PTDI or $STDI_2$–$STDI_0$, depending on the state of $\overline{BYP}_4$–$\overline{BYP}_0$ pins or the configuration requested during linking shadow protocol. Under OFF, MULTICAST, RESET, or TRST status, PTDO is at high impedance. This output is synchronous to the falling edge of PTCK.

TERMINAL FUNCTIONS (CONTINUED)

TERMINAL NAME	DESCRIPTION
PTMS	Primary test mode select. PTMS receives the TMS signal required by IEEE Std 1149.1. The LASP monitors PTMS to determine the TAP-controller state. During stable TAP states, other than Shift-DR or Shift-IR (i.e., Test-Logic-Reset, Run-Test-Idle, Pause-DR, Pause-IR), the LASP can respond to linking shadow protocols. Under BYP, MULTICAST, or ON status, the LASP buffers the PTMS signal to $STMS_2$–$STMS_0$, depending on the state of $\overline{BYP_4}$–$\overline{BYP_0}$ pins or the configuration requested during linking shadow protocol. An internal pullup forces PTMS to a high level if it has no external connection.
$\overline{PTRST}$	Primary test reset. $\overline{PTRST}$ receives the $\overline{TRST}$ signal allowed by IEEE Std 1149.1. The LASP always buffers $\overline{PTRST}$ to $\overline{STRST_2}$–$\overline{STRST_0}$. A low input at $\overline{PTRST}$ forces the LASP to assume TRST or BYP/TRST status, depending on $\overline{BYP_5}$ being high or low, respectively. Such operation also asynchronously resets the internal LASP state to its power-up condition. Otherwise, while $\overline{PTRST}$ is high, the LASP is free to respond to linking shadow protocols. An internal pullup forces $\overline{PTRST}$ to a high level if it has no external connection.
$STCK_2$–$STCK_0$	Secondary test clocks. $STCK_2$–$STCK_0$ retransmit the TCK signal required by IEEE Std 1149.1. The LASP always buffers $STCK_2$–$STCK_0$ from PTCK.
$STDI_2$–$STDI_0$	Secondary test data inputs. $STDI_2$–$STDI_0$ receive the TDI signal required by IEEE Std 1149.1. Under BYP, BYP/TRST, or ON status, the LASP buffers $STDI_2$–$STDI_0$ to $STDO_2$–$STDO_0$ or PTDO, depending on the state of $\overline{BYP_4}$–$\overline{BYP_0}$ pins or the configuration requested during linking shadow protocol. An internal pullup forces $STDI_2$–$STDI_0$ to a high level if it has no external connection.
$STDO_2$–$STDO_0$	Secondary test data outputs. $STDO_2$–$STDO_0$ transmit the TDO signal required by IEEE Std 1149.1. Under BYP, BYP/TRST, MULTICAST, or ON status, the LASP buffers $STDO_2$–$STDO_0$ from $STDI_2$–$STDI_0$, PTDI, or CTDI, depending on the state of $\overline{BYP_4}$–$\overline{BYP_0}$ pins or the configuration requested during linking shadow protocol. Under OFF, RESET, or TRST status, $STDO_2$–$STDO_0$ is at high impedance. These outputs are synchronous to the falling edge of PTCK.
$STMS_2$–$STMS_0$	Secondary test mode selects. $STMS_2$–$STMS_0$ retransmit the TMS signal required by IEEE Std 1149.1. Under BYP, MULTICAST, or ON status, the LASP buffers $STMS_2$–$STMS_0$ from PTMS, depending on the state of BYP_4–BYP_0 pins or the configuration requested during linking shadow protocol. When disconnected (as a result of OFF status), $STMS_2$–$STMS_0$ maintain their last valid state until the LASP assumes BYP/TRST, RESET, or TRST status (upon which it is forced high) or the LASP again assumes BYP, MULTICAST, or ON status.
$\overline{STRST_2}$–$\overline{STRST_0}$	Secondary test resets. $\overline{STRST_2}$–$\overline{STRST_0}$ retransmit the TRST signal allowed by IEEE Std 1149.1. The LASP always buffers $\overline{STRST_2}$–$\overline{STRST_0}$ from $\overline{PTRST}$.
CTDI	Cascade test data input. CTDI facilitates cascading multiple LASPs. CTDI is connected to CTDO of the preceding LASP in the cascade chain. When the LASP is the first device in the cascade chain or is not cascaded to any other LASPs, CTDI has no external connection and an internal pullup forces CTDI to a high level.
CTDO	Cascade test data output. CTDO facilitates cascading multiple LASPs. CTDO is connected to CTDI of the succeeding LASP in the cascade chain. The LASP buffers CTDO from $STDI_2$–$STDI_0$ or CTDI, depending on the state of $\overline{BYP_4}$–$\overline{BYP_0}$ pins or the configuration requested during linking shadow protocol. This output is synchronous to the falling edge of PTCK.
SX_2–SX_0	Secondary pass through (inputs). General-purpose inputs that can be driven to the PY output of the primary TAP. An internal pullup forces SX_2–SX_0 to a high level if it has no external connection.
SY_2–SY_0	Secondary pass through (outputs). Primary pass-through input PX drives the general-purpose SY outputs of the secondary TAPs that are connected to the primary TAP. Disconnected secondary TAPs have their SY outputs at high impedance.
PX	Primary pass through (input). A general-purpose input driven to SY outputs of the secondary TAPs that are connected to the primary TAP. An internal pullup forces PX to a high level if it has no external connection.
PY	Primary pass through (output). A general-purpose output that can be driven from SX_2–SX_0.
$\overline{OE}$	Output enable (input). When high, this active-low control signal puts the secondary TAPs of the LASP at high impedance to enable an alternative resource to access one or more of the three scan chains.
GND	Ground
V_{CC}	Supply voltage

APPLICATION INFORMATION

In application, the LASP is used at each of several serially-chained groups of IEEE Std 1149.1-compliant devices. The LASP for each such group is assigned an address (via inputs A_9–A_0) that is unique from that assigned to LASPs for the remaining groups. Additionally, within each group, each LASP is assigned a position (via inputs P_2–P_0) that is unique from that assigned to LASPs in the same groups. This allows individually configuring the secondary scan ports of each LASP within a group with a single linking shadow protocol when cascaded. Each LASP is wired at its primary TAP to common (multidrop) TAP signals (sourced from a central IEEE Std 1149.1 bus master) and fans out its secondary TAP signals to a specific linked group of IEEE Std 1149.1-compliant devices with which it is associated. Additionally, LASPs can be cascaded together to link additional secondary scan ports to one primary scan port. LASPs also can coexist with existing boards implementing the TI ASP (8996). The ASP has one primary to one secondary port, but a LASP has three secondary ports per device; Figure 1 shows an example.



NOTE A: 1149.1 means IEEE Std 1149.1.

Figure 1. LASP/ASP Application

This application allows the LASP to be wired to a four- or five-wire multidrop test access bus, such as might be found on a backplane. Each LASP would then be on a module, for example, a printed circuit board (PCB) that contains a serial chain of IEEE Std 1149.1-compliant devices and that would plug into the module-to-module bus (e.g., backplane). In the complete system, the LASP linking shadow protocols would allow the selection of the scan chain on a single module. The selected scan chain could then be controlled, via the multidrop TAP, as if it were the only scan chain in the system. Normal IR and DR scans could then be performed to accomplish the module test objectives. If ASPs are to be addressed, they would be selected by the standard shadow protocol.

Once scan operations to a given module are complete, another module can be selected in the same fashion, at which time the LASP-based connection to the first module is dissolved. This procedure can be continued progressively for each module to be tested. Finally, one of two global addresses can be issued to either leave all modules unselected [disconnect address (DSA)] or to deselect and reset scan chains for all modules [reset address (RSA)].

Additionally, in Pause-DR and Pause-IR TAP states, a third global address [test-synchronization address (TSA)] can be invoked to allow simultaneous TAP-state changes and multicast scan-in operations to selected modules. In this case, PTDO is at high impedance. This is especially useful in the former case, for allowing selected modules to be moved simultaneously to the Run-Test-Idle TAP state for module-level or module-to-module built-in self-test (BIST) functions, which operate synchronously to TCK in that TAP state and, in the latter case, for scanning common test setup/data into multiple like modules. In conjunction with the use of the pass-through input/output pairs (PX to SX_2–SX_0 and PY to SY_2–SY_0), the multicast mode can be effective for ISP of like modules.

Limitations

IEEE 1149.1 bus masters, which control the test clock (TCK), can use either a gated or free-running clock. The former, gated mode, halts the clock when pause is needed and the later, free running mode, places the applicable scan chains into a stable state while the clock continues to run. If a pause is needed while scanning data in or out, as in the Shift-DR and Shift-IR states, then the scan chains are put into Pause-DR and Pause-IR, respectively. While the LASP can successfully accept linking shadow protocols in the Pause-DR and Pause-IR states, JTAG tests cannot be successfully performed through a LASP if, while shifting data in or out, scan chains are placed in these states while using a free-running test clock.

As long as the clock continues to cycle the data in, the pad bits will continue to be updated. If the connected scan chain is in one of the pause states, the chain's boundary cells will not shift, but test values will be overwritten in the pad bits. While it may not be possible to use the LASP compatibly with a free-running test clock, by using a gated clock, these difficulties can be avoided.

ADDRESSING THE LASP

Addressing of an LASP in a system is accomplished by linking shadow protocols, which are received at PTDI synchronously to PTCK. These protocols can occur only in the following stable TAP states: Test-Logic-Reset, Run-Test/Idle, Pause-DR, and Pause-IR. Linking shadow protocols never occur in Shift-DR or Shift-IR states to prevent contention on the signal bus to which PTDO is wired. Additionally, the LASP PTMS must be held at a constant low or high level throughout a linking shadow protocol. If TAP-state changes occur in the midst of a protocol, the protocol is aborted and the select-protocol state machine returns to its initial state.

These protocols are based on a serial bit-pair signaling scheme used by the ASP (8996), in which two bit-pair combinations (data one, data zero) are used to represent data and the other two bit-pair combinations (select, idle) are used for framing — that is, to indicate where data begins and ends. This allows the LASP to coexist and be fully compatible with the ASP.

These bit pairs are received serially at PTDI (or transmitted serially at PTDO) synchronously to PTCK as follows and as shown in Figure 2:

1. The idle bit pair (I) is represented as two consecutive high signals.
2. The select bit pair (S) is represented as two consecutive low signals.
3. The data-one bit pair (D) is represented as a low signal, followed by a high signal.
4. The data-zero bit pair (D) is represented as a high signal, followed by a low signal.

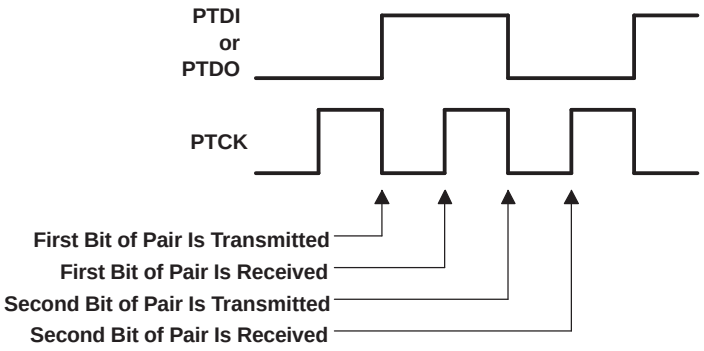


Figure 2. Bit-Pair Timing (Data Zero Shown)

Linking Shadow Protocol

A complete linking shadow protocol is composed of the receipt of a select protocol, followed, if applicable, by the transmission of an acknowledge protocol. Both select and acknowledge protocols are composed of two fields (address and command) comprising a message. Select bit pairs frame each field at the beginning and end, and idle bit pairs frame the message at the beginning and end. The address is composed of 10 data bit pairs and selects the LASP by matching it against address inputs A_9–A_0. The command consists of two subfields, position and configuration. Position identifies the physical position of the LASP in the cascaded chain and selects the LASP within the cascaded group by matching it against position inputs P_2–P_0. When the LASP is stand alone, its inputs P_2–P_0 are tied low. The configuration portion of the protocol is used for configuring the primary-to-secondary TAPs connections of the LASP whose address and position matches. Figure 3 shows a complete linking shadow protocol. (The symbol T is used to represent a high-impedance condition on the associated signal line. Because the high-impedance state at PTDI is logically high due to pullup, it maps onto the idle bit pair).

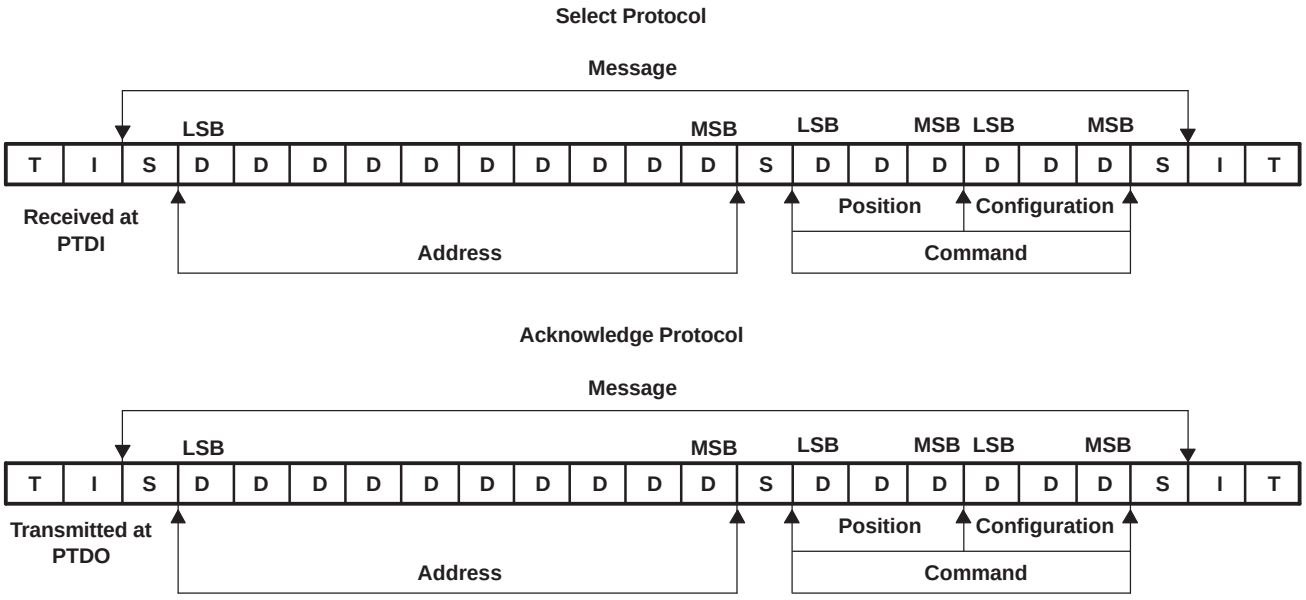


Figure 3. Complete Linking Shadow Protocol

Select Protocol

The select protocol is the LASP's means of receiving (at PTDI) address, position, and secondary TAP configuration information from an IEEE Std 1149.1 bus master. A 10-bit address value, 3-bit position value, and 3-bit configuration are decoded from the received data-one and/or data-zero bit pairs. These bit pairs are interpreted in least-significant-bit-first order.

Acknowledge Protocol

Following the receipt of a complete select-protocol sequence, the protocol result provisionally is set to NO MATCH and the connect status set to OFF. The received address and position then are compared to that at the LASP address (A_9–A_0) inputs and position (P_2–P_0) inputs, respectively. If these values match, the LASP immediately (with no delay) responds with an acknowledge protocol transmitted from PTDO. A 10-bit address value, 3-bit position value, and 3-bit configuration are encoded into data-one and/or data-zero bit pairs and transmitted. These are, by definition, the same as received in the select protocol. The bit pairs are to be interpreted in least-significant-bit-first order. If either received address or position do not match that at the A_9–A_0 or P_2–P_0 inputs, respectively, no acknowledge protocol is transmitted and the linking shadow protocol is considered complete.

Protocol Errors

Protocol errors occur when bit pairs are received out of sequence. Some of these sequencing errors can be tolerated and produce protocol result SOFT ERROR, and no specific action occurs as a result. Other errors represent cases where the message information could be incorrectly received and produce protocol result HARD ERROR, and these are characterized by sequences in which at least one bit of message data has been properly transmitted, followed by a sequencing error; when protocol result HARD ERROR occurs, any connection to an LASP is dissolved. Table 1 lists the bit-pair sequences that produce protocol results SOFT ERROR and HARD ERROR. A HARD ERROR also results when the primary TAP state changes during select protocol, following the proper transmission of at least one bit of address data. Figures 5, 6, and 7 show shadow-protocol timing in case of protocol result HARD ERROR, while Figure 8 shows shadow-protocol timing in the case of protocol result SOFT ERROR.

Table 1. Linking Shadow Protocol Errors

SOFT ERROR	HARD ERROR
I(D)I	
I(D)(S)I	
I(D)(S)(D)I	IS(D)I
I(S)I	IS(D)S(D)I
IS(S)(D)I	IS(D)S(S)I
IS(S)(D)(S)I	

Long Address

Receipt of an address longer than ten bits produces protocol result HARD ERROR, and the LASP assumes OFF status. The sole exceptions are when all data 1s are received or all data 0s are received. In these special cases, the global addresses represented by these bit sequences are observed and appropriate action taken. That is, in the case that only data 1s (ten or more) are received, the shadow-protocol result is TEST SYNCHRONIZATION (if the primary TAP state is Pause-DR or Pause-IR) and, in the case that only data 0s (ten or more) are received, the linking shadow-protocol result is RESET (see test-synchronization address and reset address).

Short Address

In all cases, receipt of an address of less than ten bits produces protocol result HARD ERROR, and the LASP assumes OFF status.

Long/Short Command

In all cases, receipt of a command that is not a multiple of six bits produces protocol result HARD ERROR, and the LASP assumes OFF status.

ARCHITECTURE

Blocks for linking shadow protocol receive and linking shadow protocol transmit are responsible for receipt of select protocol and transmission of acknowledge protocol, respectively. Connect control block monitors the primary TAP state to enable receipt/acknowledge of shadow protocols in appropriate states (namely, the stable, non-shift TAP states: Test-Logic-Reset, Run-Test/Idle, Pause-DR, and Pause-IR). Upon receipt of a valid shadow protocol, this block performs the address and position matching required to compute the shadow-protocol result.

Based on the linking shadow protocol result or protocol bypass ($\overline{BYP_4}$–$\overline{BYP_0}$) inputs, the connect control block configures the secondary TAP network. In conjunction, it also sets the states of and $\overline{CON_2}$–$\overline{CON_0}$ outputs.

TAP-State Monitor

The TAP-state monitor is a synchronous finite-state machine that monitors the primary TAP state. The state diagram is shown in Figure 4 and mirrors that specified by IEEE Std 1149.1. The TAP-state monitor proceeds through its states based on the level of PTMS at the rising edge of PTCK. Each state is described both in terms of its significance for LASP devices and for connected IEEE Std 1149.1-compliant devices (called targets). However, the monitor state (primary TAP) can be different from that of disconnected scan chains (secondary TAP).

TEST-LOGIC-RESET

The LASP TAP-state monitor powers up in the Test-Logic-Reset state. Alternatively, the LASP can be forced asynchronously to this state by assertion of its PTRST input. In the stable Test-Logic-Reset state, the LASP is enabled to receive and respond to linking shadow protocols. The LASP does not recognize the TSA in this state. For a target device in the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers also can be reset to their power-up values.

RUN-TEST/IDLE

In the stable Run-Test/Idle state, the LASP is enabled to receive and respond to linking shadow protocols. The LASP does not recognize the TSA in this state. For a target device, Run-Test/Idle is a stable state in which the test logic actively can be running a test or can be idle.

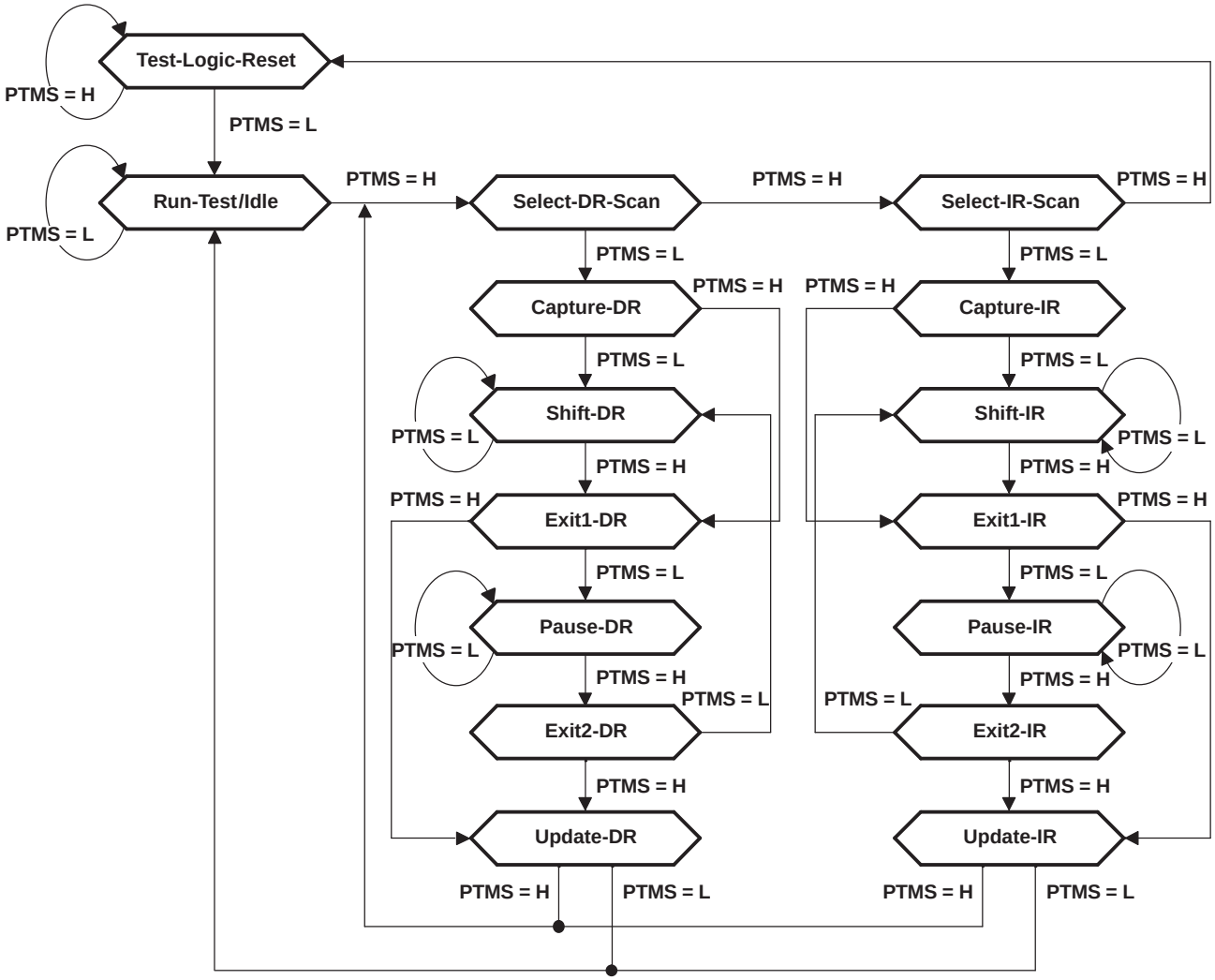


Figure 4. TAP Monitor State Diagram

SELECT-DR-SCAN, SELECT-LR-SCAN

The LASP is not enabled to receive and respond to linking shadow protocols in the Select-DR-Scan and Select-IR-Scan states. For a target device, no specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

CAPTURE-DR

The LASP is not enabled to receive and respond to linking shadow protocols in the Capture-DR state. For a target device in the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK, upon which the Capture-DR state is exited.

SHIFT-DR

The LASP is not enabled to receive and respond to linking shadow protocols in the Shift-DR state. For a target device, upon entry to the Shift-DR state, the selected data register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO outputs the logic level present in the least-significant bit of the selected data register. While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle.

EXIT1-DR, EXIT2-DR

The LASP is not enabled to receive and respond to linking shadow protocols in the Exit1-DR and Exit2-DR states. For a target device, the Exit1-DR and Exit2-DR states are temporary states that end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

PAUSE-DR

In the stable Pause-DR state, the LASP is enabled to receive and respond to linking shadow protocols. Additionally, the TSA can be recognized in this state. For target devices, no specific function is performed in the stable Pause-DR state. The Pause-DR state suspends and resumes data-register scan operations without loss of data.

UPDATE-DR

The LASP is not enabled to receive and respond to linking shadow protocols in the Update-DR state. For a target device, if the current instruction calls for the selected data register to be updated with current data, such update occurs on the falling edge of TCK, following entry to the Update-DR state.

CAPTURE-IR

The LASP is not enabled to receive and respond to linking shadow protocols in the Capture-IR state. For a target device in the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK, upon which the Capture-IR state is exited.

SHIFT-IR

The LASP is not enabled to receive and respond to linking shadow protocols in the Shift-IR state. For a target device, upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO outputs the logic level present in the least-significant bit of the instruction register. While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle.

EXIT1-IR, EXIT2-IR

The LASP is not enabled to receive and respond to linking shadow protocols in the Exit1-IR and Exit2-IR states. For target devices, the Exit1-IR and Exit2-IR states are temporary states that end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

PAUSE-IR

In the stable Pause-IR state, the LASP is enabled to receive and respond to linking shadow protocols. Additionally, the TSA can be recognized in this state. For target devices, no specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state suspends and resumes instruction-register scan operations without loss of data.

UPDATE-IR

The LASP is not enabled to receive and respond to linking shadow protocols in the Update-IR state. For target devices, the current instruction is updated and takes effect on the falling edge of TCK, following entry to the Update-IR state.

Address Matching

Connect status of the LASP is computed by a match of the address received in the last valid linking-shadow protocol against that at the address (A_9–A_0) inputs as well as against the three dedicated addresses that are internal to the LASP (DSA, RSA, and TSA). Table 2 shows the address map.

Table 2. Address Map

ADDRESS NAME	BINARY CODE	HEX CODE	LINK SHADOW PROTOCOL RESULT	RESULTANT PRIMARY-TO-SECONDARY CONNECT STATUS
Reset address (RSA)	0000000000	000	RESET	RESET
Matching address	A_9–A_0	A_9–A_0	MATCH	ON
Disconnect address (DSA)	1111111110	3FE	DISCONNECT	OFF
Test synchronization address (TSA)	1111111111	3FF	TEST SYNCHRONIZATION	MULTICAST
All other addresses	All others	All others	NO MATCH	OFF

Upon receipt of a valid linking shadow protocol, if the linking shadow protocol address and position match the address inputs A_9–A_0 and position inputs P_2–P_0, respectively, the LASP responds by transmitting an acknowledge protocol. Following the complete transmission of the acknowledge protocol, the LASP assumes ON status, in which the secondary TAPs are configured as requested by the linking shadow protocol. The ON status allows the scan chains associated with the LASP secondary TAPs to be controlled from the multidrop primary TAP as if it were directly wired as such. Figures 9 and 10 show the linking shadow protocol timing for MATCH result when the prior LASP connect status is ON and OFF, respectively. If the linking-shadow protocol address or position does not match the address inputs A_9–A_0 or position inputs P_2–P_0 (unless the address is one of the three dedicated global addresses described below), the LASP responds immediately by assuming the OFF status, in which PTDO and $STDO_2$–$STDO_0$ are high impedance and $STMS_2$–$STMS_0$ are held at their last levels. This has the effect of deselecting the scan chains associated with the LASP secondary TAPs, but leaves the TAP state of the scan chains unchanged. No acknowledge protocol is sent. Figures 11 and 12 show the linking shadow protocol timing for a NO MATCH result when the prior LASP connect status is ON and OFF, respectively.

DISCONNECT ADDRESS

The disconnect address (DSA) is one of the three internally dedicated addresses that are recognized globally. When an LASP receives the DSA, it immediately responds by assuming the OFF status, in which PTDO and $STDO_2$–$STDO_0$ are high impedance and $STMS_2$–$STMS_0$ are held at their last levels. This has the effect of deselecting the scan chain associated with the LASP secondary TAP, but leaves the TAP state of the scan chain unchanged. No acknowledge protocol is sent. Figures 13 and 14 show the linking shadow protocol timing for DISCONNECT result when the prior LASP connect status is ON and OFF, respectively. The same result occurs when a nonmatching address is received. No specific action to disconnect an LASP is required, as a given LASP is disconnected by the address that connects another. The dedicated DSA ensures that at least one address is available for the purpose of disconnecting all receiving LASPs. It is especially useful when the currently selected scan chain is in a different TAP state than that to be selected. In such a case, the DSA is used to leave the former scan chain in the proper state, after which the primary TAP state is moved to that needed to select the latter scan chain.

RESET ADDRESS

The reset address (RSA) is one of the three internally dedicated addresses that are recognized globally. When an LASP receives the RSA, it immediately responds by assuming the RESET status in which PTDO and $STDO_2$–$STDO_0$ are at high impedance and $STMS_2$–$STMS_0$ are forced to the high level. This has the effect of deselecting and resetting to Test-Logic-Reset state the scan chain associated with the LASP secondary TAP. No acknowledge protocol is sent. Figures 15 and 16 show the linking shadow protocol timing for RESET result when the prior LASP connect status is ON and OFF, respectively.

TEST SYNCHRONIZATION ADDRESS

The test synchronization address (TSA) is one of the three internally dedicated addresses that are recognized globally. When an LASP receives the TSA, it immediately responds by assuming the MULTICAST status, in which PTDI and PTMS are connected to STDO and STMS, respectively, of only those secondary TAPs whose TAP state is Pause-DR or Pause-IR while PTDO is high impedance. No acknowledge protocol is sent. The result of receipt of TSA on a secondary TAP whose TAP state is Test-Logic-Reset or Run-Test-Idle is disconnect. Figures 17 and 18 show the linking shadow protocol timing for TEST SYNCHRONIZATION result when the prior LASP connect status is ON and OFF, respectively. The TSA allows simultaneous operation of the scan chains of all selected LASPs, either for global TAP-state movement or for scan input of common serial test data via PTDI. This is especially useful in the former case, to simultaneously move such scan chains into the Run-Test/Idle state in which module-level or module-to-module BIST operations can operate synchronous to TCK in that TAP state and, in the later case, to scan common test setup/data into multiple like modules. In conjunction with the use of the pass-through input/output pairs (PX to SX_2–SX_0 and PY to SY_2–SY_0), the multicast mode can be effective for ISP of like modules.

Protocol Bypass

Protocol bypass is selected by a low $\overline{BYP_5}$ input. This protocol-bypass mode forces the LASP into BYP status. The remaining bypass $\overline{BYP_4}$–$\overline{BYP_0}$ inputs are used for configuring the primary-to-secondary TAP connections, regardless of previous linking shadow protocol results, and the corresponding $\overline{CON_2}$–$\overline{CON_0}$ outputs are made active (low). Receipt of the linking shadow protocols is disabled. When $\overline{BYP_5}$ is taken low, the primary-to-secondary TAP connections are configured immediately (asynchronously to PTCK). The PTMS signal also is connected to its respective secondary TAP signal $STMS_2$–$STMS_0$ unless $\overline{PTRST}$ is low, in which case $STMS_2$–$STMS_0$ remain high until $\overline{PTRST}$ is released. Also, the linking-shadow protocol receive block is reset to its power-up state and is held in this state, such that select protocols appearing at the primary TAP are ignored. When the $\overline{BYP_5}$ input is released (taken high), the LASP immediately (asynchronously to PTCK) resumes the connect status selected by the last valid linking shadow protocol. The linking shadow protocol receive block again is enabled to respond to select protocols. Figures 19 and 20 show protocol-bypass timing when the LASP connect status before $\overline{BYP_5}$ active is ON and OFF, respectively.

Asynchronous Reset

While the $\overline{PTRST}$ input always is buffered directly to the $STRST_2$–$STRST_0$ outputs, it also serves as an asynchronous reset for the LASP. Given that $\overline{BYP_5}$ is high, when $\overline{PTRST}$ goes low, the LASP immediately assumes TRST status, in which $\overline{CON_2}$–$\overline{CON_0}$ are high and PTDO and $STDO_2$–$STDO_0$ are at high impedance. Otherwise, if $\overline{BYP_5}$ is low, the LASP assumes BYP/TRST status. In either case, $STMS_2$–$STMS_0$ are set high so that connected IEEE Std 1149.1-compliant devices can be driven synchronously to their Test-Logic-Reset states. While $\overline{PTRST}$ is low, receipt of linking shadow protocols is disabled. Figures 21 and 22 show asynchronous reset timing when the LASPs connect status before $\overline{PTRST}$ active is ON and OFF, respectively. Figure 23 shows asynchronous reset timing when $\overline{BYP_5}$ is low.

Connect Indicators

The $\overline{CON_2}$–$\overline{CON_0}$ outputs indicate secondary-scan-port activity ($STDO_2$–$STDO_0$, $STMS_2$–$STMS_0$ active), regardless of whether such activity is achieved via protocol bypass or linking shadow protocol. When acknowledge protocol is in progress, the $\overline{CON_2}$–$\overline{CON_0}$ outputs are high.

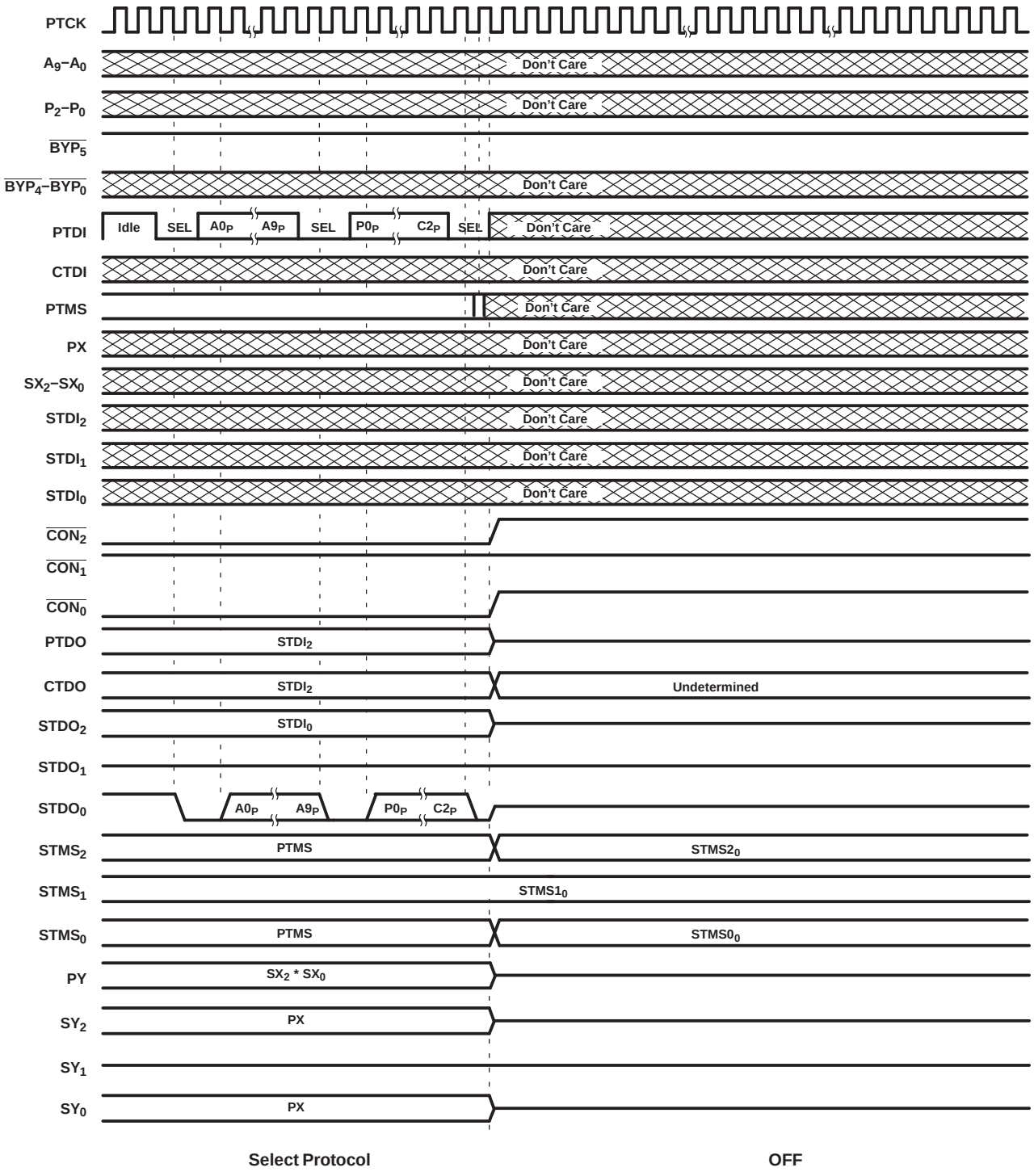


Figure 5. Linking Shadow Protocol Timing
Protocol Result = HARD ERROR (PTMS Change During Select Protocol);
Prior Connect Status = TAP2-ON, TAP1-OFF, TAP0-ON

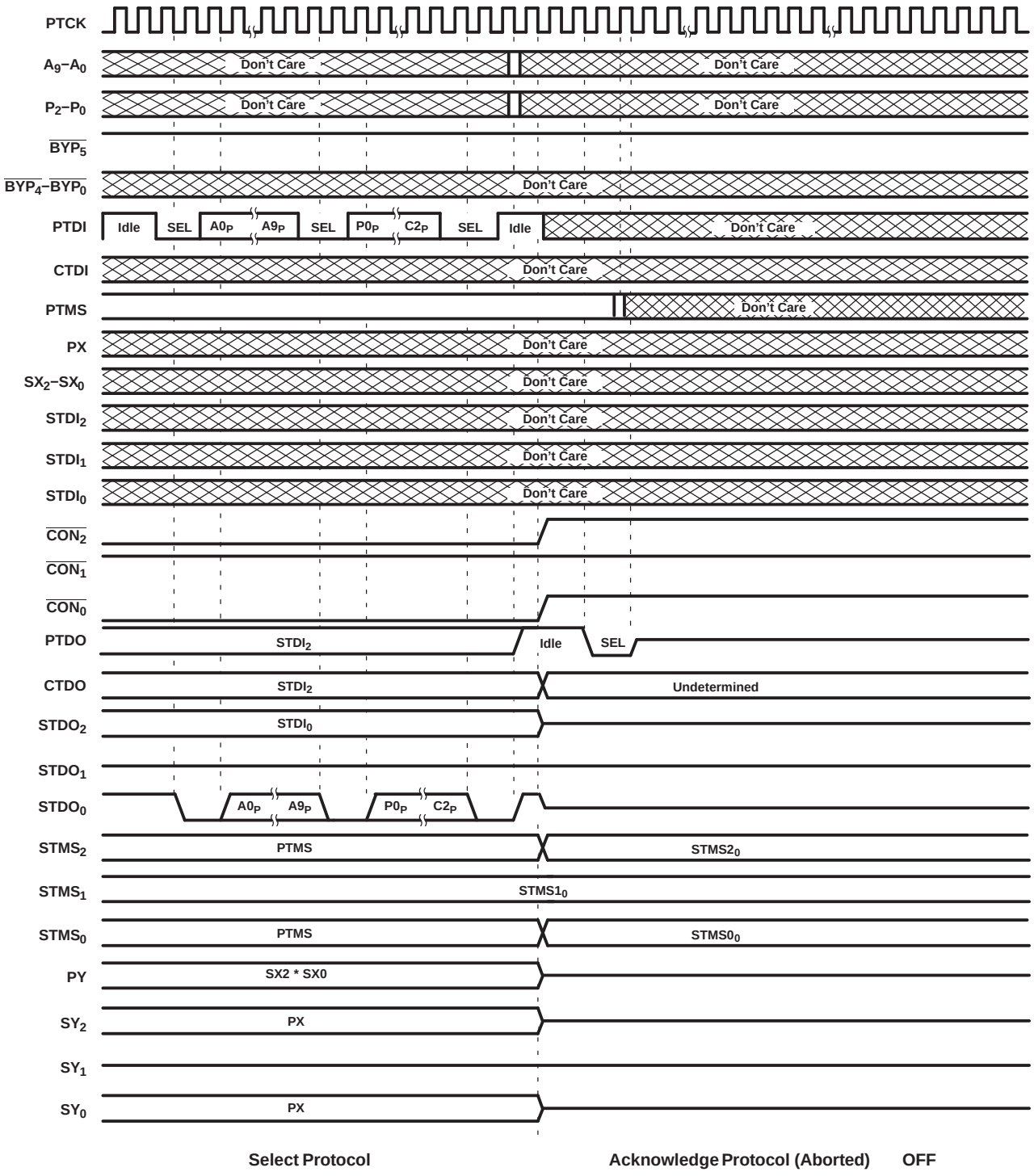


Figure 6. Linking Shadow Protocol Timing
Protocol Result = HARD ERROR (PTMS Change During Acknowledge Protocol);
Prior Connect Status = TAP2-ON, TAP1-OFF, TAP0-ON

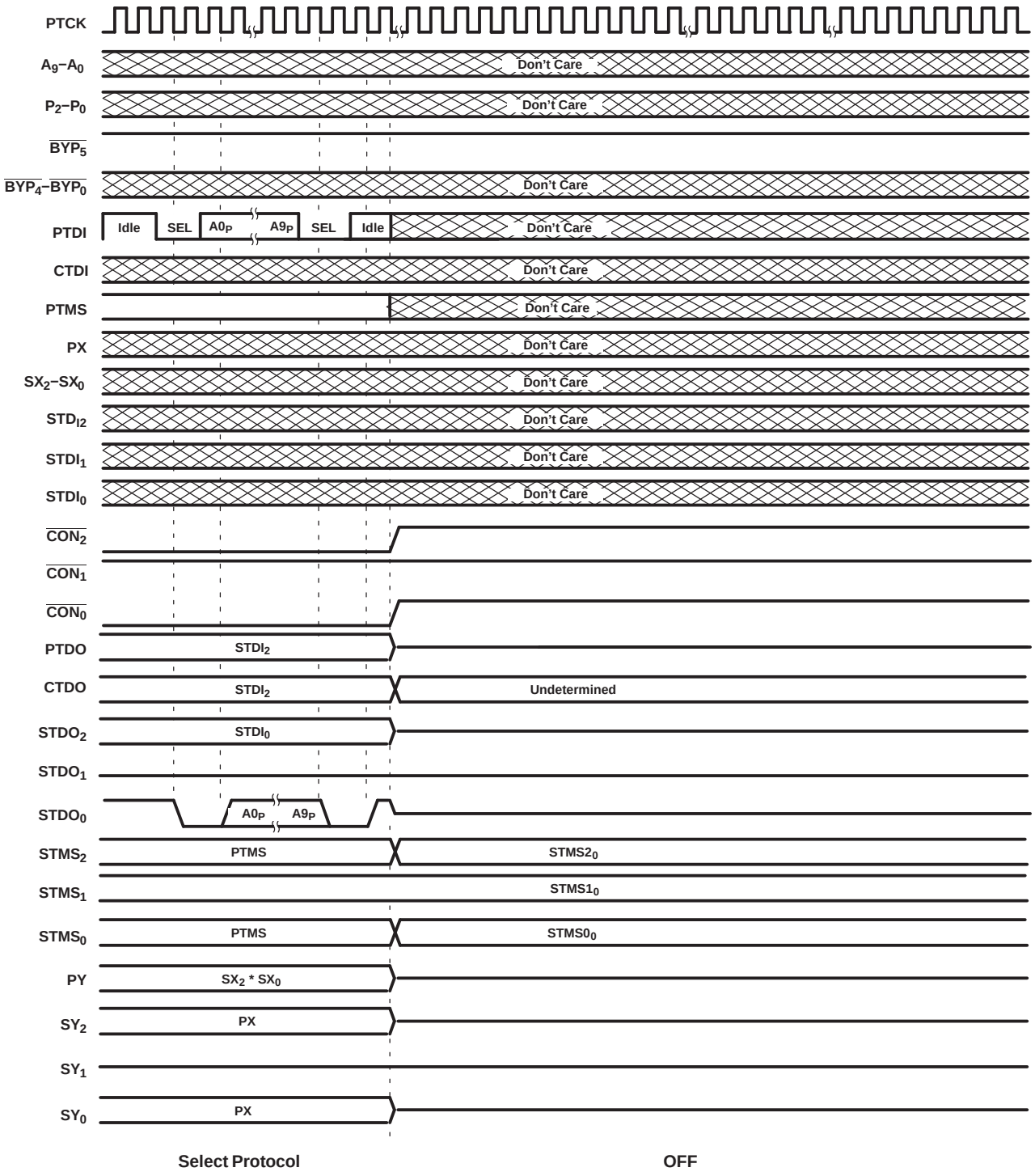


Figure 7. Linking Shadow Protocol Timing
Protocol Result = HARD ERROR (No Command);
Prior Connect Status = TAP2-ON, TAP1-OFF, TAP0-ON

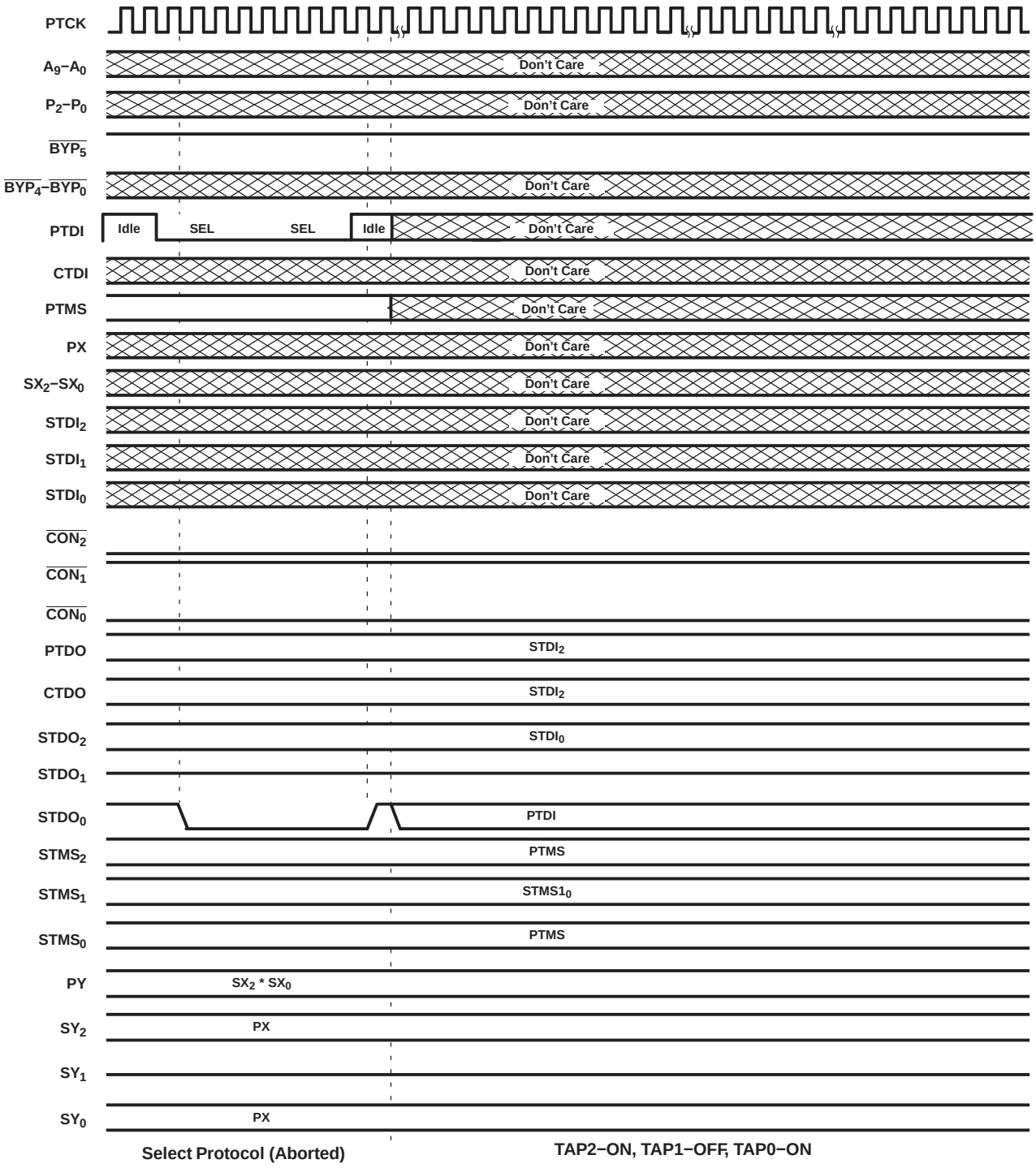


Figure 8. Linking Shadow Protocol Timing
Protocol Result = SOFT ERROR; Prior Connect Status = TAP2-ON, TAP1-OFF, TAP0-ON

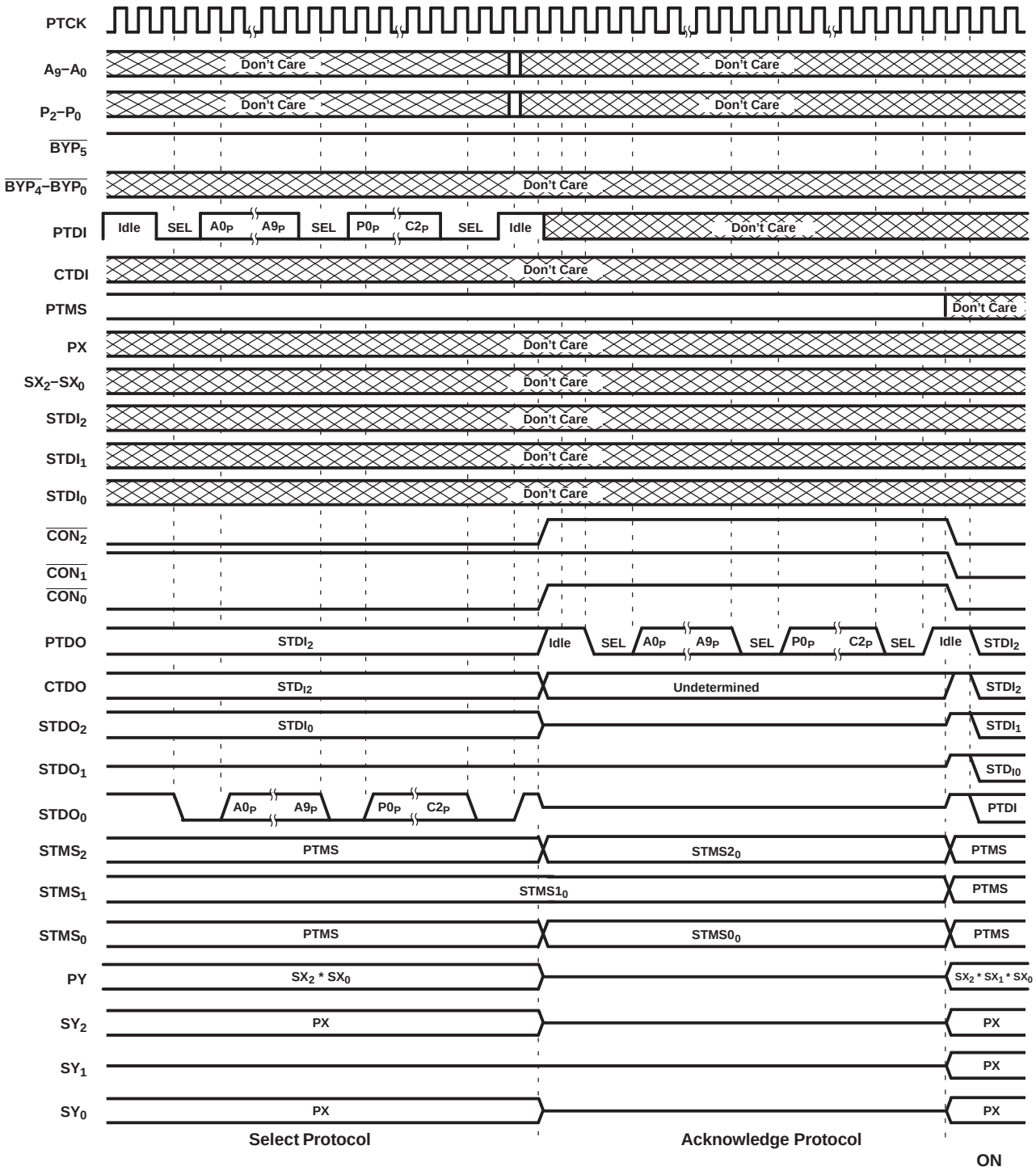


Figure 9. Linking Shadow Protocol Timing
Protocol Result = MATCH; Prior Connect Status = TAP2-ON, TAP1-OFF, TAP0-ON

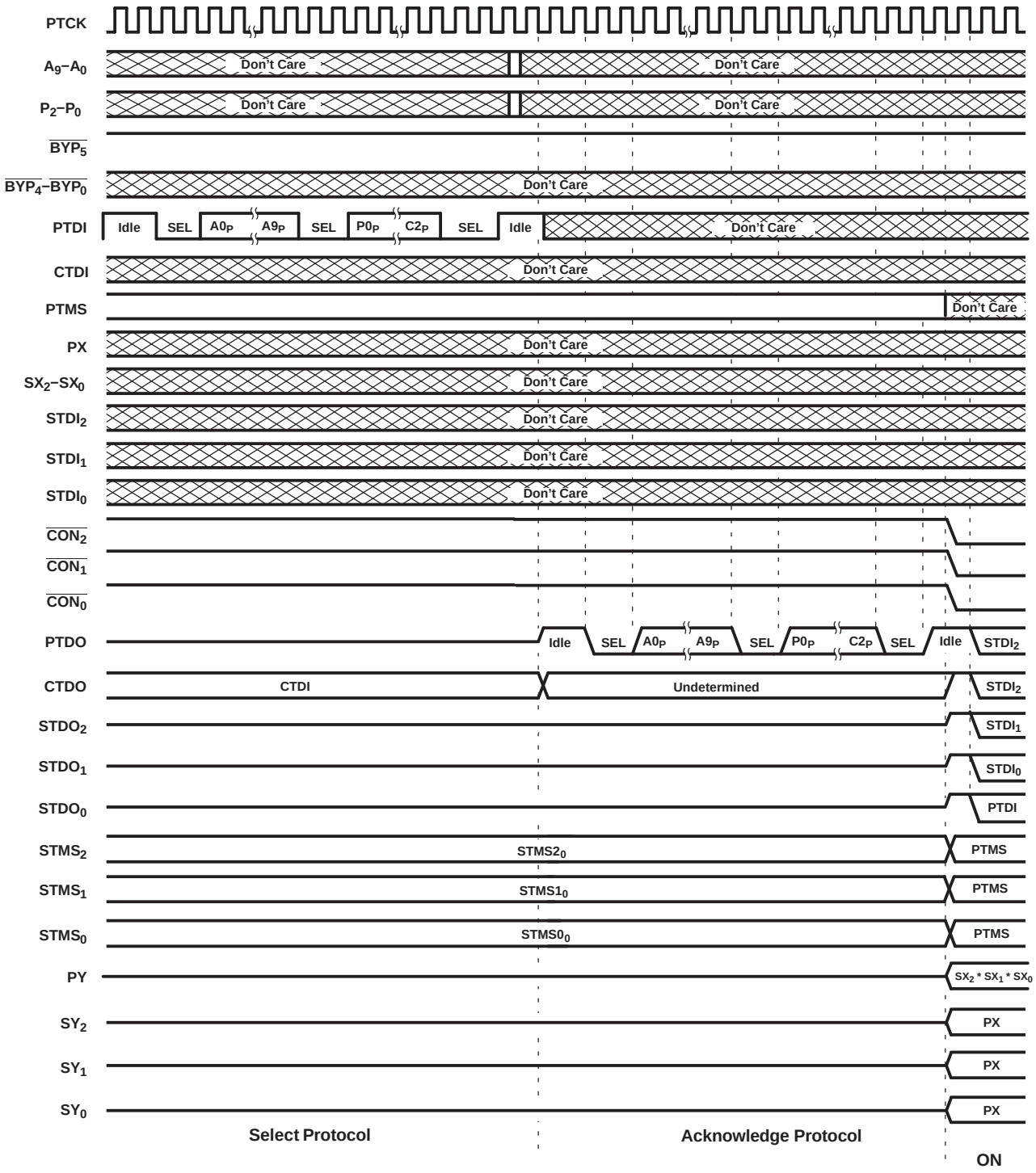


Figure 10. Linking Shadow Protocol Timing
Protocol Result = MATCH; Prior Connect Status = OFF

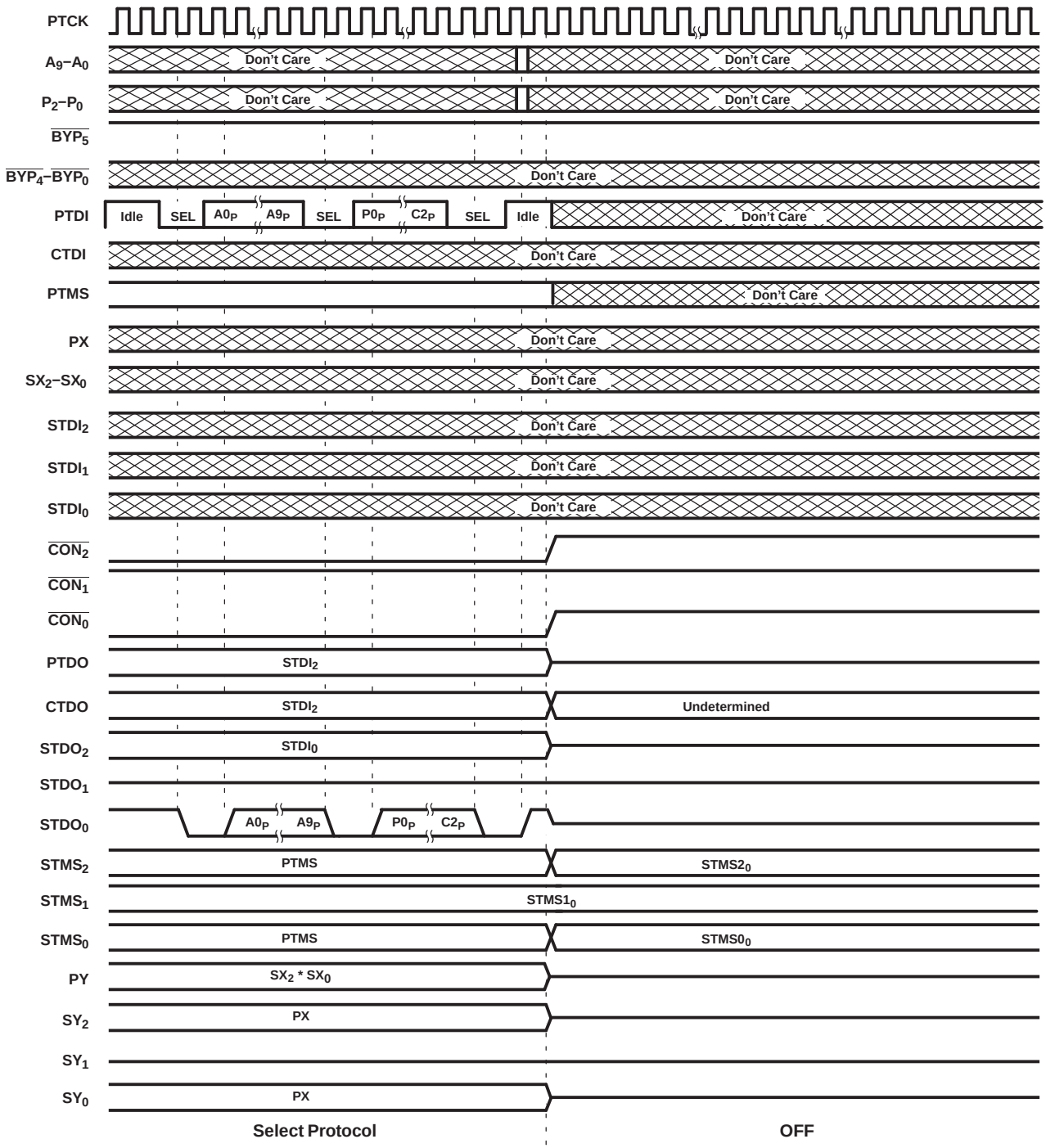


Figure 11. Linking Shadow Protocol Timing
Protocol Result = NO MATCH; Prior Connect Status = TAP2-ON, TAP1-OFF, TAP0-ON

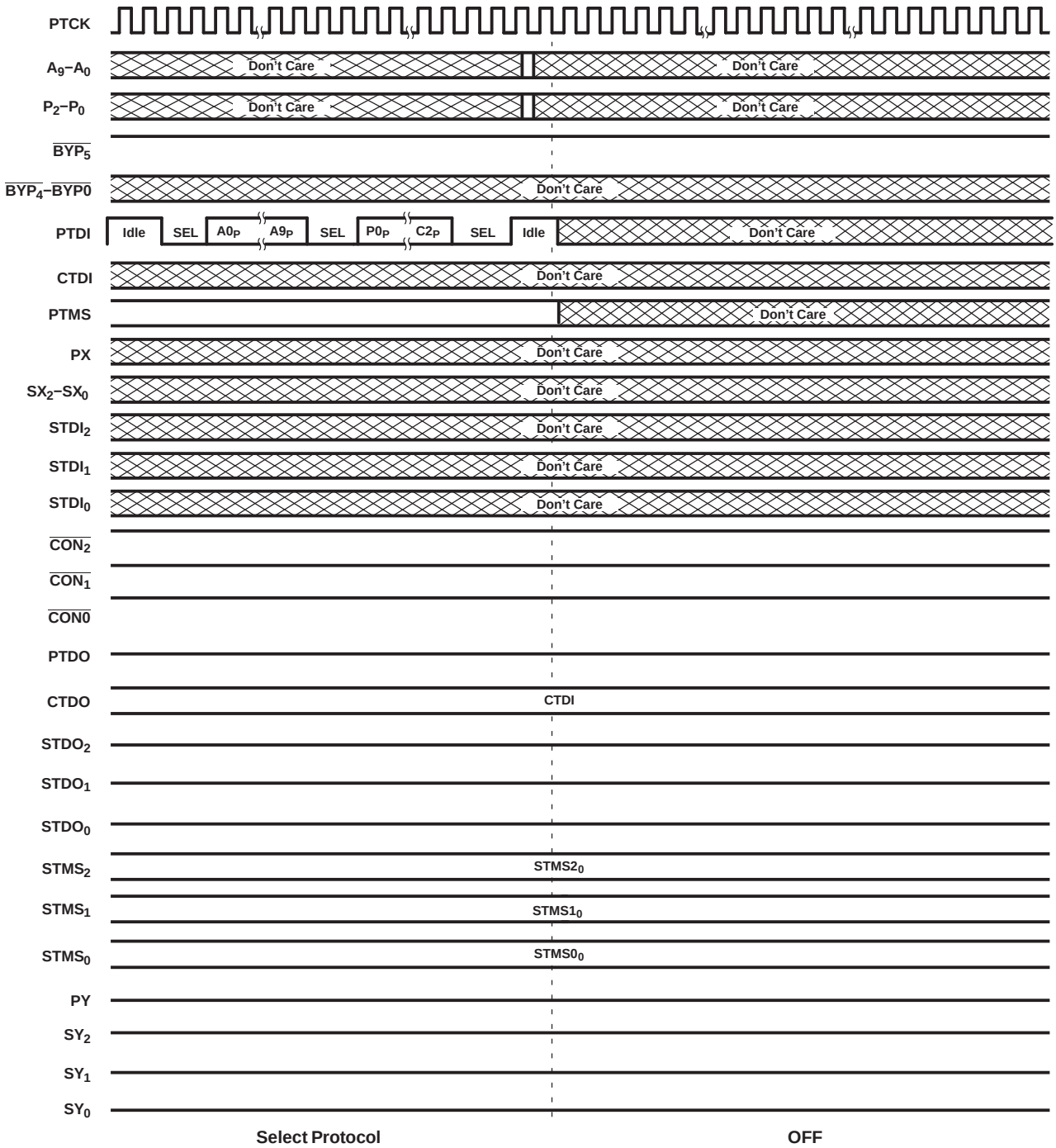


Figure 12. Linking Shadow Protocol Timing
Protocol Result = NO MATCH; Prior Connect Status = OFF

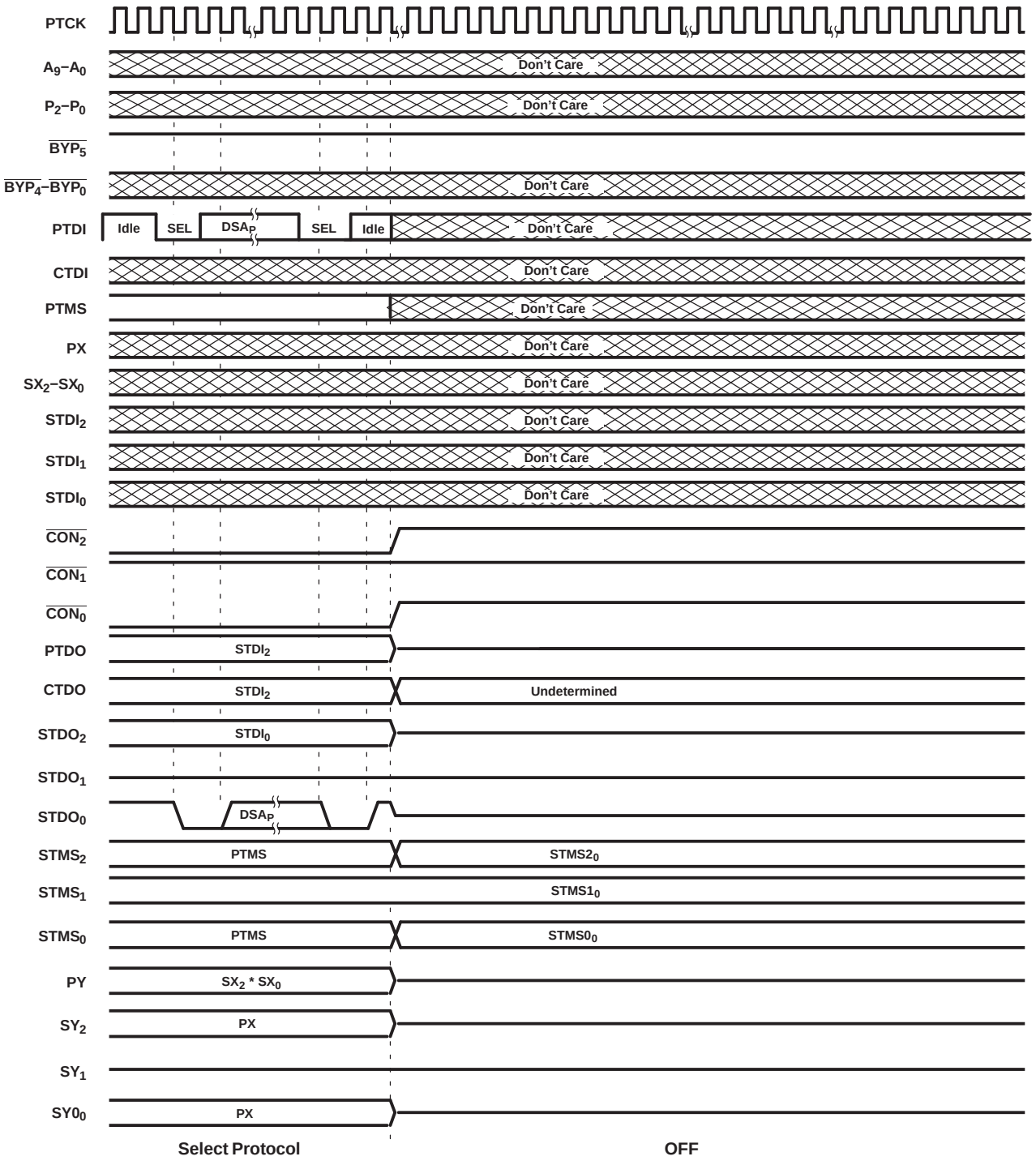


Figure 13. Linking Shadow Protocol Timing
Protocol Result = DISCONNECT; Prior Connect Status = TAP2-ON, TAP1-OFF, TAP0-ON

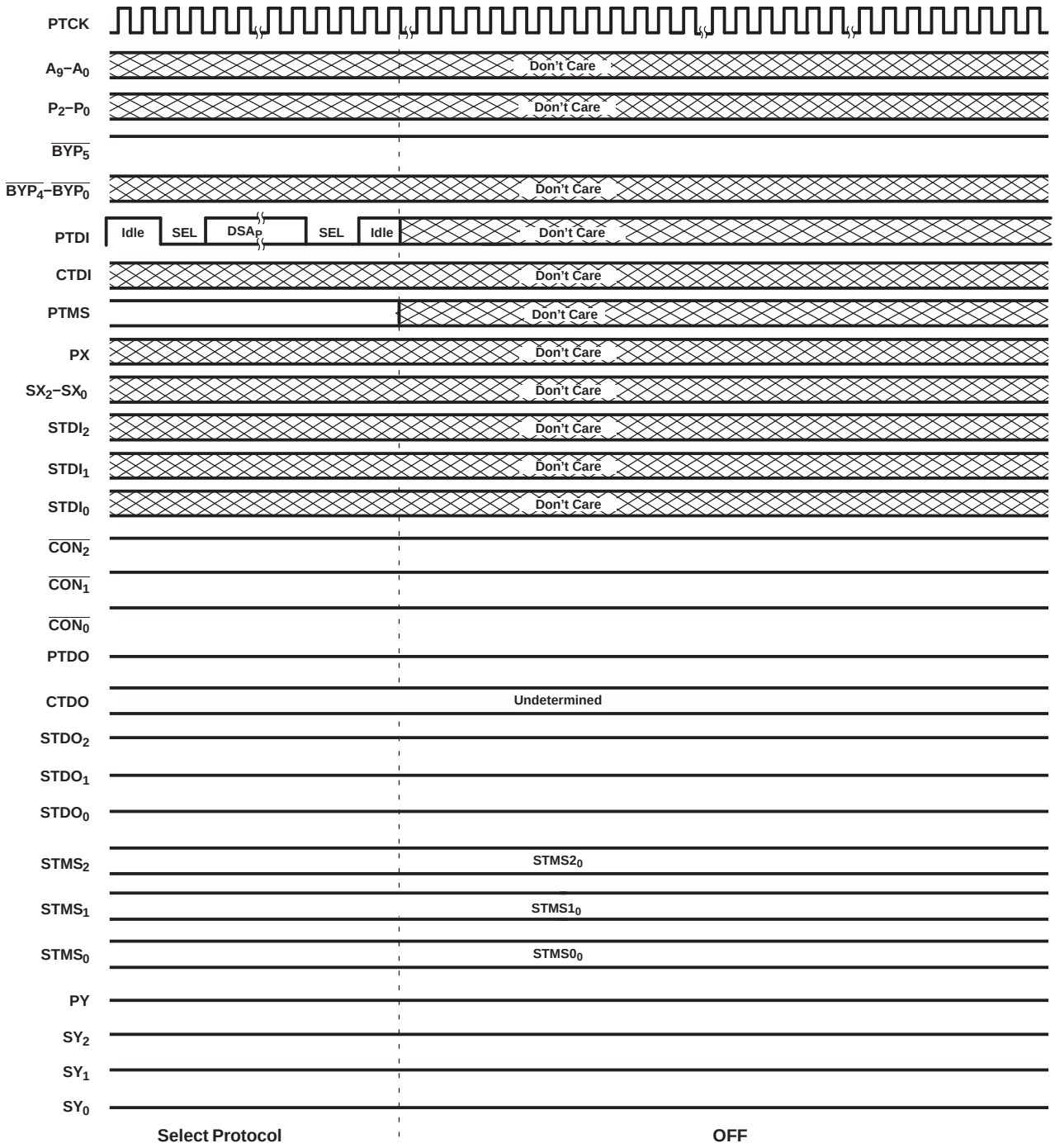


Figure 14. Linking Shadow Protocol Timing
Protocol Result = DISCONNECT; Prior Connect Status = OFF

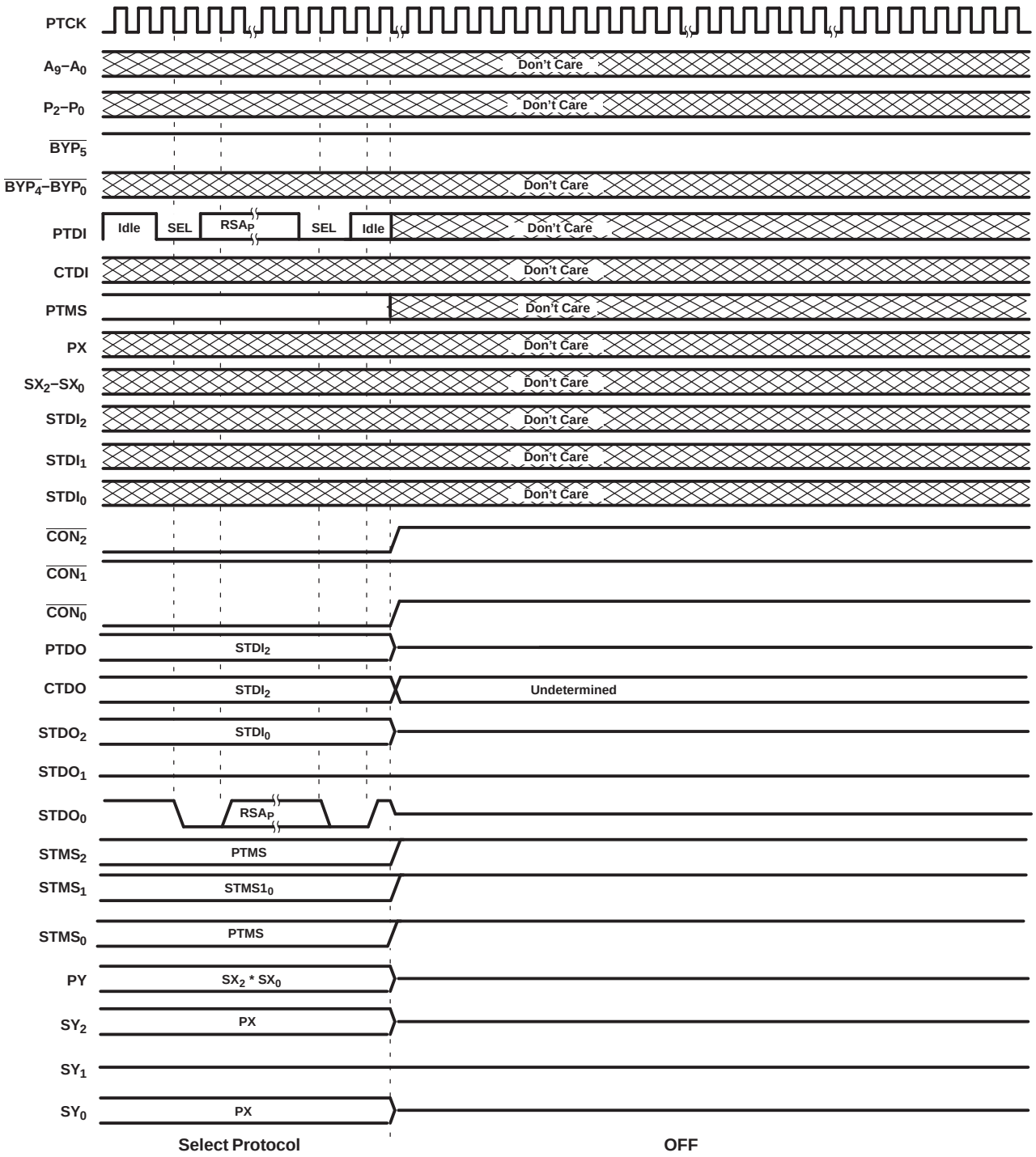


Figure 15. Linking Shadow Protocol Timing
Protocol Result = RESET; Prior Connect Status = TAP2-ON, TAP1-OFF, TAP0-ON

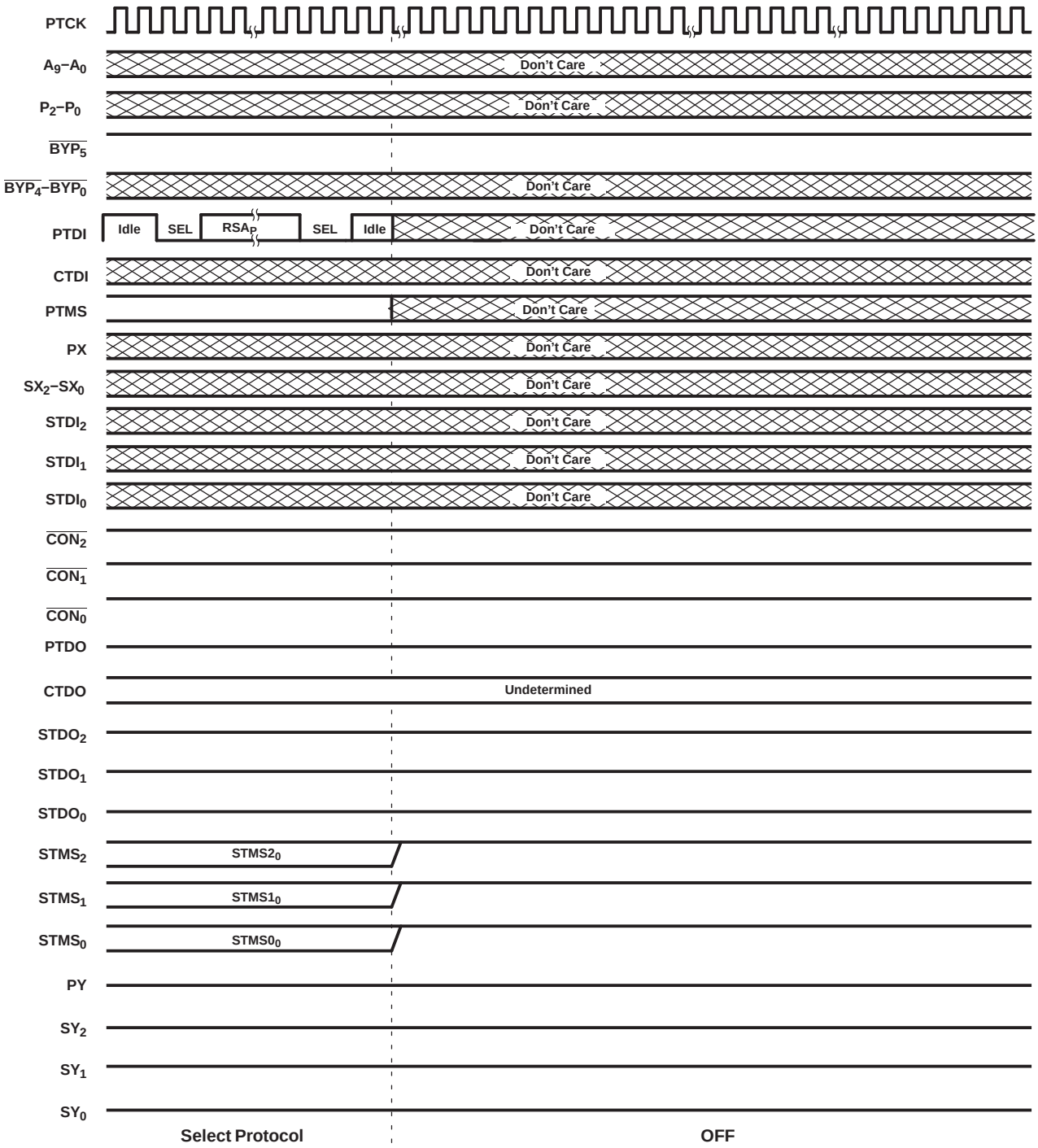


Figure 16. Linking Shadow Protocol Timing
Protocol Result = RESET; Prior Connect Status = OFF

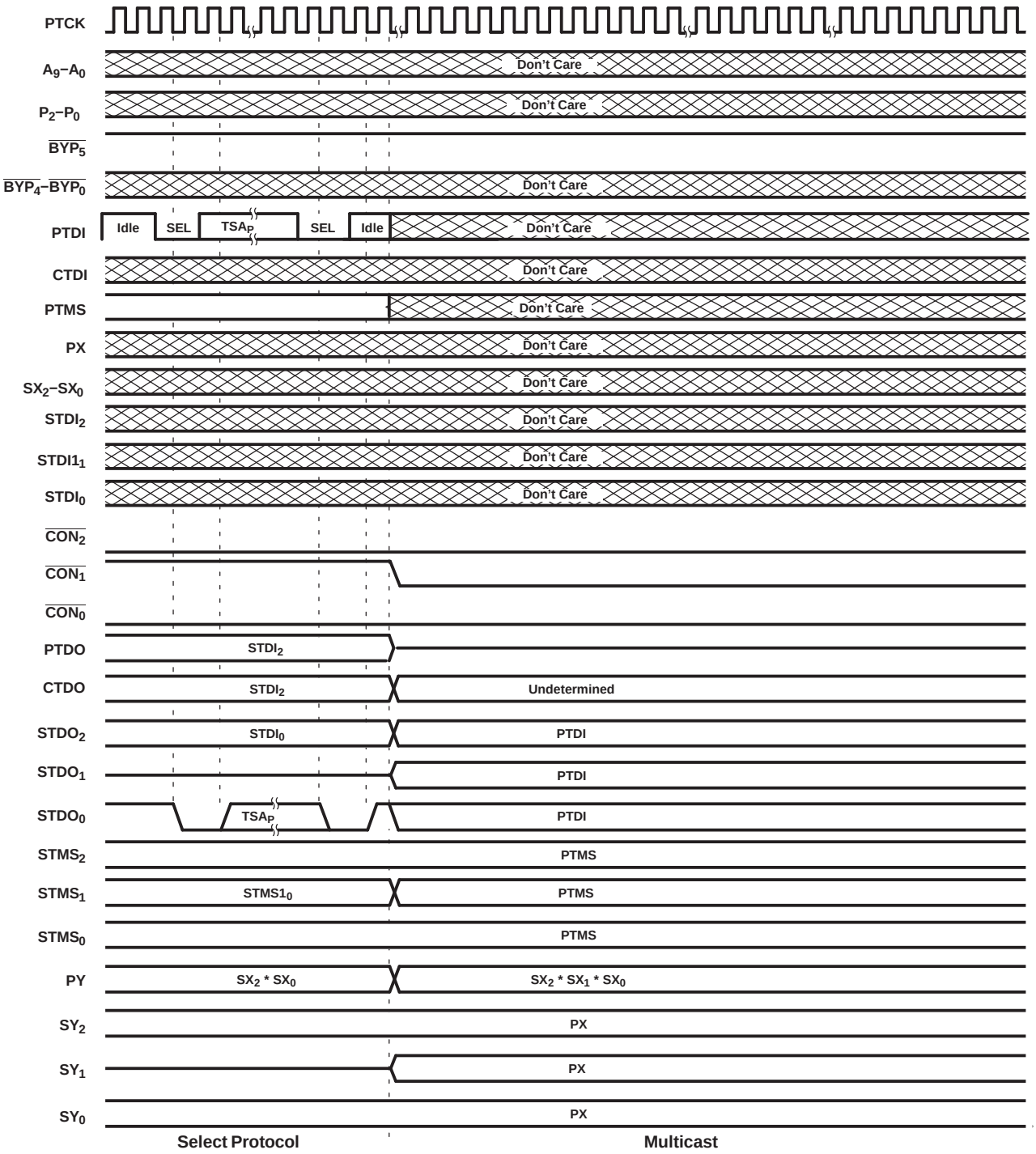


Figure 17. Linking Shadow Protocol Timing
Protocol Result = TEST SYNCHRONIZATION (all on);
Prior Connect Status = TAP2-ON, TAP1-OFF, TAP0-ON

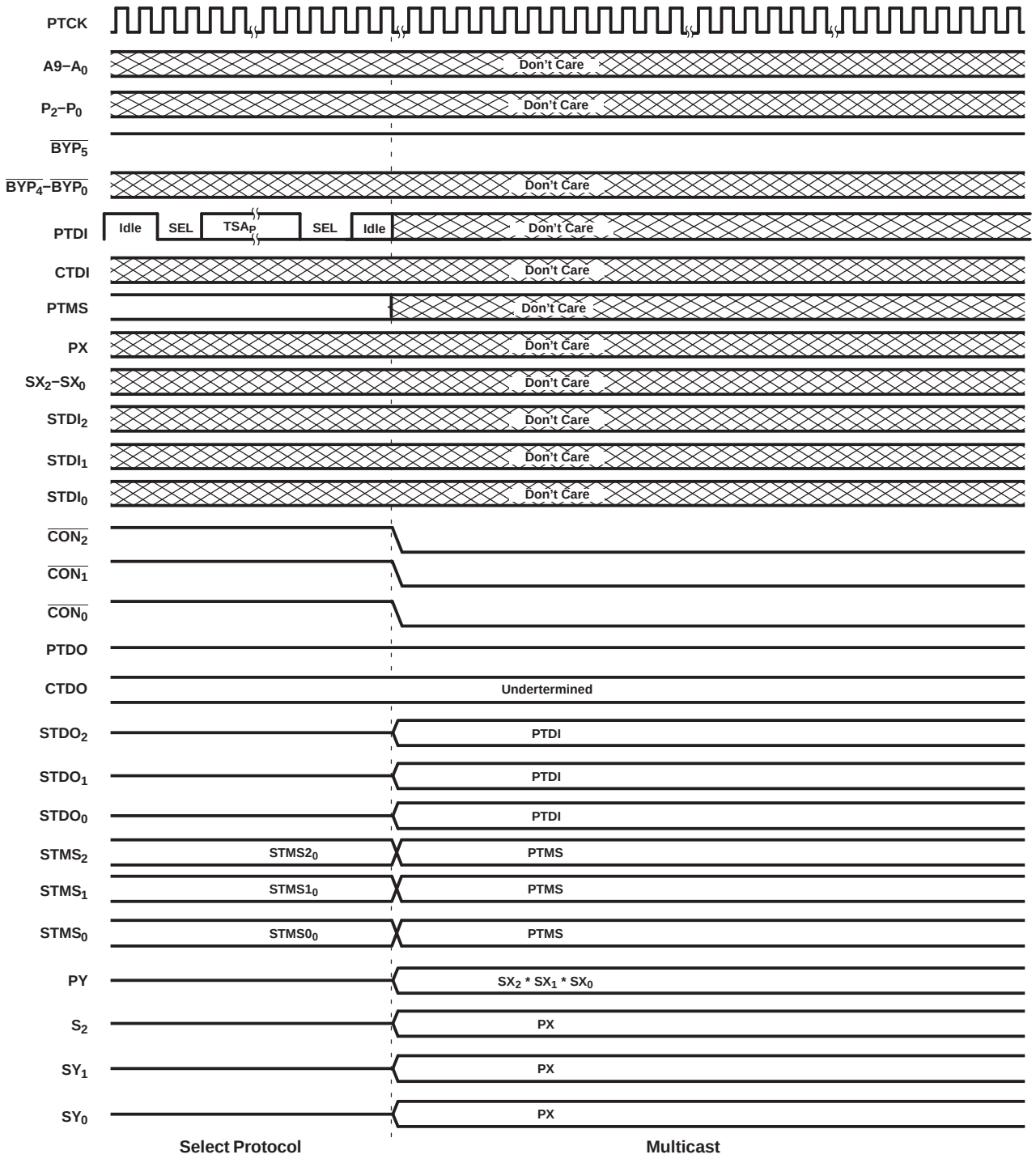


Figure 18. Linking Shadow Protocol Timing
Protocol Result = TEST SYNCHRONIZATION (all on); Prior Connect Status = OFF

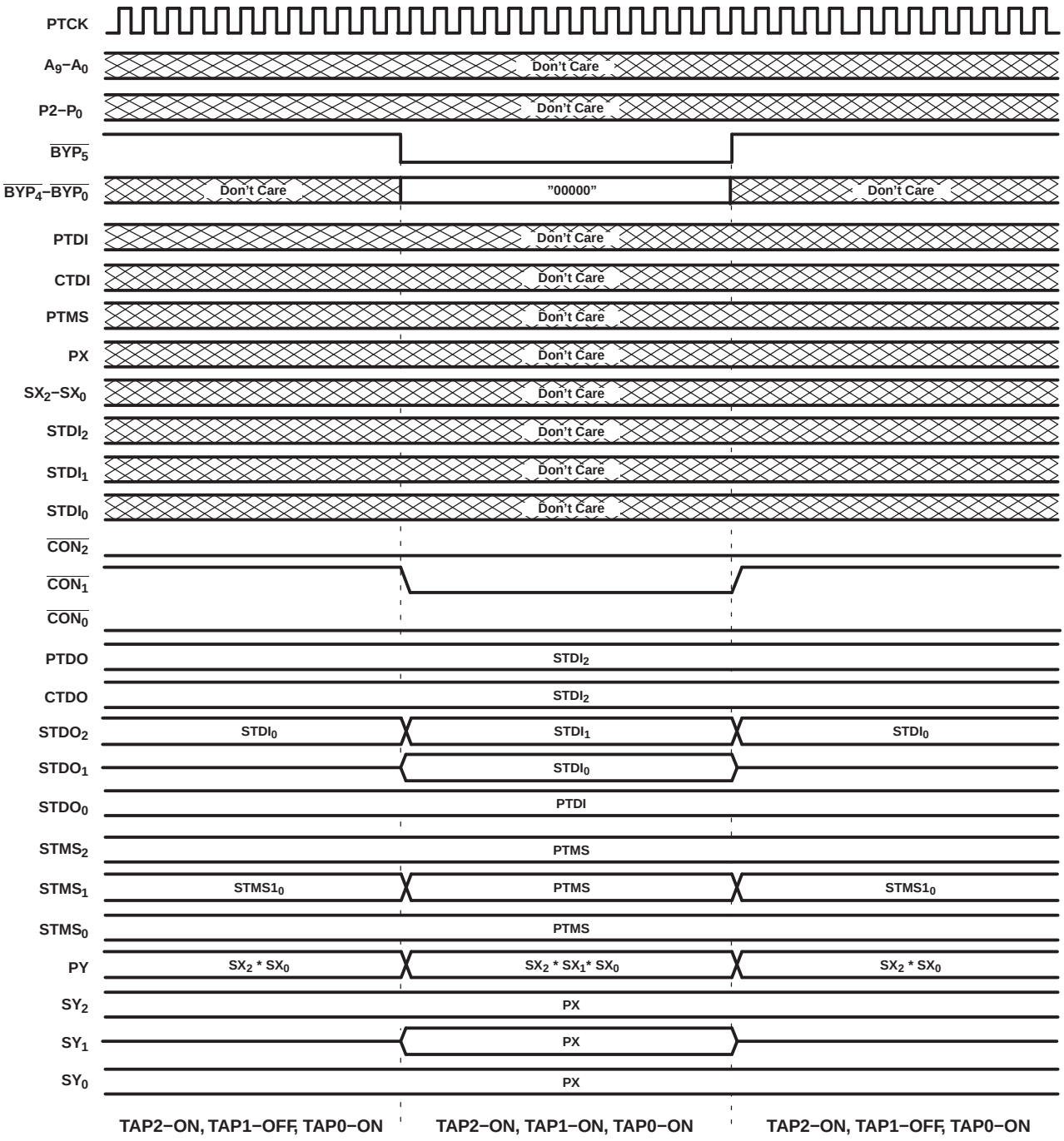


Figure 19. Protocol Bypass Timing, All TAPs ON, Stand-Alone Device, Prior Connect Status = TAP2-ON, TAP1-OFF, TAP0-ON

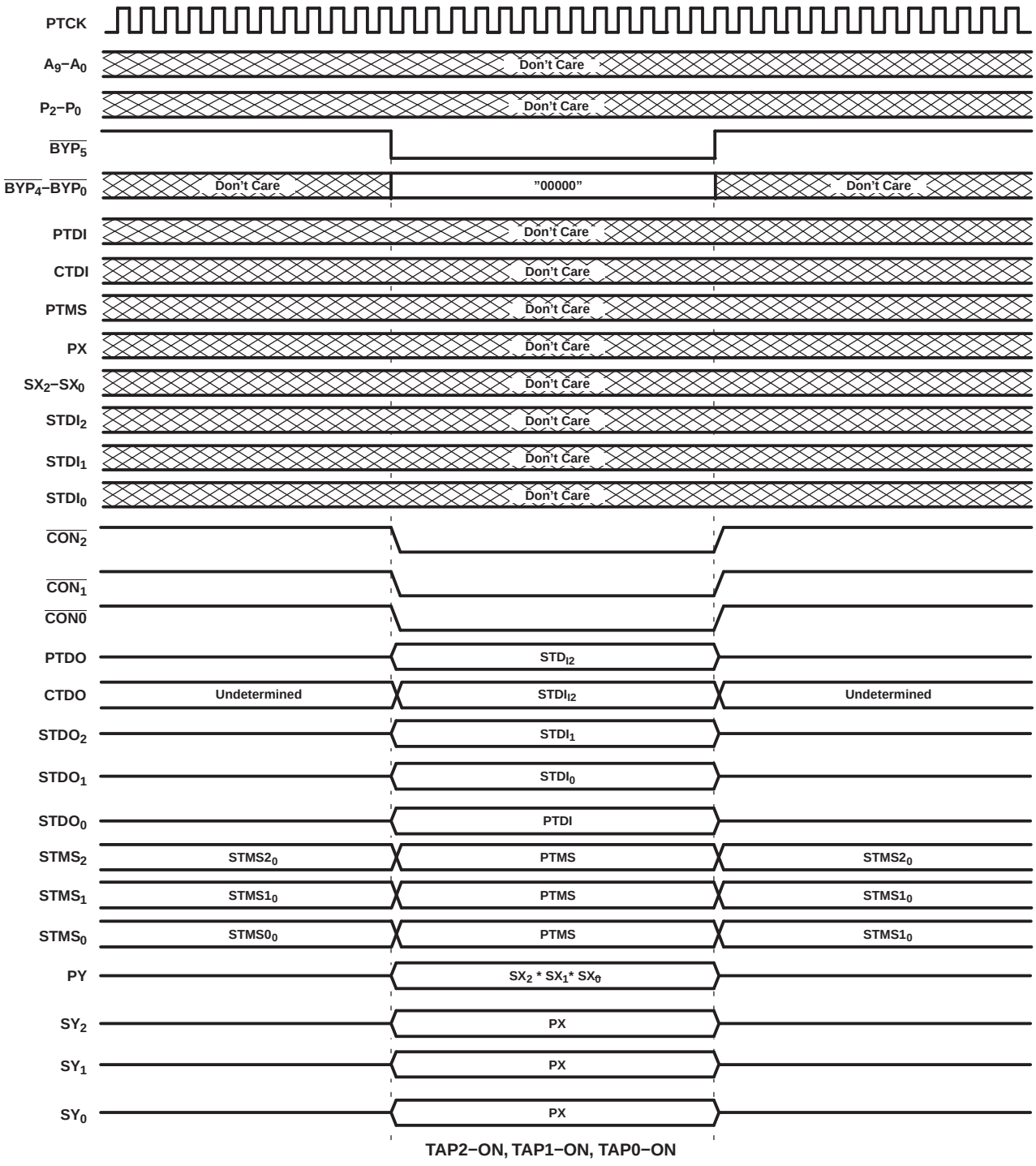


Figure 20. Protocol Bypass Timing, All TAPs ON, Stand-Alone Device, Prior Connect Status = OFF

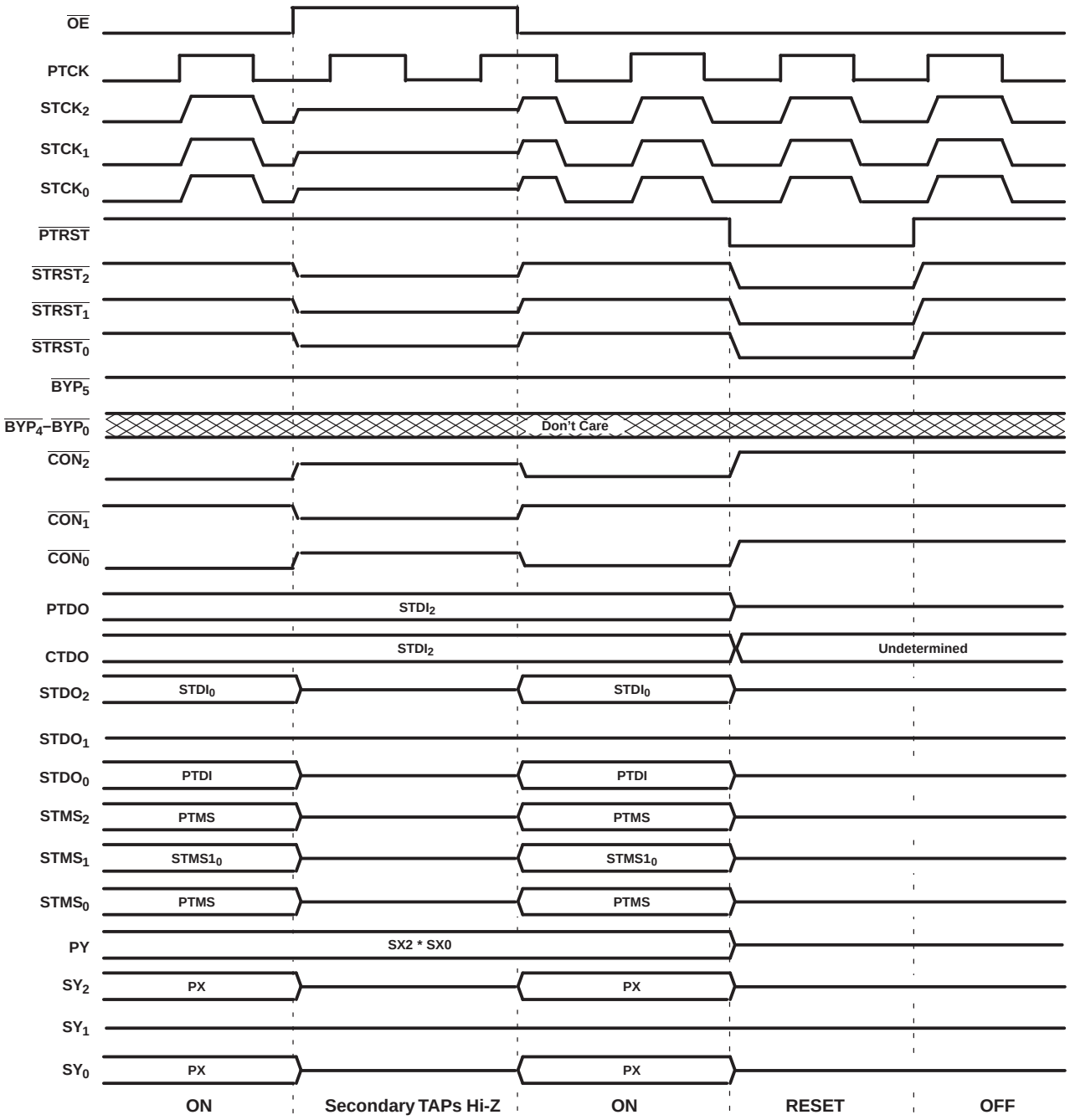


Figure 21. Asynchronous Reset and Output-Enable Timing, Prior Connect Status = TAP2-ON, TAP1-OFF, TAP0-ON

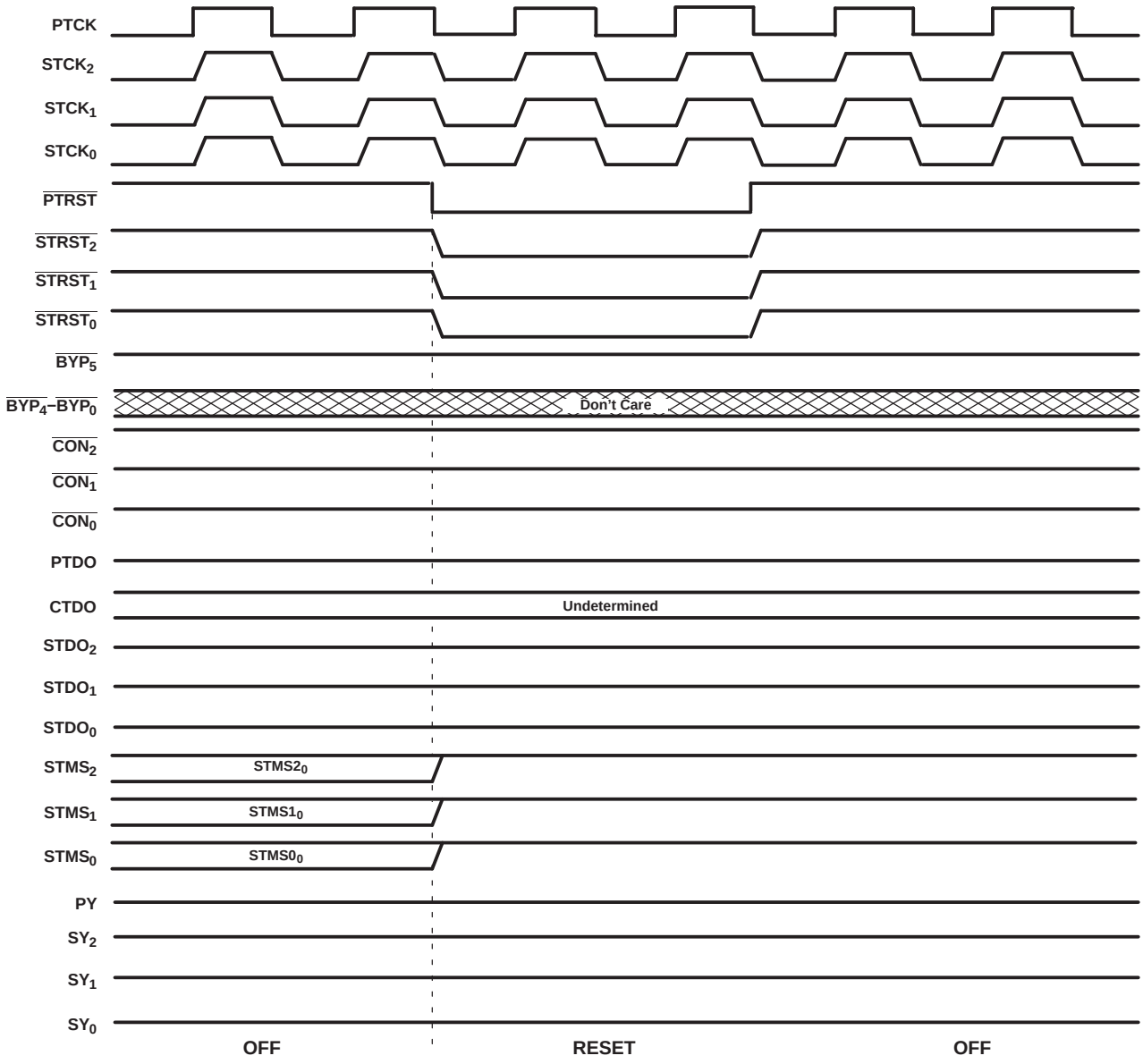


Figure 22. Asynchronous Reset Timing, Prior Connect Status = OFF

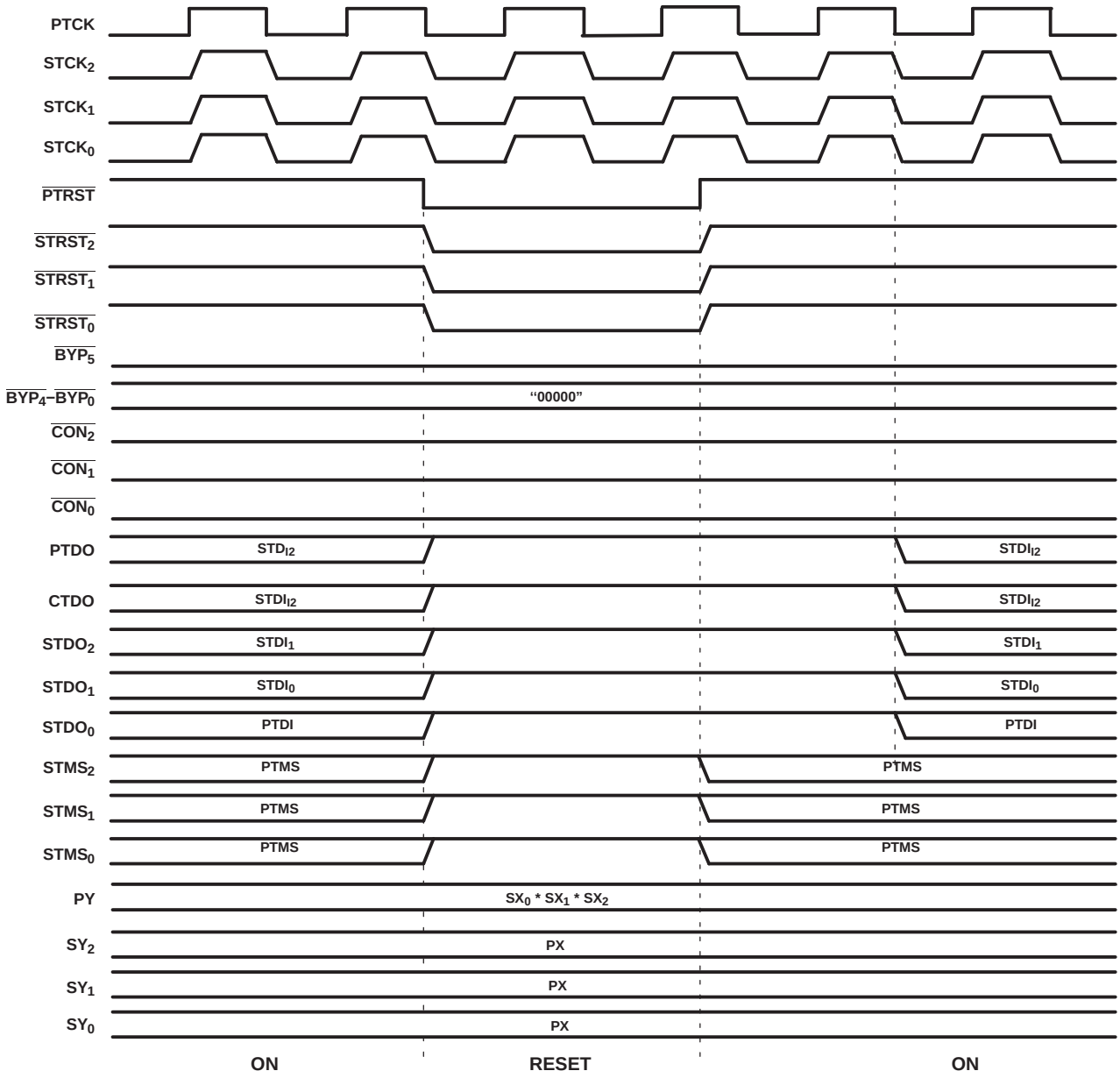


**Figure 23. Asynchronous Reset Timing,
Bypass Mode, Prior Connect Status = All ON**

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range(2)		–0.7	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	7	V
I_{OL}	Current into any output in the low state	SN54LVT8986		96	mA
		SN74LVT8986		128	
I_O	Current into any output in the high state(3)	SN54LVT8986		48	mA
		SN74LVT8986		64	
I_{IK}	Input clamp current	$V_I < 0$		±20	mA
I_{OK}	Output clamp current	$V_O < 0$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±35	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
(3) This current flows only when the output is in the high state and $V_O < V_{CC}$

Recommended Operating Conditions

		SN54LVT88986(1)		SN74LVT88986		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		µs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

(1) Product Preview

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVT8986(1)			SN74LVT8986			UNIT
				MIN	TYP(2)	MAX	MIN	TYP(2)	MAX	
V_{IK}		V_{CC} = 2.7 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}		V_{CC} = 2.7 V to 3.6 V,	I_{OH} = –100 µA	V_{CC} – 0.3			V_{CC} – 0.3			V
		V_{CC} = 2.7 V,	I_{OH} = –8 mA	2.4			2.4			
		V_{CC} = 3 V	I_{OH} = –24 mA	2						
			I_{OH} = –32 mA				2			
V_{OL}		V_{CC} = 2.7 V	I_{OL} = 100 µA			0.2			0.2	V
			I_{OL} = 24 mA			0.5			0.5	
		V_{CC} = 2.7 V	I_{OL} = 16 mA			0.4			0.4	
			I_{OL} = 32 mA			0.5			0.5	
			I_{OL} = 48 mA			0.55				
			I_{OL} = 64 mA						0.55	
I_I		V_{CC} = 0 or 3.6 V,	V_I = 5.5 V			10			10	µA
	PTCK	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1			±1	
I_{IH}	PTDI, PTMS, $\overline{PTRST}$, PX	V_{CC} = 3.6 V	V_I = V_{CC}			1			1	µA
	$A_{9–0}$, $P_{2–0}$, $\overline{BYP_{5–0}}$, $STDI_{2–0}$, $SX_{2–1}$, CTDI, $\overline{OE}$					1			1	
I_{IL}	PTDI, PTMS, $\overline{PTRST}$, PX	V_{CC} = 3.6 V,	V_I = GND	–8		–30	–8		–30	µA
	$A_{9–0}$, $P_{2–0}$, $\overline{BYP_{5–0}}$, $STDI_{2–0}$, $SX_{2–1}$, CTDI, $\overline{OE}$			–25		–100	–25		–100	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 4.5 V						±100	µA
I_{OZH}	PTDO, $STDO_{2–0}$, $STMS_{2–0}$, $STCK_{2–0}$, $STRST_{2–0}$, PY, $SY_{2–0}$	V_{CC} = 3.6 V,	V_O = 3 V			5			5	µA
I_{OZL}	PTDO, $STDO_{2–0}$, $STMS_{2–0}$, $STCK_{2–0}$, $STRST_{2–0}$, PY, $SY_{2–0}$	V_{CC} = 3.6 V,	V_O = 0.5 V			–5			–5	µA
I_{OZPU}		V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V,				±100(3)		±100	µA
I_{OZPD}		V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 3 V				±100(3)		±100	µA

(1) Product Preview
(2) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(3) On products compliant to MIL-PRF-38535, this parameter is not production tested.

Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT8986(1)			SN74LVT8986			UNIT
			MIN	TYP(2)	MAX	MIN	TYP(2)	MAX	
I_{CC}	V_{CC} = 3.6 V, $V_I = V_{CC}$ or GND, I_O = 0	OFF, STCK2–0 = H, STMS2–0 = H			2			2	mA
		ON, PTDO = L, STCK2–0= L, STDO2–0 = L, STMS2–0 = L			25			25	
		ON, PTDO = H, STCK2–0 = H, STDO2–0 = H, STMS2–0 = H			7			7	
		$\overline{STRST2}$–0, STCK2–0 = L			10			10	
ΔI_{CC}(4)	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND				0.2			0.2	mA
C_i	V_I = 3 V or 0			7.5			7.5		pF
C_o	V_O = 3 V or 0			8.5			8.5		pF

(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND

Timing Requirements

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 24)

			SN54LVT8986(1)		SN74LVT8986		UNIT
			MIN	MAX	MIN	MAX	
f_{clock1}	Clock frequency, LASP not cascaded	PTCK		40		40	MHz
f_{clock2}	Clock frequency, LASP cascaded			33		33	
t_{w1}	Pulse duration, LASP not cascaded	PTCK high	15		15		ns
		PTCK low	10		10		
t_{w2}	Pulse duration, LASP cascaded	PTCK high	15		15		
		PTCK low	15		15		
t_{w3}	Pulse duration	$\overline{PTRST}$ low	9		9		
t_{su}	Setup time	A_9–A_0 and P_2–P_0 before PTCK↓(2)	10.2		8		ns
		$STDI_0$–$STDI_2$, PTDI before PTCK↑	10.1		10		
		CTDI before PTCK↑	2		2		
		PTMS before PTCK↑	10		10		
		$\overline{BYP_5}$ before PTCK↑			8		
		$\overline{BYP_4}$, $\overline{BYP_2}$–$\overline{BYP_0}$ before PTCK↓			8		
t_h	Hold time	A_9–A_0 and P_2–P_0 after PTCK↓(2)	4		4		ns
		CTDI, $STDI_0$–$STDI_2$, PTDI after PTCK↑	4		4		
		PTMS after PTCK↑	4		4		
		$\overline{BYP_5}$ after PTCK↑	4		4		
		$\overline{BYP_4}$, $\overline{BYP_2}$–$\overline{BYP_0}$ after PTCK↓	4		4		

(1) Product Preview
(2) These requirements apply only in the case in which the address inputs are changed during a linking shadow protocol. For normal application of the LASP, it is recommended that the address and position inputs remain static throughout any shadow protocols. In such cases, the timing of address and position inputs relative to PTCK need not be considered.

Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 24)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT8986(1)				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	
t_{pd}	$\overline{BYP_5}$–$\overline{BYP_0}$	$\overline{CON_2}$–$\overline{CON_0}$		13.5		14.5	ns
	$\overline{BYP_5}$–$\overline{BYP_0}$↓	$STMS_2$–$STMS_0$		16.5		18	
	PTCK	$STCK_2$–$STCK_0$		9.5		10.5	
	PTCK↓	$\overline{CON_2}$–$\overline{CON_0}$		15		17.5	
	PTCK↓ (linking shadow protocol acknowledge)	PTDO		12		14.5	
t_{pd}(2)	PTCK↓ (connect)	$STMS_2$–$STMS_0$		17		21	ns
t_{pd}	PTCK↓	$STDO_2$–$STDO_0$		13.5		16	ns
	PTMS	$STMS_2$–$STMS_0$		13		14	
	$\overline{PTRST}$	$\overline{STRST_2}$–$\overline{STRST_0}$		11		12	
t_{PLH}	$\overline{PTRST}$↓	$\overline{CON_2}$–$\overline{CON_0}$		19.5		21.5	ns
		$STMS_2$–$STMS_0$		17.5		18.5	
t_{pd}	PTCK↓	PTDO, CTDO		12		14.5	ns
	PX	SY_2–SY_0		8		9	
	SX_2–SX_0	PY		9		10	
t_{en}(3)	$\overline{BYP_5}$–$\overline{BYP_0}$↓	PTDO, $STDO_2$–$STDO_0$		13		15	ns
t_{dis}	$\overline{BYP_5}$–$\overline{BYP_0}$↓	PY, SY_2–SY_0		16		18	ns
t_{en}(3)	$\overline{OE}$↓	$STDO_2$–$STDO_0$		14		15	ns
t_{en}	$\overline{OE}$↓	SY_2–SY_0		14		15	ns
t_{PZH}(3)	PTCK↓	PTDO, $STDO_2$–$STDO_0$		17		18	ns
t_{dis}(3)	$\overline{BYP_5}$–$\overline{BYP_0}$↓	PTDO, $STDO_2$–$STDO_0$		11		12	ns
t_{dis}	$\overline{BYP_5}$–$\overline{BYP_0}$↓	PY, SY_2–SY_0		11		12	ns
t_{dis}(3)	$\overline{OE}$↑	$STDO_2$–$STDO_0$		10		11	ns
t_{dis}	$\overline{OE}$↑	SY_2–SY_0		10		11	ns
t_{dis}(3)	PTCK↓	PTDO, $STDO_2$–$STDO_0$		15		17	ns
t_{dis}	PTCK↓	PY, SY_2–SY_0		17		19	ns
t_{dis}(3)	$\overline{PTRST}$↓	PTDO, $STDO_2$–$STDO_0$		18		20	ns
t_{dis}	$\overline{PTRST}$↓	PY, SY_2–SY_0		21.5		23.5	ns

(1) Product Preview
(2) The transitions at $STMS_x$ are possible only when a linking shadow protocol select is issued while $STMS_x$ is held (in the OFF status) at a level that differs from that at PTMS. Such operation is not recommended because state synchronization of the primary TAP to secondary TAP cannot be ensured.
(3) In most applications, the node to which PTDO and $STDO_2$–$STDO_0$ are connected has a pullup resistor. In such cases, this parameter is not significant.

Switching Characteristics

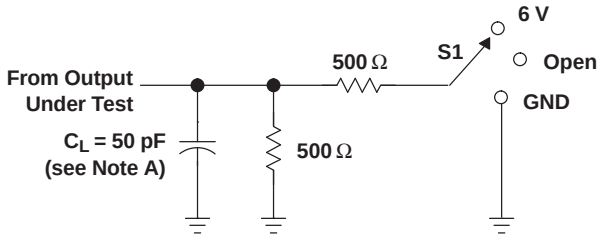
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 24)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVT8986				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	
t_{pd}	$\overline{BYP_5}$–$\overline{BYP_0}$	$\overline{CON_2}$–$\overline{CON_0}$		13.5		14.5	ns
	$\overline{BYP_5}$–$\overline{BYP_0}$↓	$STMS_2$–$STMS_0$		16.5		18	
	PTCK	$STCK_2$–$STCK_0$		9.5		10.5	
	PTCK↓	$\overline{CON_2}$–$\overline{CON_0}$		15		17.5	
	PTCK↓ (linking shadow protocol acknowledge)	PTDO		12		14.5	
t_{pd}(1)	PTCK↓ (connect)	$STMS_2$–$STMS_0$		17		21	ns
t_{pd}	PTCK↓	$STDO_2$–$STDO_0$		13.5		16	ns
	PTMS	$STMS_2$–$STMS_0$		13		14	
	$\overline{PTRST}$	$\overline{STRST_2}$–$\overline{STRST_0}$		11		12	
t_{PLH}	$\overline{PTRST}$↓	$\overline{CON_2}$–$\overline{CON_0}$		19.5		21.5	ns
		$STMS_2$–$STMS_0$		17.5		18.5	
t_{pd}	PTCK↓	PTDO, CTDO		12		14.5	ns
	PX	SY_2–SY_0		8		9	
	SX_2–SX_0	PY		9		10	
t_{en}(2)	$\overline{BYP_5}$–$\overline{BYP_0}$↓	PTDO, $STDO_2$–$STDO_0$		13		15	ns
t_{dis}	$\overline{BYP_5}$–$\overline{BYP_0}$↓	PY, SY_2–SY_0		16		18	ns
t_{en}(2)	$\overline{OE}$↓	$STDO_2$–$STDO_0$		14		15	ns
t_{en}	$\overline{OE}$↓	SY_2–SY_0		14		15	ns
t_{PZH}(2)	PTCK↓	PTDO, $STDO_2$–$STDO_0$		17		18	ns
t_{dis}(2)	$\overline{BYP_5}$–$\overline{BYP_0}$↓	PTDO, $STDO_2$–$STDO_0$		11		12	ns
t_{dis}	$\overline{BYP_5}$–$\overline{BYP_0}$↓	PY, SY_2–SY_0		11		12	ns
t_{dis}(2)	$\overline{OE}$↑	$STDO_2$–$STDO_0$		10		11	ns
t_{dis}	$\overline{OE}$↑	SY_2–SY_0		10		11	ns
t_{dis}(2)	PTCK↓	PTDO, $STDO_2$–$STDO_0$		15		17	ns
t_{dis}	PTCK↓	PY, SY_2–SY_0		17		19	ns
t_{dis}(2)	$\overline{PTRST}$↓	PTDO, $STDO_2$–$STDO_0$		18		20	ns
t_{dis}	$\overline{PTRST}$↓	PY, SY_2–SY_0		21.5		23.5	ns

(1) The transitions at $STMS_x$ are possible only when a linking shadow protocol select is issued while $STMS_x$ is held (in the OFF status) at a level that differs from that at PTMS. Such operation is not recommended because state synchronization of the primary TAP to secondary TAP cannot be ensured.

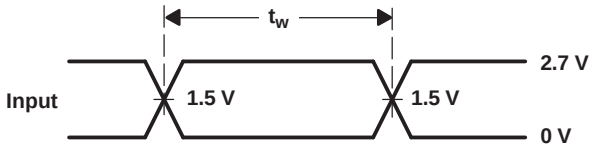
(2) In most applications, the node to which PTDO and $STDO_2$–$STDO_0$ are connected has a pullup resistor. In such cases, this parameter is not significant.

PARAMETER MEASUREMENT INFORMATION

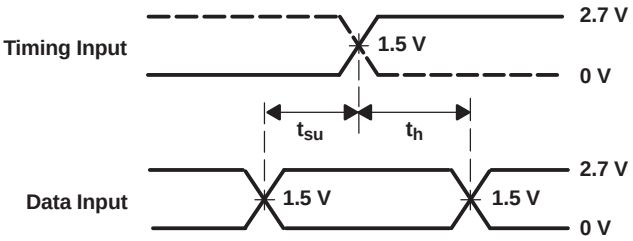


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

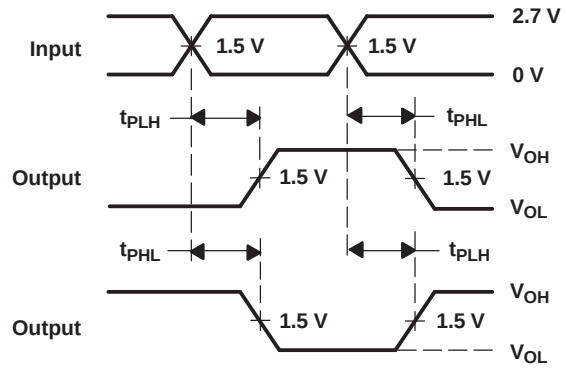
LOAD CIRCUIT



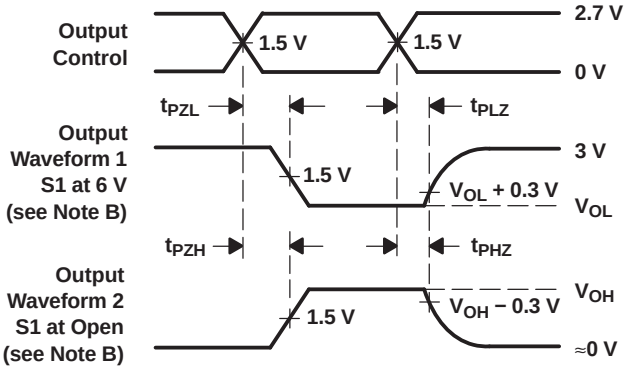
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.

Figure 24. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVT8986PM	Active	Production	LQFP (PM) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	LVT8986
SN74LVT8986PMG4	Active	Production	LQFP (PM) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	LVT8986

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

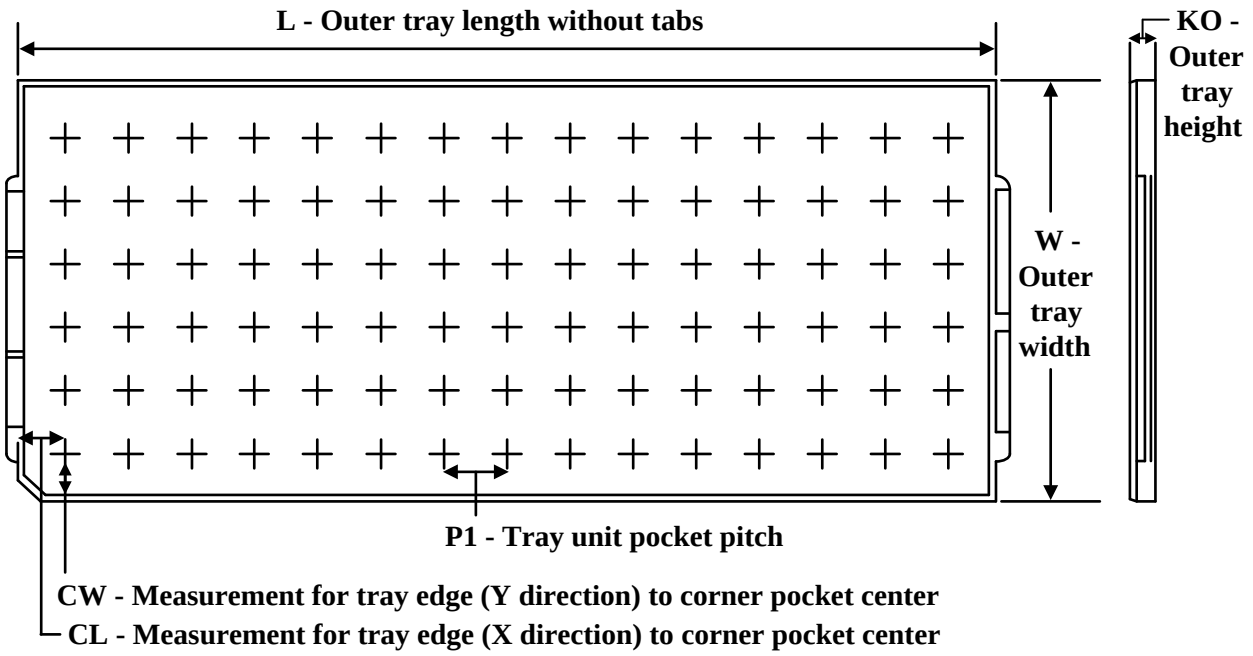
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

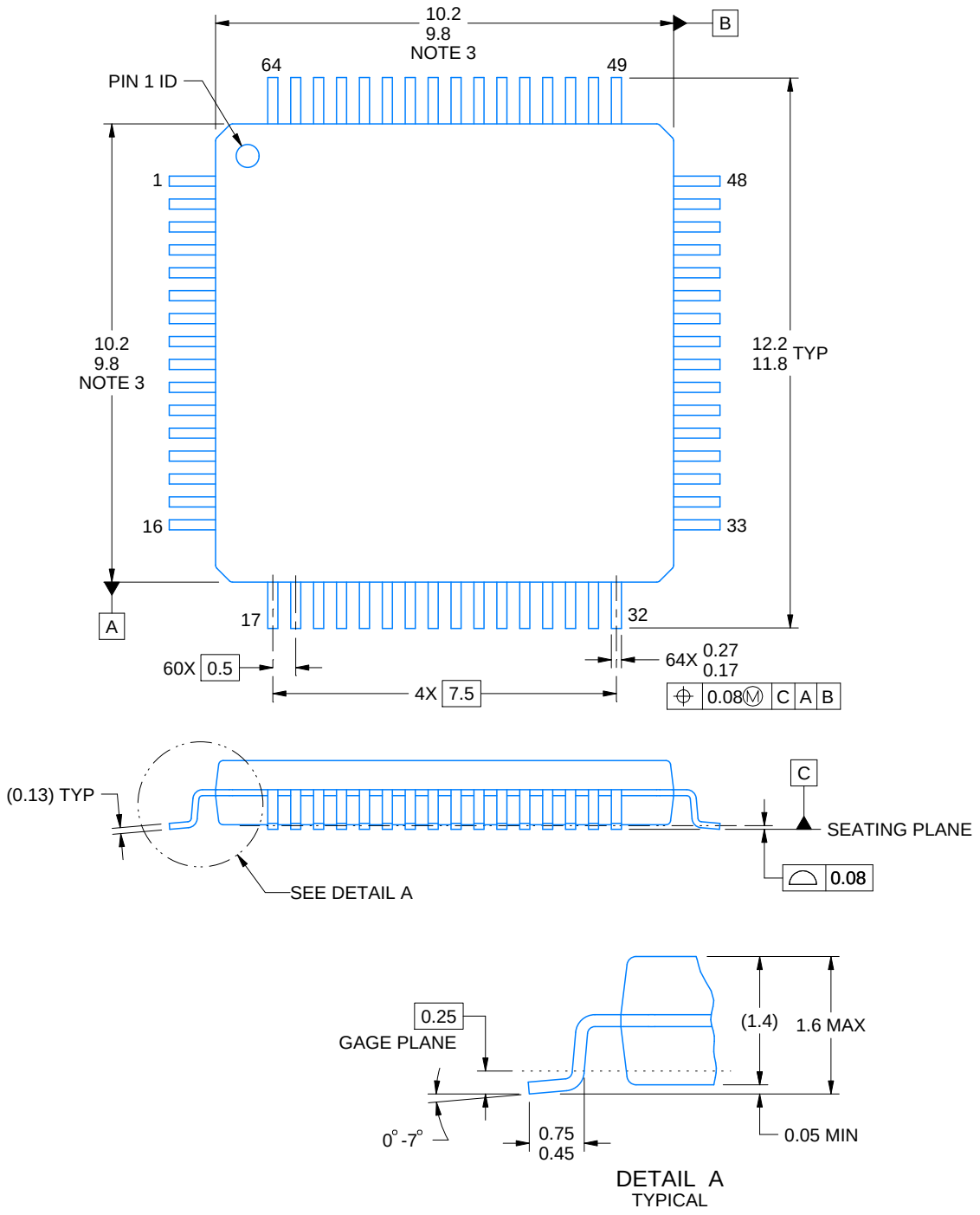
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
SN74LVT8986PM	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13
SN74LVT8986PMG4	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13

PACKAGE OUTLINE

PM0064A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



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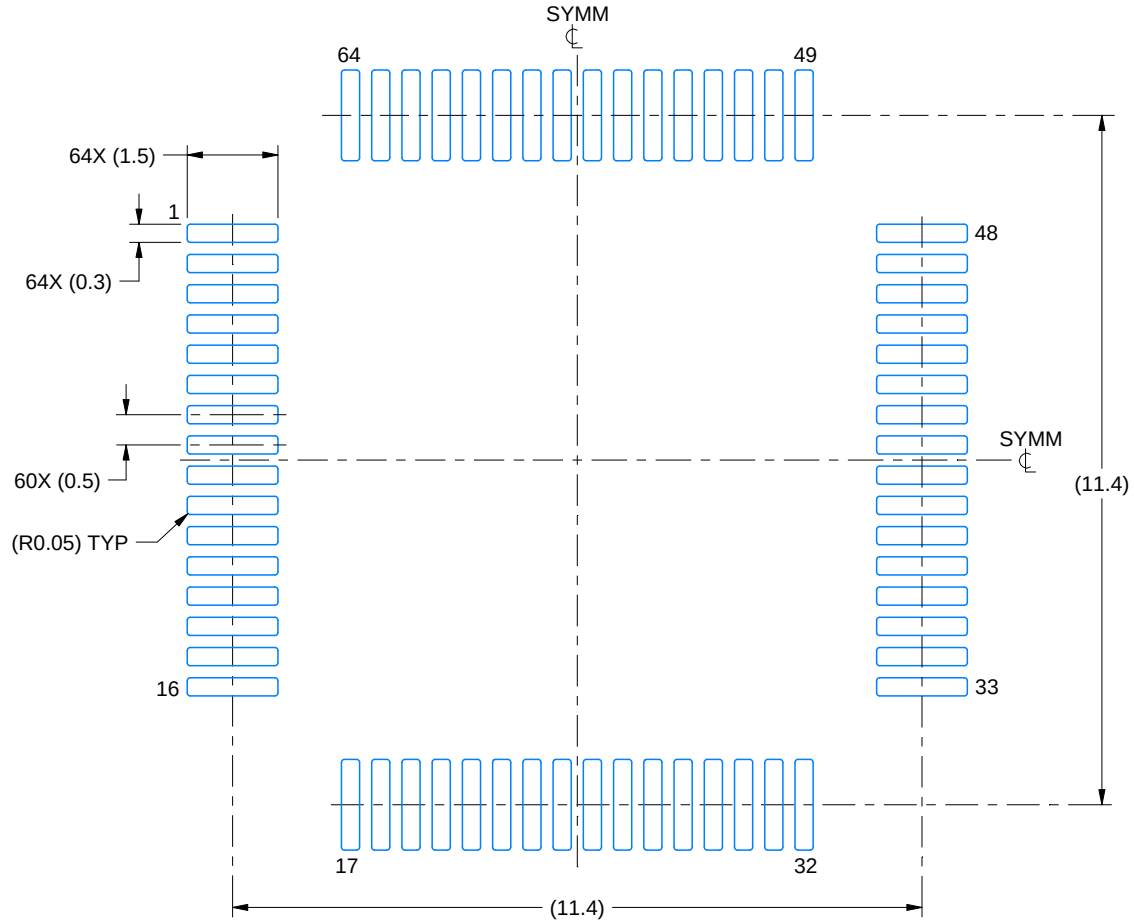
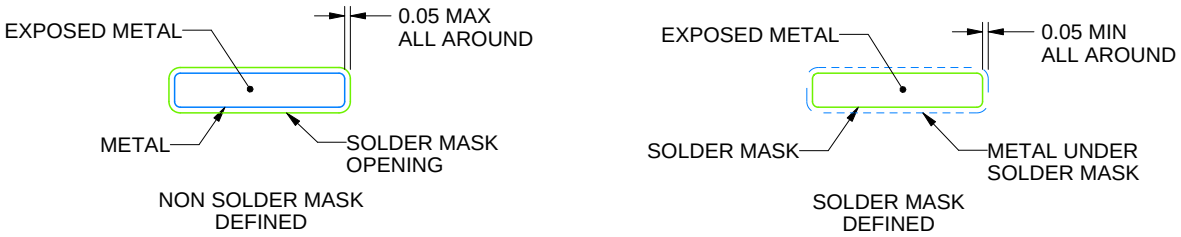
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

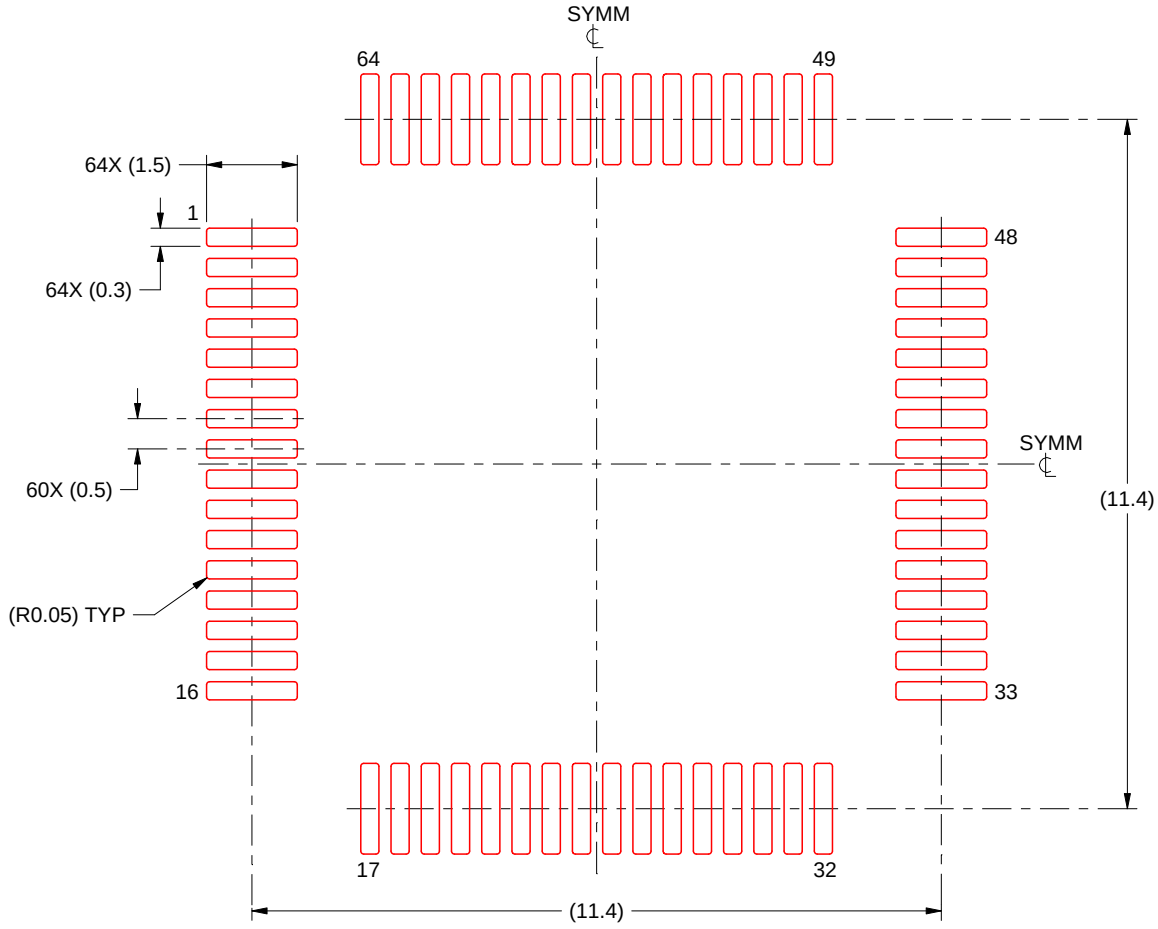


SOLDER MASK DETAILS

4215162/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4215162/A 03/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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