TEXAS INSTRUMENTS

SN74CB3Q3305
SCDS141D – OCTOBER 2003 – REVISED SEPTEMBER 2021

SN74CB3Q3305 Dual FET Bus Switch
2.5-V or 3.3-V Low-Voltage High-Bandwidth Bus Switch

1 Features

- High-bandwidth data path (up to 500 MHz)[1]
- 5-V tolerant I/Os with device powered up or powered down
- Low and flat ON-state resistance (r_{on}) characteristics over operating range (r_{on} = 3 Ω typical)
- Supports input voltage beyond supply on data I/O ports
    - 0 to 5 V switching with 3.3 V V_{CC}
    - 0 to 3.3 V switching with 2.5 V V_{CC}
- Bidirectional data flow with near-zero propagation delay
- Low input or output capacitance minimizes loading and signal distortion ($C_{io(OFF)}$ = 3.5 pF typical)
- Fast switching frequency (f_{OE} = 20 MHz maximum)
- Data and control inputs provide undershoot clamp diodes
- Low power consumption (I_{CC} = 0.25 mA typical)
- V_{CC} operating range from 2.3 V to 3.6 V
- Data I/Os support 0 to 5 V signaling levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, and 5 V)
- Control inputs can be driven by TTL or 5 V/3.3 V CMOS outputs
- I_{off} supports partial-power-down mode operation
- Latch-up performance exceeds 100 mA per JESD 78, Class II

2 Applications

- IP phones: wired and wireless
- Optical modules
- Optical networking: video over fiber and EPON
- Private branch exchange (PBX)
- WiMAX and wireless infrastructure equipment
- USB, differential signal interface
- Bus isolation

3 Description

The SN74CB3Q3305 device is a high-bandwidth FET bus switch using a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports switching input voltage beyond the supply on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3305 device provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74CB3Q3305	VSSOP (8)	2.00 mm × 3.10 mm
	TSSOP (8)	3.00 mm × 6.10 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
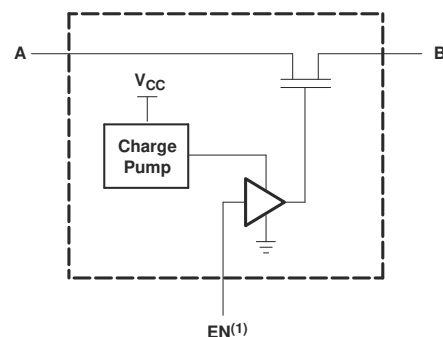
(1) EN is the internal enable signal applied to the switch.

Simplified Schematic, Each FET Switch (SW)

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[1] For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, *CBT-C, CB3T, and CB3Q Signal-Switch Families*, SCDA008.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

5 Pin Configuration and Functions
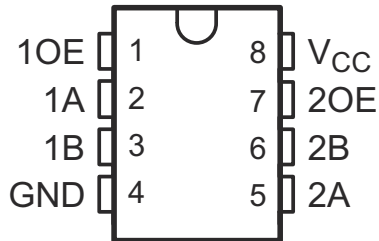
**Figure 5-1. PW Package
8-Pin TSSOP
Top View**
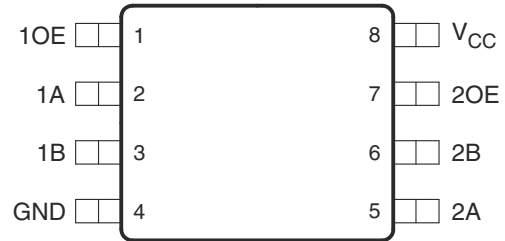
**Figure 5-2. DCU Package
8-Pin VSSOP
Top View**

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
1A	2	I/O	Channel 1 A port
1B	3	I/O	Channel 1 B port
1OE	1	I	Output Enable for switch 1
2A	5	I/O	Channel 2 A port
2B	6	I/O	Channel 2 B port
2OE	7	I	Output Enable for switch 2
GND	4	P	Ground
V_{CC}	8	P	Power supply

(1)   I = input, O = output, I/O = input and output, P = power

Product Folder Links: *SN74CB3Q3305*

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		−0.5	4.6	V
V_{IN}	Control input voltage[2] [3]		−0.5	7	V
$V_{I/O}$	Switch I/O voltage[2] [3] [4]		−0.5	7	V
I_{IK}	Control input clamp current	$V_{IN} < 0$		−50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O} < 0$		−50	mA
$I_{I/O}$	ON-state switch current[5]			±64	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance[6]			88	°C/W
T_j	Junction temperature			150	°C
T_{stg}	Storage temperature		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		−40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information

THERMAL METRIC[1]		SN74CB3Q3305 DCU (VSSOP) 8 PINS	SN74CB3Q3305 PW (TSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	183	190.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	64.2	74.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62.5	119.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.3	120.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.1	117.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS			MIN	TYP[2]	MAX	UNIT
V_{IK}		V_{CC} = 3.6 V,	I_I = −18 mA				−1.8	V
I_{IN}	Control inputs	V_{CC} = 3.6 V,	V_{IN} = 0 to 5.5 V				±1	µA
I_{OZ} [3]		V_{CC} = 3.6 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±1	µA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			1	µA
I_{CC}		V_{CC} = 3.6 V,	$I_{I/O}$ = 0, Switch ON or OFF,	V_{IN} = V_{CC} or GND		0.25	0.7	mA
ΔI_{CC} [4]	Control inputs	V_{CC} = 3.6 V, One input at 3 V, Other inputs at V_{CC} or GND					25	µA
I_{CCD} [5]	Per control input	V_{CC} = 3.6 V, A and B ports open, Control input switching at 50% duty cycle				0.040	0.045	mA/ MHz
C_{in}	Control inputs	V_{CC} = 3.3 V,	V_{IN} = 5.5 V, 3.3 V, or 0			2.5	3.5	pF
$C_{io(OFF)}$		V_{CC} = 3.3 V,	Switch OFF, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0		3.5	5	pF
$C_{io(ON)}$		V_{CC} = 3.3 V,	Switch ON, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0		8	10.5	pF
r_{on} [6]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0, I_O = 30 mA			3	8	Ω
			V_I = 1.7 V, I_O = −15 mA			3.5	9	
		V_{CC} = 3 V	V_I = 0, I_O = 30 mA			3	6	
			V_I = 2.4 V, I_O = −15 mA			3.5	8	

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
(2) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
(5) This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 9-2).
(6) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V$_{CC}$	MIN	MAX	UNIT
f$_{OE}$ [1]	OE	A or B	V$_{CC}$ = 2.5 V ± 0.2 V		10	MHz
			V$_{CC}$ = 3.3 V ± 0.3 V		20	
t$_{pd}$ [2]	A or B	B or A	V$_{CC}$ = 2.5 V ± 0.2 V		0.09	ns
			V$_{CC}$ = 3.3 V ± 0.3 V		0.15	
t$_{en}$	OE	A or B	V$_{CC}$ = 2.5 V ± 0.2 V	1	5	ns
			V$_{CC}$ = 3.3 V ± 0.3 V	1	4.5	
t$_{dis}$	OE	A or B	V$_{CC}$ = 2.5 V ± 0.2 V	1	4.5	ns
			V$_{CC}$ = 3.3 V ± 0.3 V	1	5	

(1) Maximum switching frequency for control input (V$_O$ > V$_{CC}$, V$_I$ = 5 V, R$_L$ ≥ 1 MΩ, C$_L$ = 0).
(2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
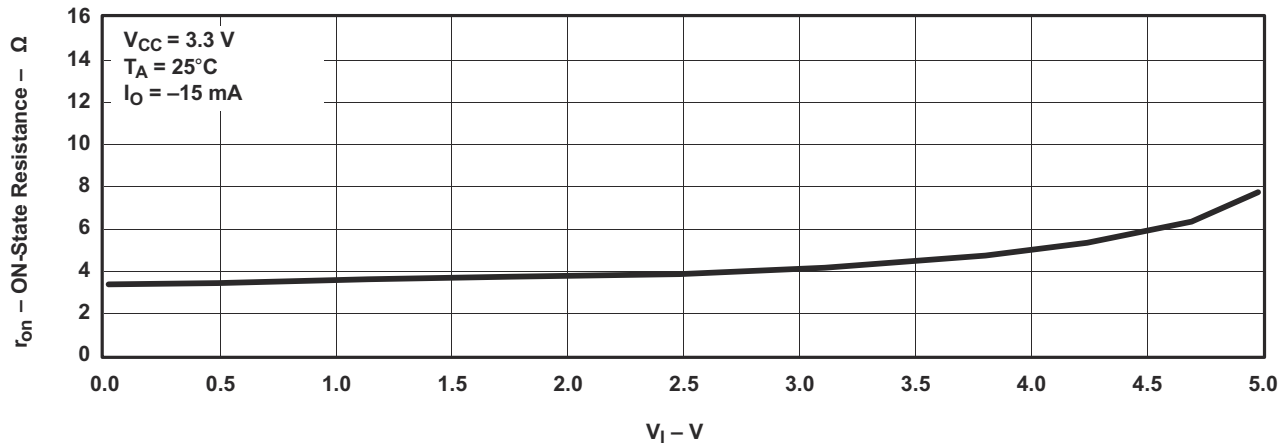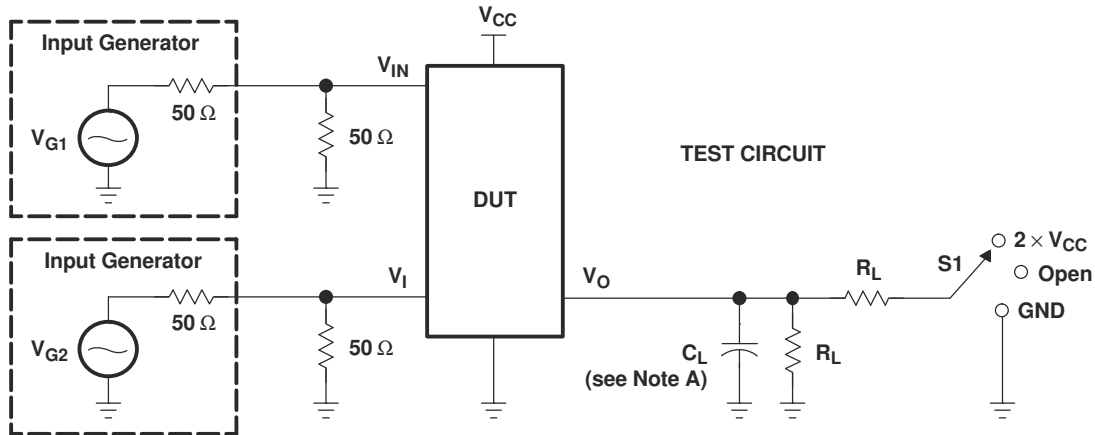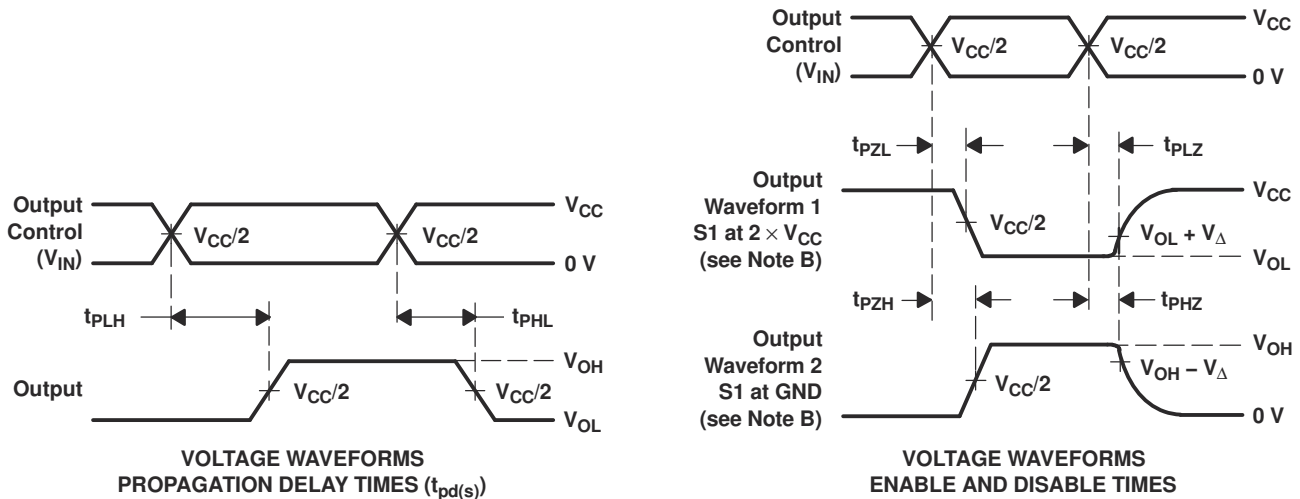
6.7 Typical Characteristics

Figure 6-1. Typical r$_{on}$ vs V$_I$

Product Folder Links: *SN74CB3Q3305*

7 Parameter Measurement Information

TEST CIRCUIT

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V $\pm$ 0.2 V	Open	500 Ω	V_{CC} or GND	30 pF	
	3.3 V $\pm$ 0.3 V	Open	500 Ω	V_{CC} or GND	50 pF	
t_{PLZ}/t_{PZL}	2.5 V $\pm$ 0.2 V	2 $\times$ V_{CC}	500 Ω	GND	30 pF	0.15 V
	3.3 V $\pm$ 0.3 V	2 $\times$ V_{CC}	500 Ω	GND	50 pF	0.3 V
t_{PHZ}/t_{PZH}	2.5 V $\pm$ 0.2 V	GND	500 Ω	V_{CC}	30 pF	0.15 V
	3.3 V $\pm$ 0.3 V	GND	500 Ω	V_{CC}	50 pF	0.3 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, Z_O = 50 Ω, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

Figure 7-1. Test Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74CB3Q3305 device is organized as two 1-bit switches with separate output-enable (1OE and 2OE) inputs. It can be used as two 1-bit bus switches or as one 2-bit bus switch. When OE is high, the associated 1-bit bus switch is ON and the A port is connected to the B port, allowing bidirectional data flow between ports. When OE is low, the associated 1-bit bus switch is OFF and a high-impedance state exists between the A and B ports.
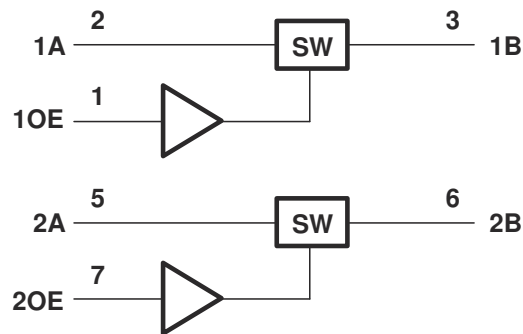
8.2 Functional Block Diagram

Figure 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

The device supports High-Bandwidth data path up to 500 MHz. The I/O ports are 5 V tolerant when powered up or powered down due to I_{OFF}. The charge pump creates low and flat ON-state resistance characteristics over the whole operating temperature range.

Switching input voltage beyond the supply is supported on data I/O ports: 0 V to 5 V with 3.3 V V_{CC} or 0 V to 3.3 V with 2.5 V V_{CC}.

The data flow is bidirectional with near-zero propagation delay. Reduced input/output capacitance for higher speed applications. OE can be toggled at the high speeds of 20 MHz for fast switching applications.

8.4 Device Functional Modes

Table 8-1 lists the functional modes of the SN74CB3Q3305.

Table 8-1. Function Table (Each Bus Switch)

INPUT OE	INPUT/OUTPUT A	FUNCTION
H	B	A port = B port
L	Z	Disconnect

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

Figure 9-1 shows that the SN74CB3Q3305 can be used as bidirectional switch. The controller operates at 5 V and the peripheral can accept 5 V. Even with a V_{CC} of 3 V on the SN74CB3Q3305, the two ports can be connected to pass the 5 V signal. The controller uses the OE pin control the switch. This is a very generic example and could apply to many situations. For applications that require only 1 bit (for example, one channel), tie the unused OE low and tie the unused ports A and B to either high or low (not shown).
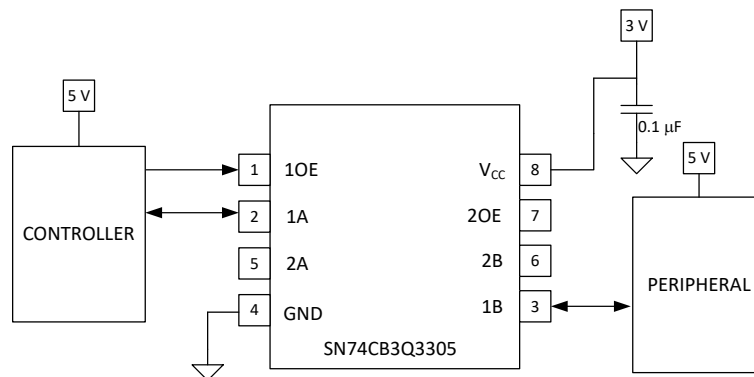
9.2 Typical Application

Figure 9-1. Typical Application of the SN74CB3Q3305

9.2.1 Design Requirements

1. Recommended Input Conditions:
   - For specified high and low levels, see V_{IH} and V_{IL} in Section 6.3.
   - Inputs and outputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
2. Absolute Maximum Conditions:
   - I/O currents should not exceed ±64 mA per channel.
   - Continuos current through GND or V_{CC} should not exceed ±100 mA.
3. Frequency Selection Criterion:
   - Maximum frequency tested is 500 MHz.
   - Added trace resistance/capacitance can reduce maximum frequency capability; use layout practices as directed in Section 11.

9.2.2 Detailed Design Procedure

The 0.1 µF capacitor should be placed as close as possible to the device.
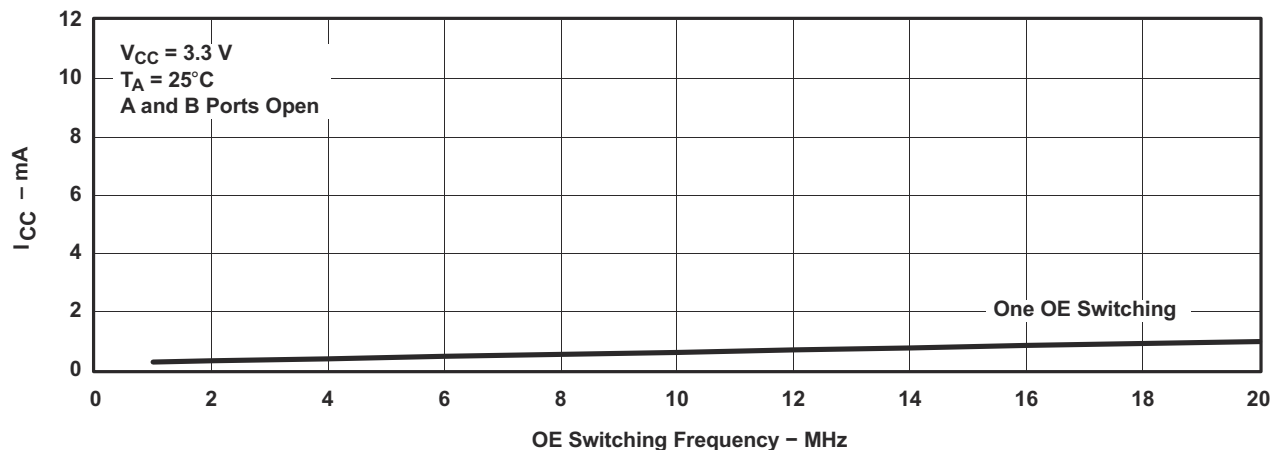
9.2.3 Application Curve

Figure 9-2. Typical I_{CC} vs OE Switching Frequency

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in Section 6.1 table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 µF bypass capacitor is recommended. If multiple pins are labeled V_{CC}, then a 0.01 µF or 0.022 µF capacitor is recommended for each V_{CC} because the V_{CC} pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1 µF bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 11-1 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.
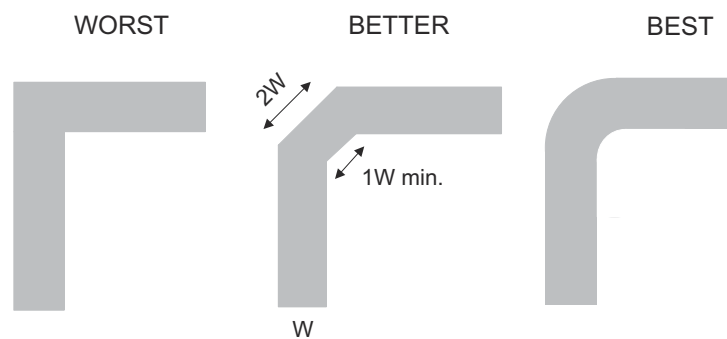
11.2 Layout Example

Figure 11-1. Trace Example

Product Folder Links: *SN74CB3Q3305*

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:
- Texas Instruments, *CBT-C, CB3T, and CB3Q Signal-Switch Families* application report
- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application report
- Texas Instruments, *Selecting the Right Texas Instruments Signal Switch* application report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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Product Folder Links: *SN74CB3Q3305*

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74CB3Q3305DCURG4	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GARR	Samples
SN74CB3Q3305DCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(GARQ, GARR)	Samples
SN74CB3Q3305PW	LIFEBUY	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU305	
SN74CB3Q3305PWG4	LIFEBUY	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU305	
SN74CB3Q3305PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	BU305	Samples
SN74CB3Q3305PWRE4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU305	Samples
SN74CB3Q3305PWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU305	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74CB3Q3305DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74CB3Q3305DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74CB3Q3305PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
SN74CB3Q3305PWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74CB3Q3305DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74CB3Q3305DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
SN74CB3Q3305PWR	TSSOP	PW	8	2000	367.0	367.0	35.0
SN74CB3Q3305PWRG4	TSSOP	PW	8	2000	367.0	367.0	35.0

PACKAGE MATERIALS INFORMATION

TUBE

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74CB3Q3305PW	PW	TSSOP	8	150	530	10.2	3600	3.5
SN74CB3Q3305PWG4	PW	TSSOP	8	150	530	10.2	3600	3.5

A

3.2
3.0 TYP

PIN 1 INDEX AREA

1

8

6X $\boxed{0.5}$

2X

$\boxed{1.5}$

2.1
1.9
NOTE 3

4

5

B

2.4
2.2
NOTE 3

8X $\begin{array}{c} 0.25 \\ 0.17 \end{array}$

$\boxed{\oplus \mid 0.08\text{\scriptsize M} \mid C \mid A \mid B}$

C

$\boxed{\bigcirc \mid 0.1 \mid C}$

SEATING
PLANE

SEE DETAIL A

(0.13) TYP

$\boxed{0.12}$
GAGE PLANE

0°-6°

0.35
0.20

0.9
0.6

0.1
0.0

DETAIL A
TYPICAL

4225266/A   09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.

8X (0.85)

SYMM

SEE SOLDER MASK
DETAILS

(R0.05) TYP

8X (0.3)   1

8

SYMM

6X (0.5)

4

5

(3.1)
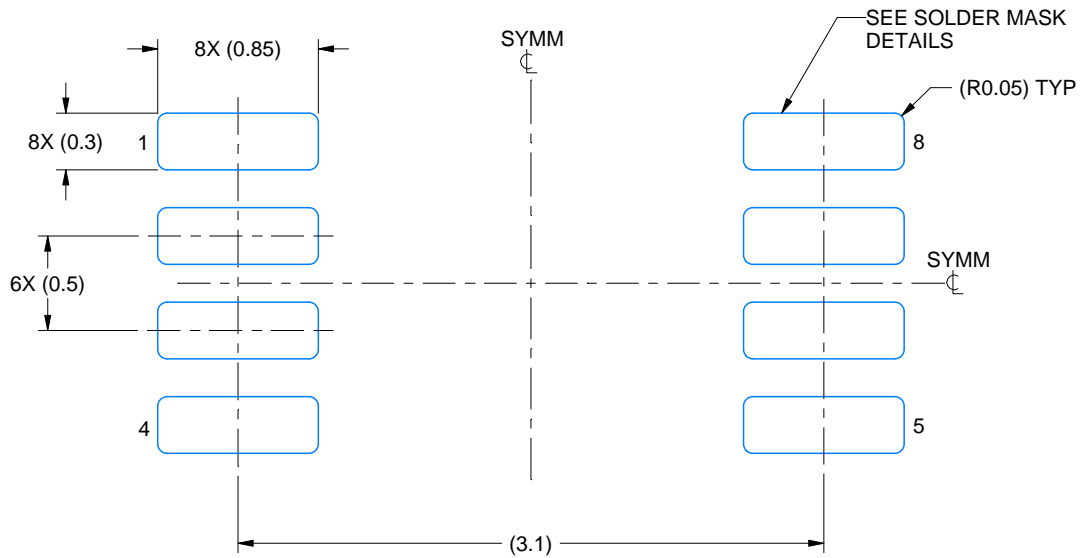
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

0.05 MIN
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4225266/A   09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

8X (0.85)

SYMM

(R0.05) TYP

8X (0.3) 1

8

SYMM

6X (0.5)

4

5

(3.1)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A   09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
8. Board assembly site may have different recommendations for stencil design.

6.6
6.2 TYP

A

PIN 1 ID
AREA

1

3.1
2.9
NOTE 3

4

B

4.5
4.3
NOTE 4

8

6X 0.65

2X

1.95

5

8X 0.30
0.19

⊕ 0.1 Ⓜ C AⓈ BⓈ

C

SEATING PLANE

⌒ 0.1 C

1.2 MAX

SEE DETAIL A

(0.15) TYP

0.25
GAGE PLANE

0° - 8°

0.75
0.50

0.15
0.05

DETAIL A
TYPICAL

4221848/A   02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

8X (0.45)

8X (1.5)

SYMM

(R0.05)
TYP

1

8

SYMM

6X (0.65)

4

5

(5.8)

LAND PATTERN EXAMPLE
SCALE:10X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.05 MAX
ALL AROUND

0.05 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4221848/A   02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A   02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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