SN74GTL2003 8-Bit Bidirectional Low-Voltage Translator

1 Features

- Provides bidirectional voltage translation with no direction control required
- Allows voltage level translation from 0.95 V up to 5 V
- Provides direct interface with GTL, GTL+, LVTTL/TTL, and 5-V CMOS levels
- Supports 50 MHz up or down translation at ≦20 pF capacitive load
- Low ON-state resistance between input and output pins (Sn/Dn)
- Supports hot insertion
- No power supply required – will not latch up
- 5-V-tolerant inputs
- Low standby current
- Flow-through pinout for ease of printed circuit board trace routing

2 Applications

- Bidirectional or unidirectional applications requiring voltage-level translation from any voltage (0.95 V to 5 V) to any voltage (0.95 V to 5 V)
- Low voltage processor I^2C port translation to 3.3-V or 5-V I^2C bus signal levels
- GTL/GTL+ translation to LVTTL/TTL signal levels
- HPC server
- Dialysis machines
- Service router
- Servers

3 Description

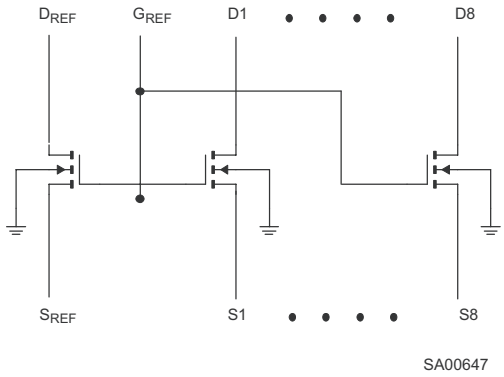
The SN74GTL2003 device provides eight NMOS pass transistors (Sn and Dn) with a common gate (G_{REF}) and a reference transistor (S_{REF} and D_{REF}). The low ON-state resistance of the switch allows connections to be made with minimal propagation delay. With no direction control pin required, the device allows bidirectional voltage translations any voltage (0.95 V to 5 V) to any voltage (0.95 V to 5 V).

All transistors in the SN74GTL2003 have the same electrical characteristics, and there is minimal deviation from one output to another in voltage or propagation delay. This offers superior matching over discrete transistor voltage-translation solutions where the fabrication of the transistors is not symmetrical. With all transistors being identical, the reference transistor (S_{REF}/D_{REF}) can be located on any of the other eight matched Sn/Dn transistors, allowing for easier board layout. The translator transistors with integrated ESD circuitry provides excellent ESD protection.

Package Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74GTL2003	PW (TSSOP, 20)	6.50 mm × 4.40 mm
	RKS (VQFN, 20)	4.50 mm × 2.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Clamp Schematic

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (September 2016) to Revision D (September 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated definition of the switching characteristics table	5

Changes from Revision B (June 2015) to Revision C (September 2016)	Page
• Updated *Features*	1
• Updated pinout images to new format	3
• Added *Receiving Notification of Documentation Updates* section	17

Changes from Revision A (March 2013) to Revision B (June 2015)	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions

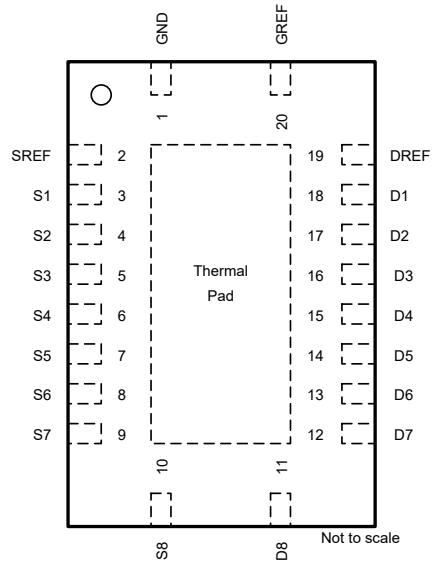


Figure 5-1. RKS Package, 20-Pin VQFN (Top View)

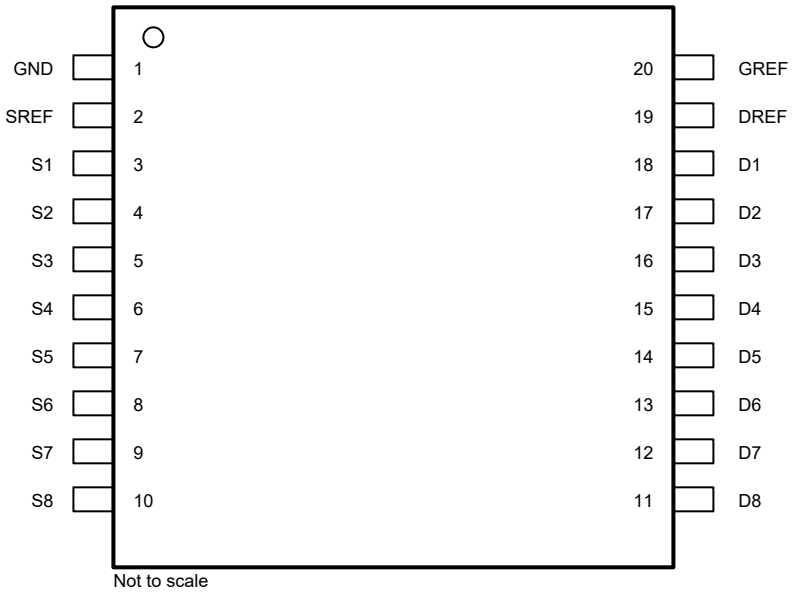


Figure 5-2. PW Package, 20-Pin TSSOP (Top View)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
D1	18	I/O	GTL drain port
D2	17	I/O	GTL drain port
D3	16	I/O	GTL drain port
D4	15	I/O	GTL drain port
D5	14	I/O	GTL drain port
D6	13	I/O	GTL drain port
D7	12	I/O	GTL drain port
D8	11	I/O	GTL drain port
D_{REF}	19	—	Drain of reference transistor, tie directly to G_{REF} and pull up to reference voltage through a 200-kΩ resistor
GND	1	—	Ground
G_{REF}	20	—	Gate of reference transistor, tie directly to D_{REF} and pull up to reference voltage through a 200-kΩ resistor
S1	3	I/O	LVTTL/TTL source port
S2	4	I/O	LVTTL/TTL source port
S3	5	I/O	LVTTL/TTL source port
S4	6	I/O	LVTTL/TTL source port
S5	7	I/O	LVTTL/TTL source port
S6	8	I/O	LVTTL/TTL source port
S7	9	I/O	LVTTL/TTL source port
S8	10	I/O	LVTTL/TTL source port
S_{REF}	2	—	Source of reference transistor

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{SREF}	DC source reference voltage		–0.5	7	V
V_{DREF}	DC drain reference voltage		–0.5	7	V
V_{GREF}	DC gate reference voltage		–0.5	7	V
V_{Sn}	DC voltage port Sn		–0.5	7	V
V_{Dn}	DC voltage port Dn		–0.5	7	V
I_{REFK}	DC diode current on reference pins	V_I < 0 V		–50	mA
I_{SK}	DC diode current port Sn	V_I < 0V		–50	mA
I_{DK}	DC diode current port Dn	V_I < 0 V		–50	mA
I_{MAX}	DC clamp current per channel	Channel is ON state		±128	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
$V_{I/O}$	Input/output voltage (Sn, Dn)	0	5.5	V
V_{SREF}	DC source reference voltage(1)	0	5.5	V
V_{DREF}	DC drain reference voltage	0	5.5	V
V_{GREF}	DC gate reference voltage	0	5.5	V
I_{PASS}	Pass transistor current		64	mA
T_A	Operating ambient temperature (in free air)	–40	85	°C

(1) V_{SREF} = V_{DREF} – 1.5 V for best results in level-shifting applications.

6.4 Thermal Information

THERMAL METRIC(1)		SN74GTL2003		UNIT
		PW (TSSOP)	RKS (VQFN)	
		20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83	81	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32	36	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]			MIN	TYP[1]	MAX	UNIT
V_{OL}	Low-level output voltage	V_{DD} = 3 V, V_{SREF} = 1.365 V, V_{Sn} or V_{Dn} = 0.175 V, I_{clamp} = 15.2 mA				260	350	mV
V_{IK}	Input clamp voltage	I_I = –18 mA	V_{GREF} = 0 V				–1.2	V
I_{IH}	Gate input leakage	V_I = 5 V	V_{GREF} = 0 V				5	µA
$C_{I(GREF)}$	Gate capacitance	V_I = 3 V or 0 V				56		pF
$C_{IO(OFF)}$	OFF capacitance	V_O = 3 V or 0 V	V_{GREF} = 0 V			7.4		pF
$C_{IO(ON)}$	ON capacitance	V_O = 3 V or 0 V	V_{GREF} = 3 V			18.6		pF
r_{on} [2]	ON-state resistance	V_I = 0 V	V_{GREF} = 4.5 V	I_O = 64 mA		3.5	5	Ω
			V_{GREF} = 3 V			4.4	7	
			V_{GREF} = 2.3 V			5.5	9	
			V_{GREF} = 1.5 V			67	105	
			V_{GREF} = 1.5 V,	I_O = 30 mA		9	15	
		V_I = 2.4 V	V_{GREF} = 4.5 V	I_O = 15 mA		7	10	
			V_{GREF} = 3 V			58	80	
		V_I = 1.7 V	V_{GREF} = 2.3 V			50	70	

(1) All typical values are measured at T_A = 25°C.
(2) Measured by the voltage drop between the Sn and the Dn terminals at the indicated current through the switch. ON-state resistance is determined by the lowest voltage of the two (Sn or Dn) terminals.

6.6 Switching Characteristics

V_{REF} = 1.365 V to 1.635 V, V_{DD1} = 3 V to 3.6 V, V_{DD2} = 2.36 V to 2.64 V, GND = 0 V, $t_r = t_f \leq 3$ ns, T_A = –40°C to +85°C (see Figure 9-1)[1]

PARAMETER		MIN	TYP[2]	MAX	UNIT
t_{PLH} [3]	Propagation delay (Sn to Dn, Dn to Sn)	0.5	1.5	5.5	ns

(1) $C_{ON(max)}$ of 30 pF and a $C_{OFF(max)}$ of 15 pF is specified by design.
(2) All typical values are measured at V_{DD1} = 3.3 V, V_{DD2} = 2.5 V, V_{REF} = 1.5 V and T_A = 25°C.
(3) Propagation delay specified by characterization.

6.7 Switching Characteristics

V_{GREF} = 5 V ± 0.5 V, GND = 0 V, T_A = –40°C to +85°C (see Figure 9-1)

PARAMETER		MIN	TYP	MAX	UNIT
t_{PD}	Propagation delay[1]			250	ps

(1) This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical ON-state resistance of the switch and a load capacitance of 50 pF, when driven by a voltage source with zero output impedance.

6.8 Typical Characteristics

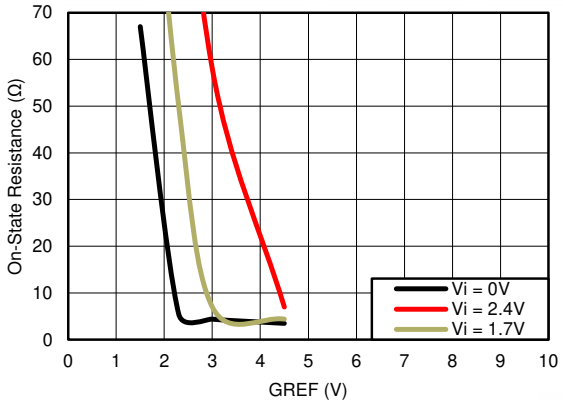


Figure 6-1. ON-Resistance vs G_{REF} Typical Curves

7 Parameter Measurement Information

C_L = Load Capacitance, includes jig and probe capacitance (see *Section 6.5* for value)

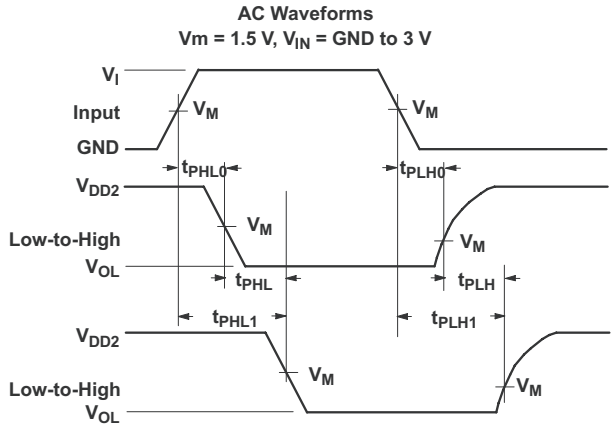


Figure 7-1. Input (Sn) to Output (Dn) Propagation Delays

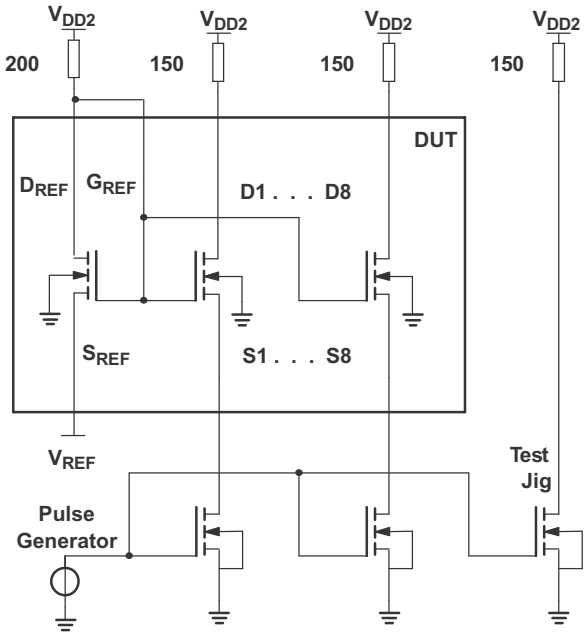


Figure 7-2. Load Circuit

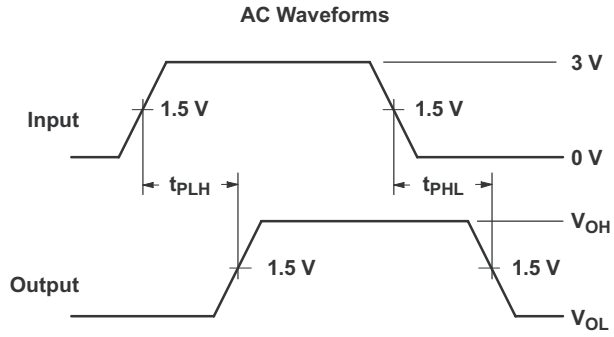


Figure 7-3. Input (Sn) to Output (Dn) Propagation Delays

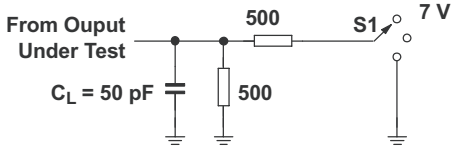


Figure 7-4. Load Circuit

Table 7-1. Test Conditions

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
T_{PHZ}/T_{PZH}	Open

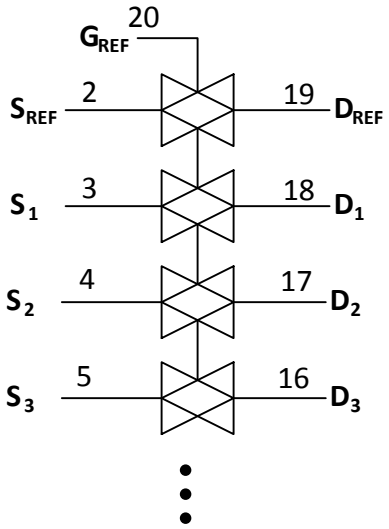
8 Detailed Description

8.1 Overview

The SN74GTL2003 device provides eight NMOS pass transistors (Sn and Dn) with a common gate (G_{REF}) and a reference transistor (S_{REF} and D_{REF}). The low ON-state resistance of the switch allows connections to be made with minimal propagation delay. With no direction control pin required, the device allows bidirectional voltage translations from any voltage (0.95 V to 5 V) to any voltage (0.95 V to 5 V).

When the Sn or Dn port is LOW, the clamp is in the ON state and a low-resistance connection exists between the Sn and Dn ports. Assuming the higher voltage is on the Dn port, when the Dn port is HIGH, the voltage on the Sn port is limited to the voltage set by the reference transistor (S_{REF}). When the Sn port is HIGH, the Dn port is pulled to VCC by the pullup resistors.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Provides Bidirectional Voltage Translation With No Direction Control Required

Because the circuit acts essentially as a pass transistor, no direction pin is needed, as data is allowed to flow both ways.

8.3.2 Flow Through Pinout

Allocated pins for input and output A on right side and input and output B on left side. Reduces the need for multi-layer board layout or long traces through the system.

8.4 Device Functional Modes

Table 8-1. High to Low Translation
(Assuming Dn is at the Higher Voltage Level)

G_{REF} (1)	D_{REF}	S_{REF}	INPUTS D8–D1	OUTPUT S8–S1	TRANSISTOR
H	H	0 V	X	X	Off
H	H	V_{TT} (2)	H	V_{TT} (3)	On
H	H	V_{TT}	L	L(4)	On
L	L	0 – V_{TT}	X	X	Off

(1) G_{REF} should be at least 1.5 V higher than S_{REF} for best translator operation.
(2) V_{TT} is equal to the S_{REF} voltage.
(3) Sn is not pulled up or pulled down.
(4) Sn follows the Dn input LOW.

Table 8-2. Low to High Translation
(Assuming Dn is at the Higher Voltage Level)

GREF(1)	DREF	SREF	INPUTS D8–D1	OUTPUT S8–S1	TRANSISTOR
H	H	0 V	X	X	Off
H	H	V_{TT} (2)	V_{TT}	H(3)	Nearly Off
H	H	V_{TT}	L	L(4)	On
L	L	0 – V_{TT}	X	X	Off

(1) G_{REF} should be at least 1.5 V higher than S_{REF} for best translator operation.
(2) V_{TT} is equal to the S_{REF} voltage.
(3) Dn is pulled up to VCC through an external resistor.
(4) Dn follows the Sn input LOW.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

SN74GTL2003 is a GTL/GTL+ to LVTTL/TTL bidirectional voltage level translator. This device can be used in both unidirectional applications and bidirectional. Please find the reference schematics and recommended values for passive components in *Section 9.2*.

9.2 Typical Applications

9.2.1 Bidirectional Translation

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the G_{REF} input must be connected to D_{REF} and both pins pulled to HIGH-side V_{CC} through a pullup resistor (typically 200 kΩ). TI recommends a filter capacitor on D_{REF}. The processor output can be totem pole or open drain (pullup resistors) and the chipset output can be totem pole or open drain (pullup resistors are required to pull the Dn outputs to V_{CC}). However, if either output is totem pole, data must be unidirectional or the outputs must be 3-statable, and the outputs must be controlled by some direction-control mechanism to prevent HIGH-to-LOW contentions in either direction. If both outputs are open drain, no direction control is needed. The opposite side of the reference transistor (S_{REF}) is connected to the processor core power-supply voltage. When D_{REF} is connected through a 200-kΩ resistor to a 3.3-V to 5.5-V VCC supply and S_{REF} is set from 1 V to V_{CC} 1.5 V, the output of each Sn has a maximum output voltage equal to S_{REF}, and the output of each Dn has a maximum output voltage equal to V_{CC}.

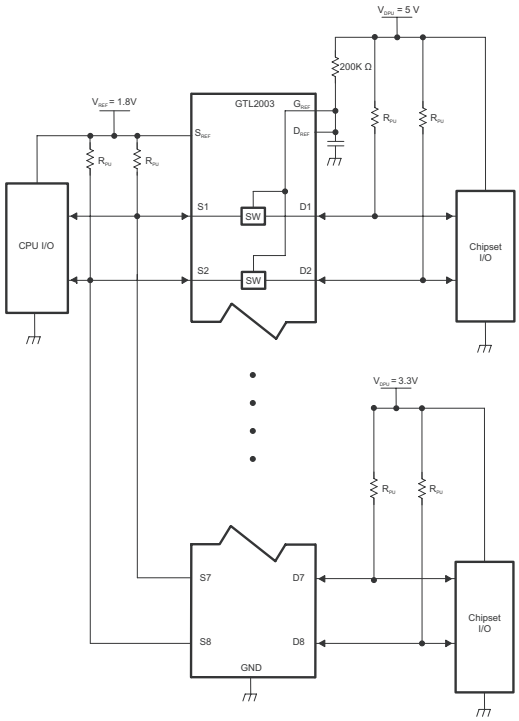


Figure 9-1. Bidirectional Translation to Multiple Higher Voltage Levels (Such as an I²C or SMBus Applications)

9.2.1.1 Design Requirements

- SN74GTL2003 requires industry standard GTL and LVTTL/TTL voltage levels.
- Place pullup resistors of ≅200 kΩ in all inputs/outputs to the GTL/TTL voltage levels.
- Place 0.1-μF bypass capacitors close to the power supply pins to reduce errors coupling in from noisy or high-impedance power supplies.
- Comply to the parameters in *Section 6.3*.

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Sizing Pullup Resistors

The pullup resistor value should limit the current through the pass transistor when it is in the on state to about 15 mA. This ensures a pass voltage of 260 mV to 350 mV. If the current through the pass transistor is higher than 15 mA, the pass voltage also is higher in the on state. To set the current through each pass transistor at 15 mA, the pullup resistor value is calculated as:

$$\text{Resistor value}(\Omega) = \frac{\text{Pullup voltage}(\text{V}) - 0.35\ \text{V}}{0.015\ \text{A}} \quad (1)$$

Table 9-1 provides resistor values for various reference voltages and currents at 15 mA, 10 mA, and 3 mA. The resistor value shown in the +10% column, or a larger value, should be used to ensure that the pass voltage of the transistor would be 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the GTL device at 0.175 V, although the 15 mA only applies to current flowing through the SN74GTL2003.

Table 9-1. Pullup Resistor Values(1) (2) (3) (4)

PULLUP RESISTOR VALUE (Ω)						
VOLTAGE	15 mA		10 mA		3 mA	
	NOMINAL	+10%	NOMINAL	+10%	NOMINAL	+10%
5.0 V	310	341	465	512	1550	1705
3.3 V	197	217	295	325	983	1082
2.5 V	143	158	215	237	717	788
1.8 V	97	106	145	160	483	532
1.5 V	77	85	115	127	383	422
1.2 V	57	63	85	94	283	312

(1) H = HIGH voltage level, L = LOW voltage level, X = do not care.
(2) Calculated for V_{OL} = 0.35 V
(3) Assumes output driver V_{OL} = 0.175 V at stated current
(4) +10% to compensate for V_{DD} range and resistor tolerance

9.2.1.3 Application Curve

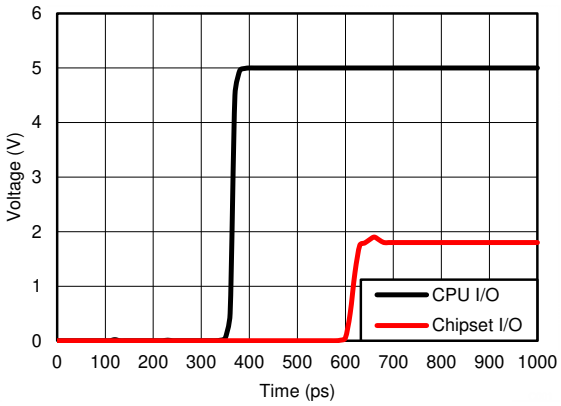


Figure 9-2. Signal Voltage vs Time (ps) (Simulated Design Results)

9.2.2 Unidirectional Down Translation

For unidirectional clamping (higher voltage to lower voltage), the G_{REF} input must be connected to D_{REF} and both pins pulled to the higher-side V_{CC} through a pullup resistor (typically 200 kΩ). TI recommends a filter capacitor on D_{REF}. Pullup resistors are required if the chipset I/Os are open drain. The opposite side of the reference transistor (S_{REF}) is connected to the processor core power supply voltage. When D_{REF} is connected through a 200-kΩ resistor to a 3.3-V to 5.5-V V_{CC} supply and S_{REF} is set from 1 V to V_{CC} – 1.5 V, the output of each Sn has a maximum output voltage equal to S_{REF}.

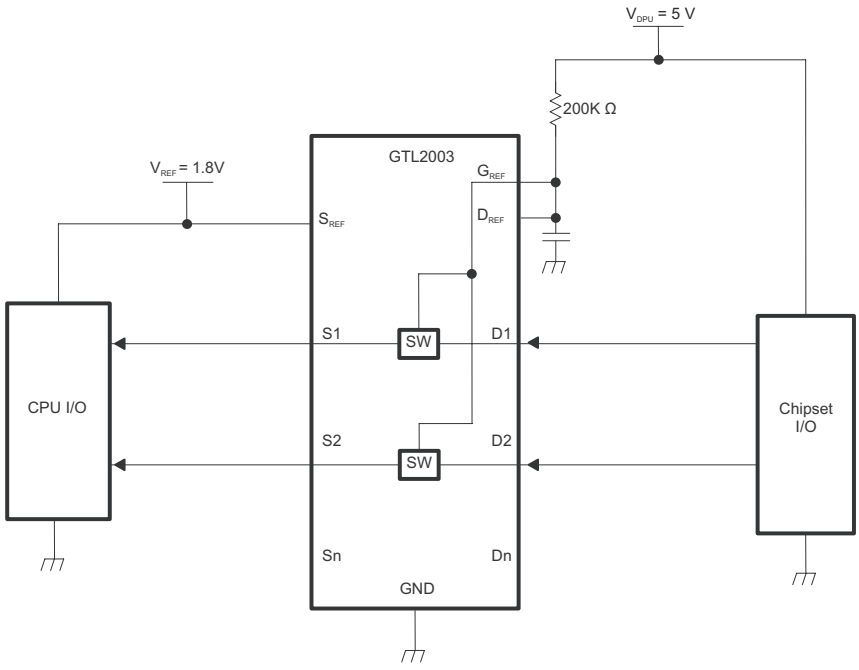


Figure 9-3. Unidirectional Down Translation to Protect Low-Voltage Processor Pins

9.2.2.1 Design Requirements

- SN74GTL2003 requires industry standard GTL and LVTTL/TTL voltage levels.
- Place pullup resistors of ≅200 kΩ in all inputs/outputs to the GTL/TTL voltage levels.
- Place 0.1-μF bypass capacitors close to the power supply pins to reduce errors coupling in from noisy or high-impedance power supplies.
- Comply to the parameters in *Section 6.3*.

9.2.2.2 Detailed Design Procedure

9.2.2.2.1 Sizing Pullup Resistors

The pullup resistor value should limit the current through the pass transistor when it is in the on state to about 15 mA. This ensures a pass voltage of 260 mV to 350 mV. If the current through the pass transistor is higher than 15 mA, the pass voltage also is higher in the on state. To set the current through each pass transistor at 15 mA, the pullup resistor value is calculated as:

$$\text{Resistor value}(\Omega) = \frac{\text{Pullup voltage}(\text{V}) - 0.35\ \text{V}}{0.015\ \text{A}} \quad (2)$$

Table 9-2 provides resistor values for various reference voltages and currents at 15 mA, 10 mA, and 3 mA. The resistor value shown in the +10% column, or a larger value, should be used to ensure that the pass voltage of the transistor would be 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the GTL device at 0.175 V, although the 15 mA only applies to current flowing through the SN74GTL2003.

Table 9-2. Pullup Resistor Values(1) (2) (3) (4)

PULLUP RESISTOR VALUE (Ω)						
VOLTAGE	15 mA		10 mA		3 mA	
	NOMINAL	+10%	NOMINAL	+10%	NOMINAL	+10%
5.0 V	310	341	465	512	1550	1705
3.3 V	197	217	295	325	983	1082
2.5 V	143	158	215	237	717	788
1.8 V	97	106	145	160	483	532
1.5 V	77	85	115	127	383	422
1.2 V	57	63	85	94	283	312

(1) H = HIGH voltage level, L = LOW voltage level, X = do not care.
(2) Calculated for V_{OL} = 0.35 V
(3) Assumes output driver V_{OL} = 0.175 V at stated current
(4) +10% to compensate for V_{DD} range and resistor tolerance

9.2.3 Unidirectional Up Translation

For unidirectional up translation (lower voltage to higher voltage), the reference transistor is connected the same as for a down translation. A pullup resistor is required on the higher voltage side (Dn or Sn) to get the full HIGH level, because the GTL device only passes the reference source (S_{REF}) voltage as a HIGH when doing an up translation. The driver on the lower voltage side only needs pullup resistors if it is open drain.

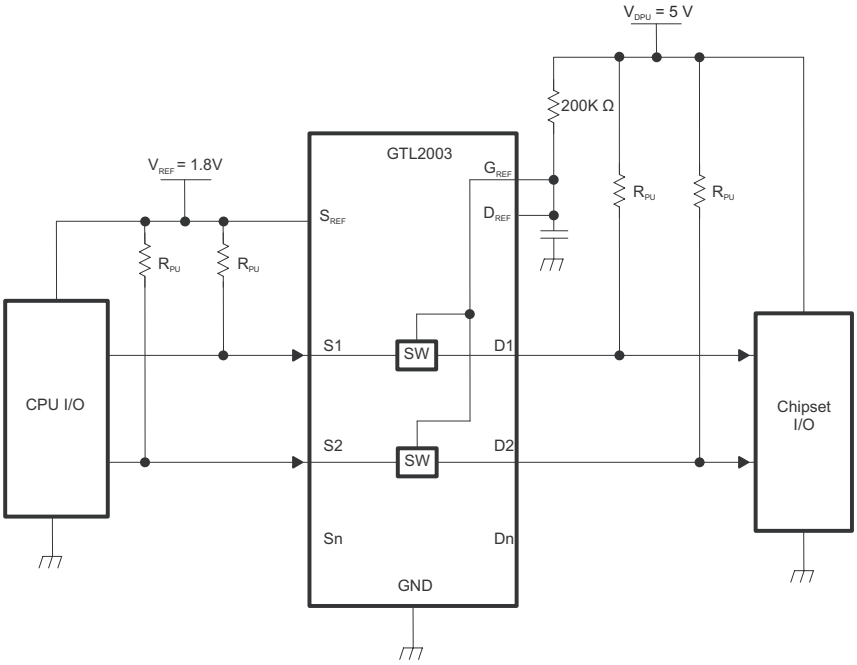


Figure 9-4. Unidirectional Up Translation to Higher-Voltage Chipsets

9.2.3.1 Design Requirements

- SN74GTL2003 requires industry standard GTL and LVTTL/TTL voltage levels.
- Place pullup resistors of ≅200 kΩ in all inputs/outputs to the GTL/TTL voltage levels.
- Place 0.1-µF bypass capacitors close to the power supply pins to reduce errors coupling in from noisy or high-impedance power supplies.
- Comply to the parameters in *Section 6.3*

9.2.3.2 Detailed Design Procedure

9.2.3.2.1 Sizing Pullup Resistors

The pullup resistor value should limit the current through the pass transistor when it is in the on state to about 15 mA. This ensures a pass voltage of 260 mV to 350 mV. If the current through the pass transistor is higher than 15 mA, the pass voltage also is higher in the on state. To set the current through each pass transistor at 15 mA, the pullup resistor value is calculated as:

$$\text{Resistor value}(\Omega) = \frac{\text{Pullup voltage}(\text{V}) - 0.35\ \text{V}}{0.015\ \text{A}} \tag{3}$$

Table 9-3 provides resistor values for various reference voltages and currents at 15 mA, 10 mA, and 3 mA. The resistor value shown in the +10% column, or a larger value, should be used to ensure that the pass voltage of the transistor would be 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the GTL device at 0.175 V, although the 15 mA only applies to current flowing through the SN74GTL2003.

Table 9-3. Pullup Resistor Value(1) (2) (3) (4)

PULLUP RESISTOR VALUE (Ω)						
VOLTAGE	15 mA		10 mA		3 mA	
	NOMINAL	+10%	NOMINAL	+10%	NOMINAL	+10%
5.0 V	310	341	465	512	1550	1705
3.3 V	197	217	295	325	983	1082
2.5 V	143	158	215	237	717	788

Table 9-3. Pullup Resistor Value(1) (2) (3) (4) (continued)

PULLUP RESISTOR VALUE (Ω)						
VOLTAGE	15 mA		10 mA		3 mA	
	NOMINAL	+10%	NOMINAL	+10%	NOMINAL	+10%
1.8 V	97	106	145	160	483	532
1.5 V	77	85	115	127	383	422
1.2 V	57	63	85	94	283	312

(1) H = HIGH voltage level, L = LOW voltage level, X = do not care.
(2) Calculated for V_{OL} = 0.35 V
(3) Assumes output driver V_{OL} = 0.175 V at stated current
(4) +10% to compensate for V_{DD} range and resistor tolerance

10 Power Supply Recommendations

Place 0.1-µF bypass capacitors close to the power supply pins to reduce errors coupling in from noisy or high-impedance power supplies.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

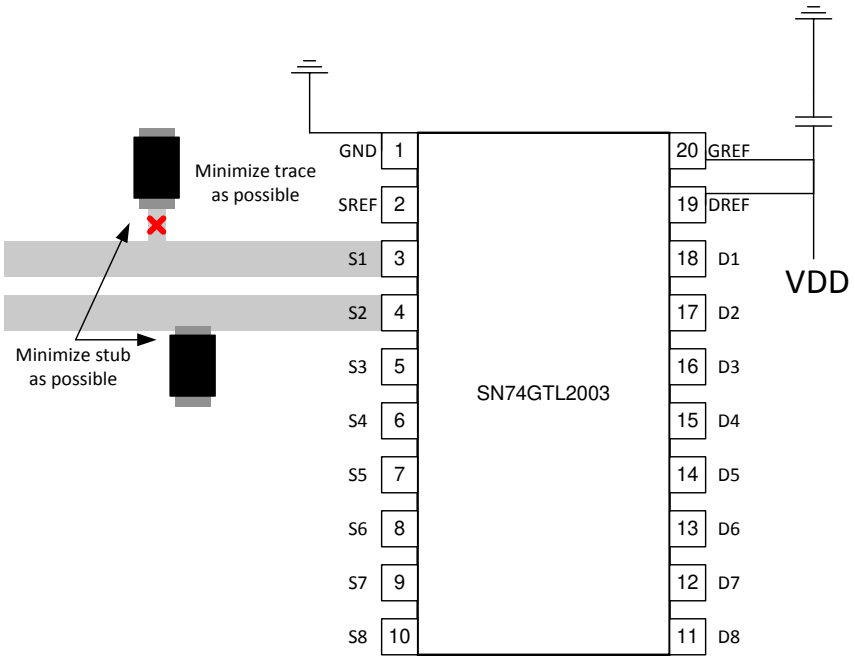


Figure 11-1. Layout Example for GTL Trace

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74GTL2003PW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GK2003	Samples
SN74GTL2003PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GK2003	Samples
SN74GTL2003RKSR	ACTIVE	VQFN	RKS	20	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	GK2003	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

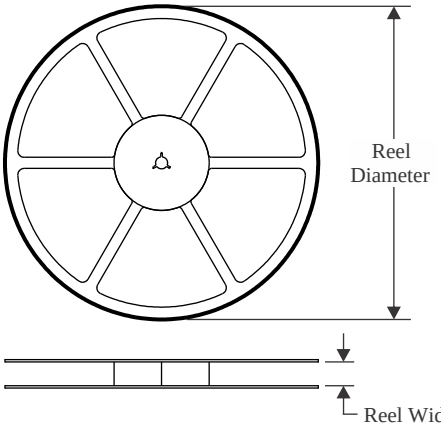
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

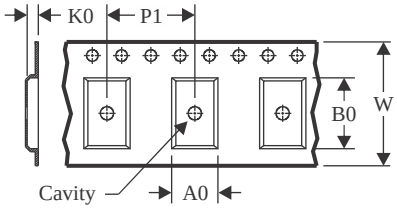
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

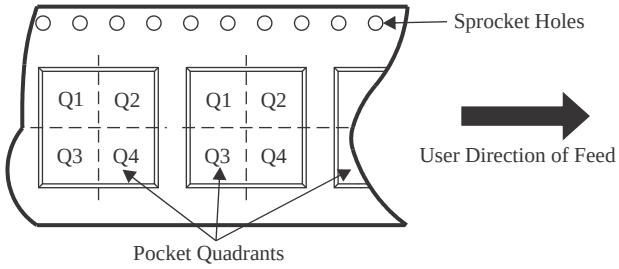


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

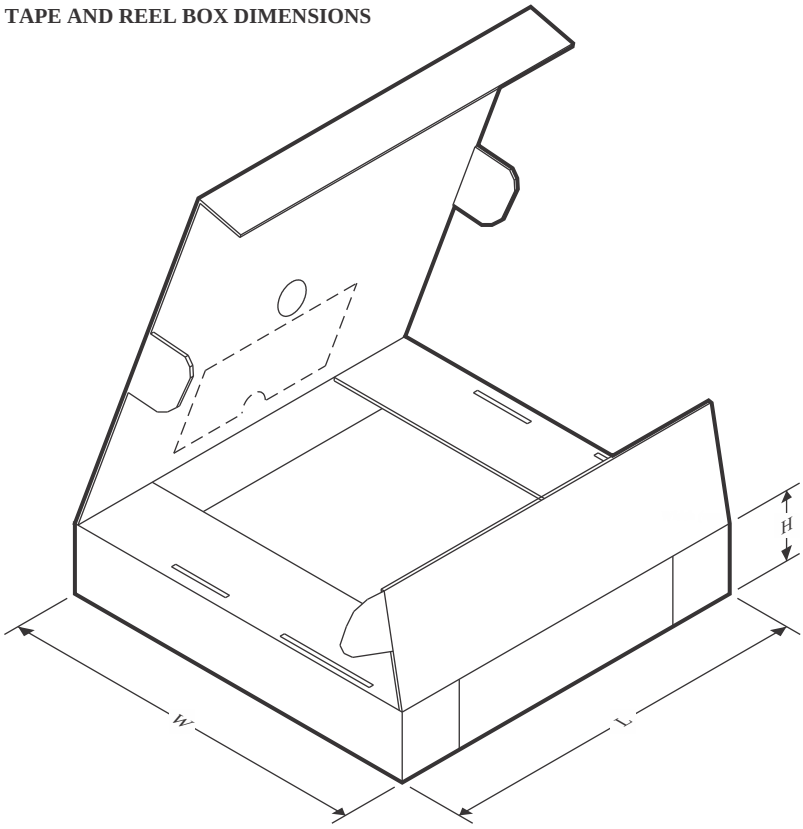
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74GTL2003PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74GTL2003PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74GTL2003RKSR	VQFN	RKS	20	3000	177.8	12.4	2.73	4.85	1.03	4.0	12.0	Q1
SN74GTL2003RKSR	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1

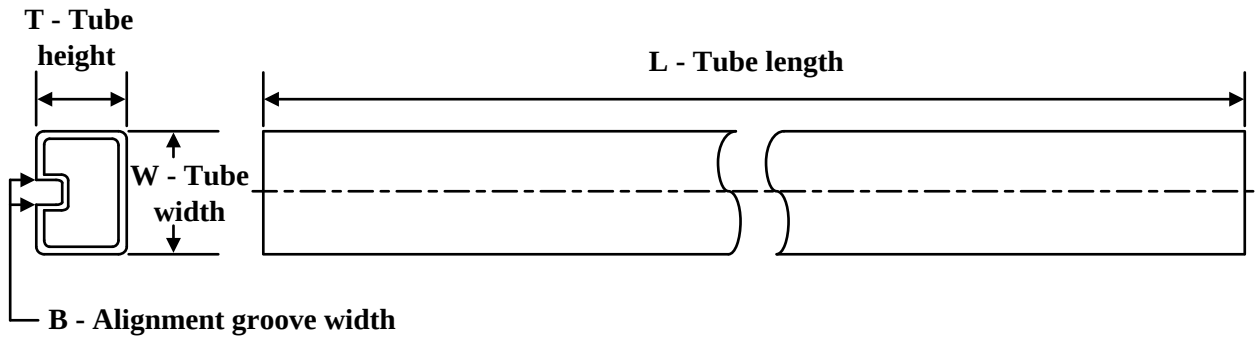
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74GTL2003PWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74GTL2003PWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74GTL2003RKSR	VQFN	RKS	20	3000	202.0	201.0	28.0
SN74GTL2003RKSR	VQFN	RKS	20	3000	210.0	185.0	35.0

TUBE



*All dimensions are nominal

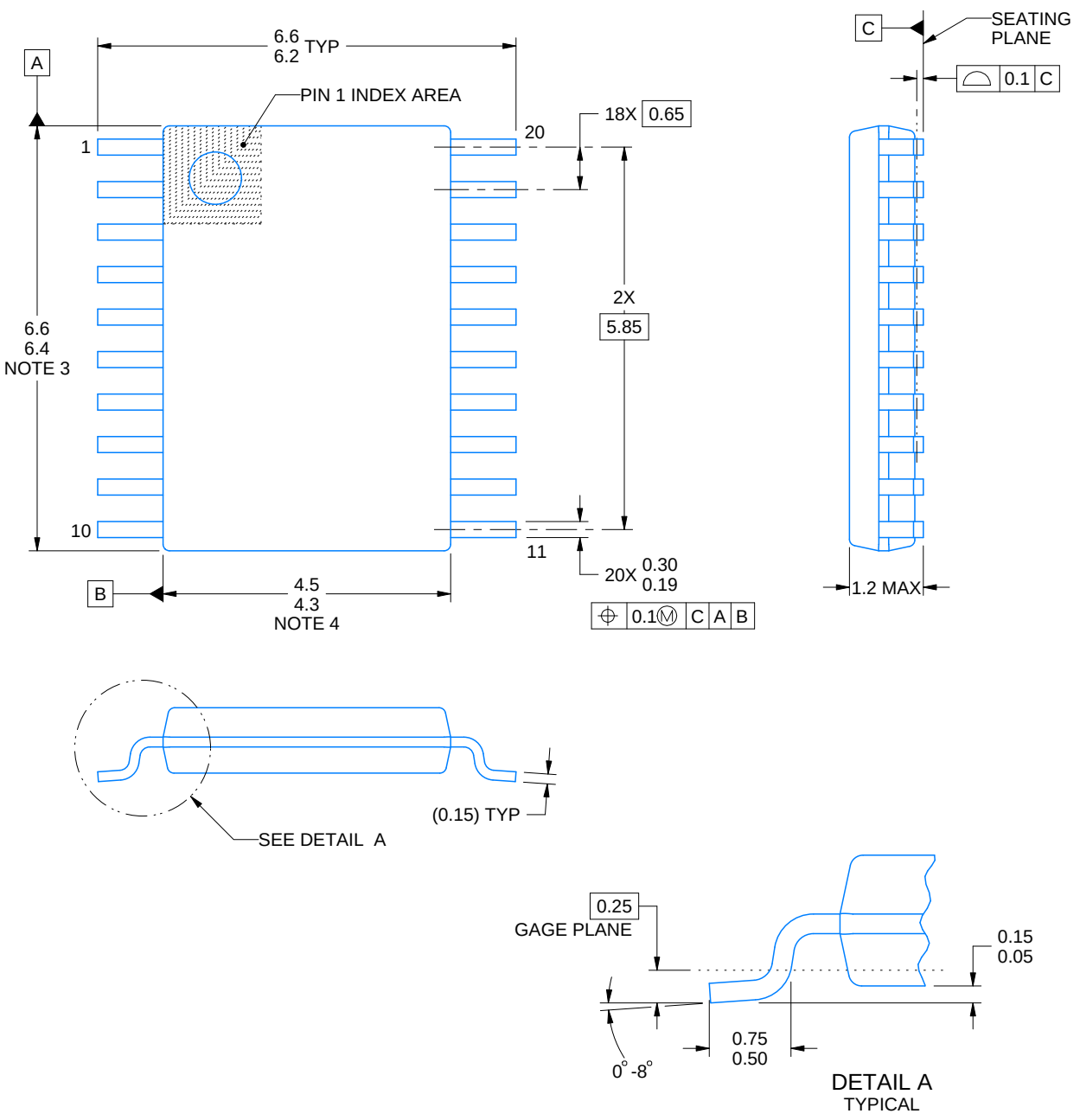
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74GTL2003PW	PW	TSSOP	20	70	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0020A

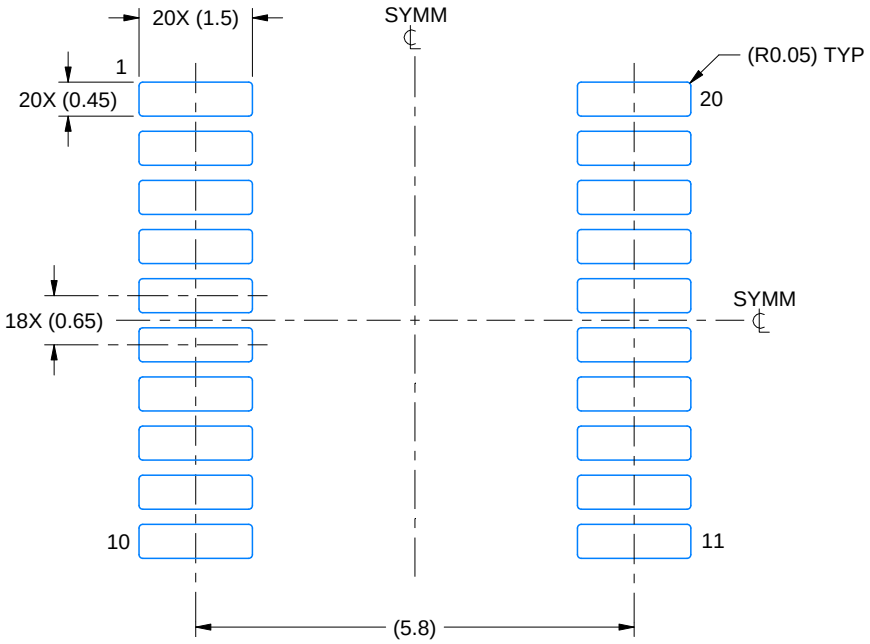
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



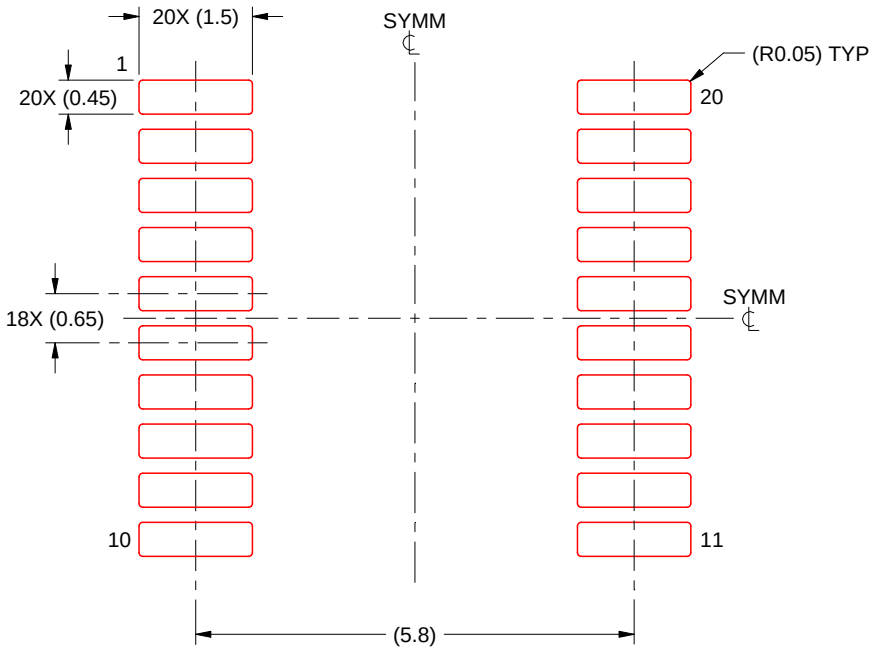
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



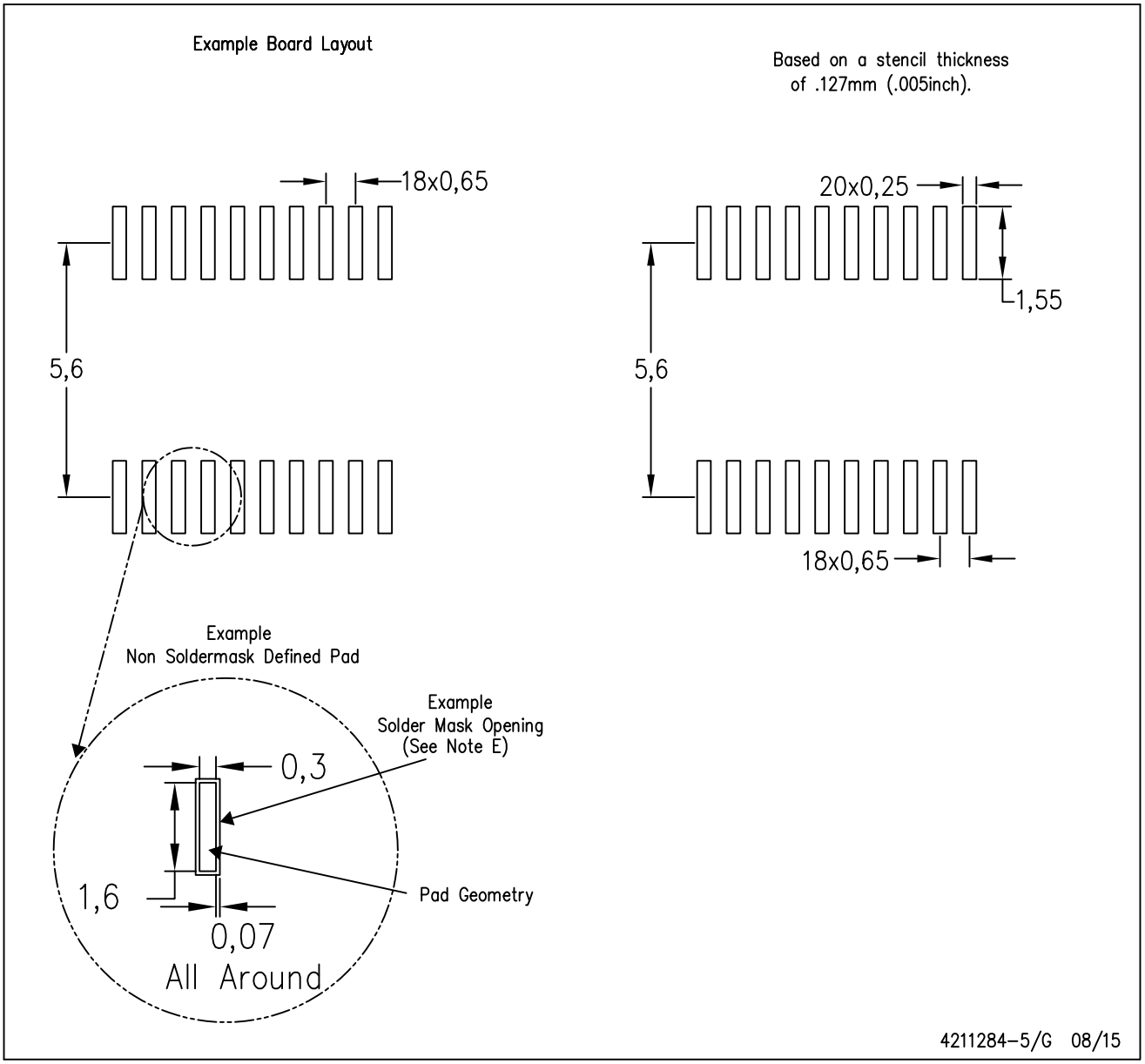
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

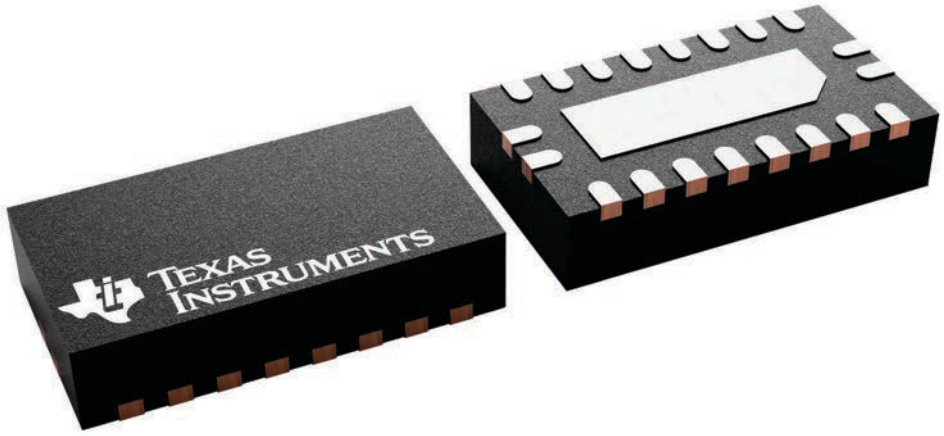
RKS 20

VQFN - 1 mm max height

2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

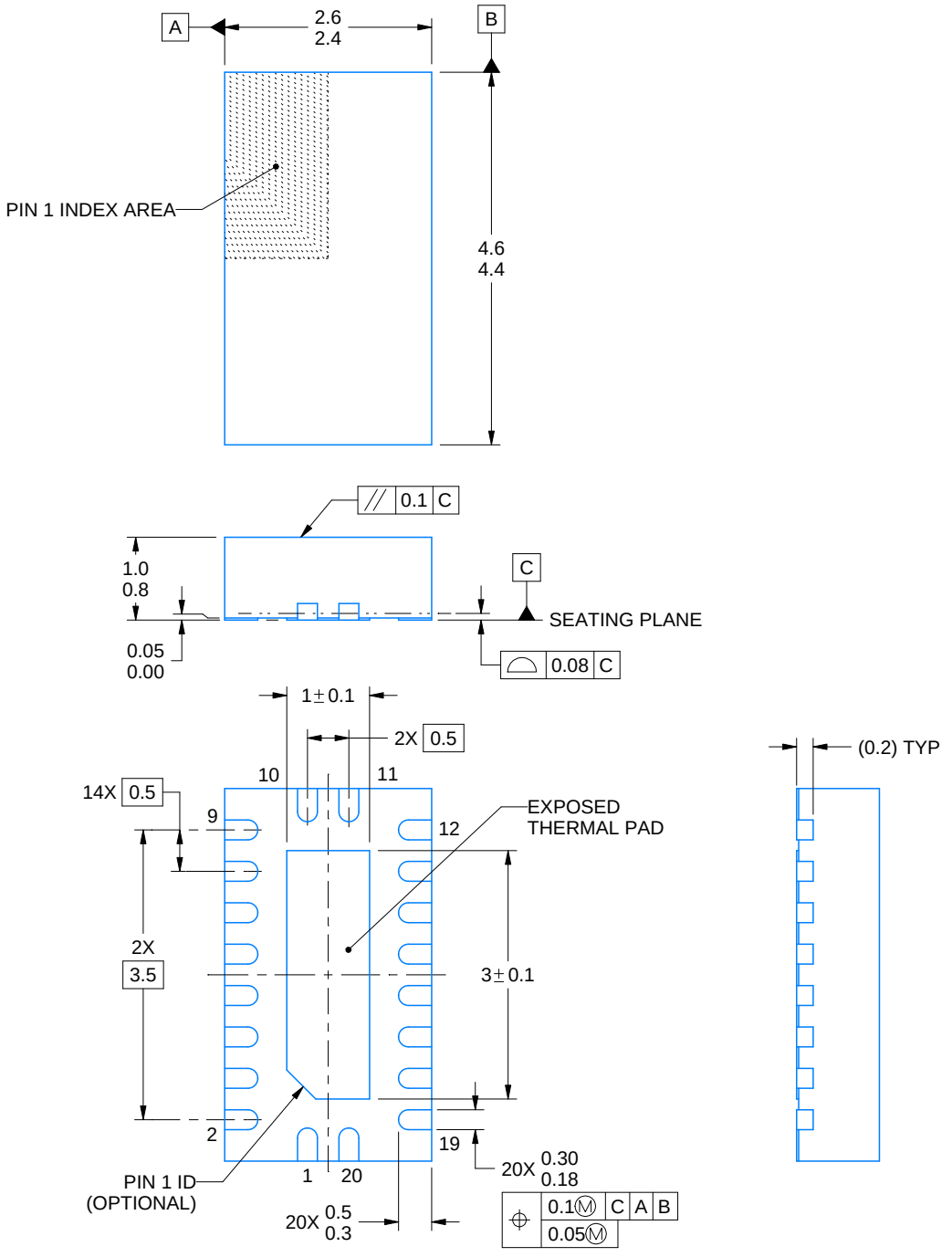


PACKAGE OUTLINE

RKS0020A

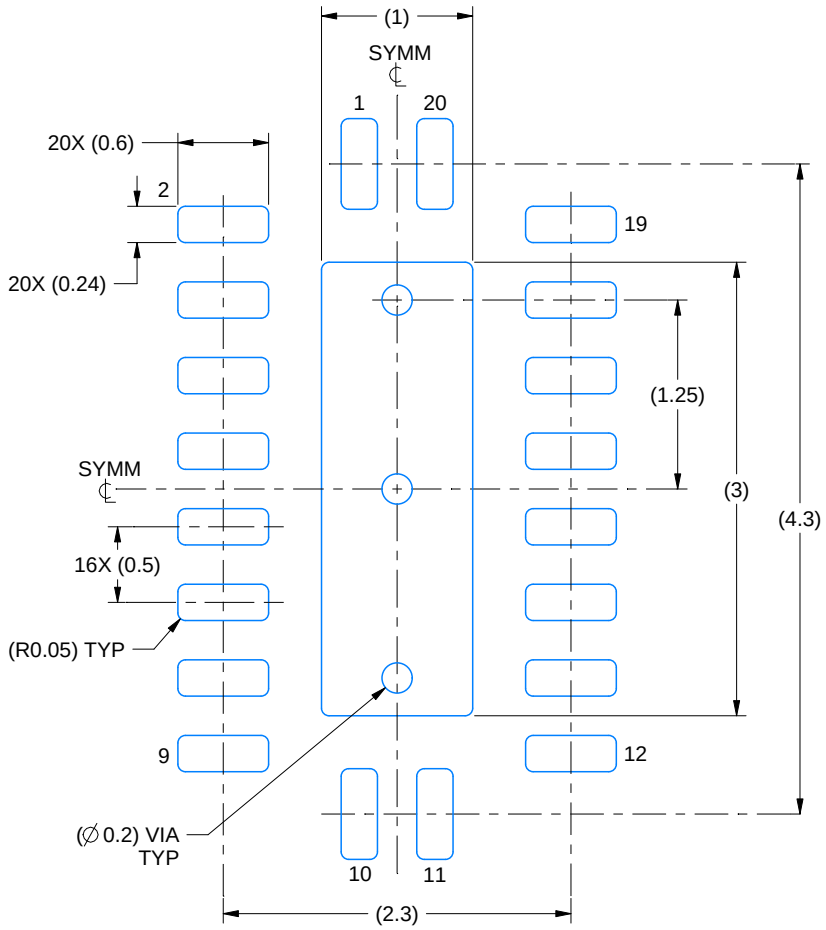
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

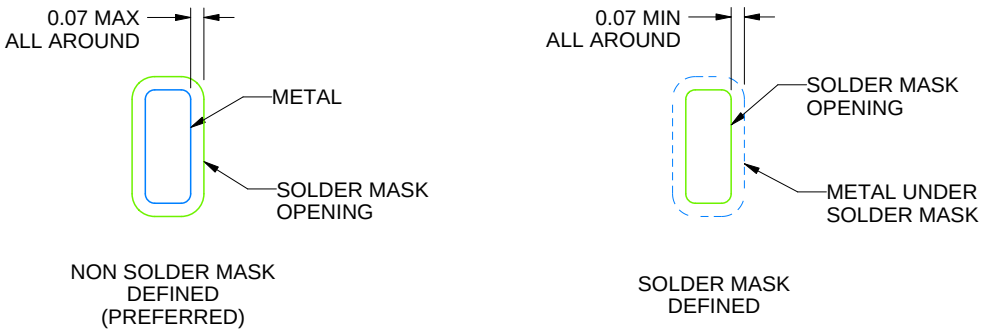


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

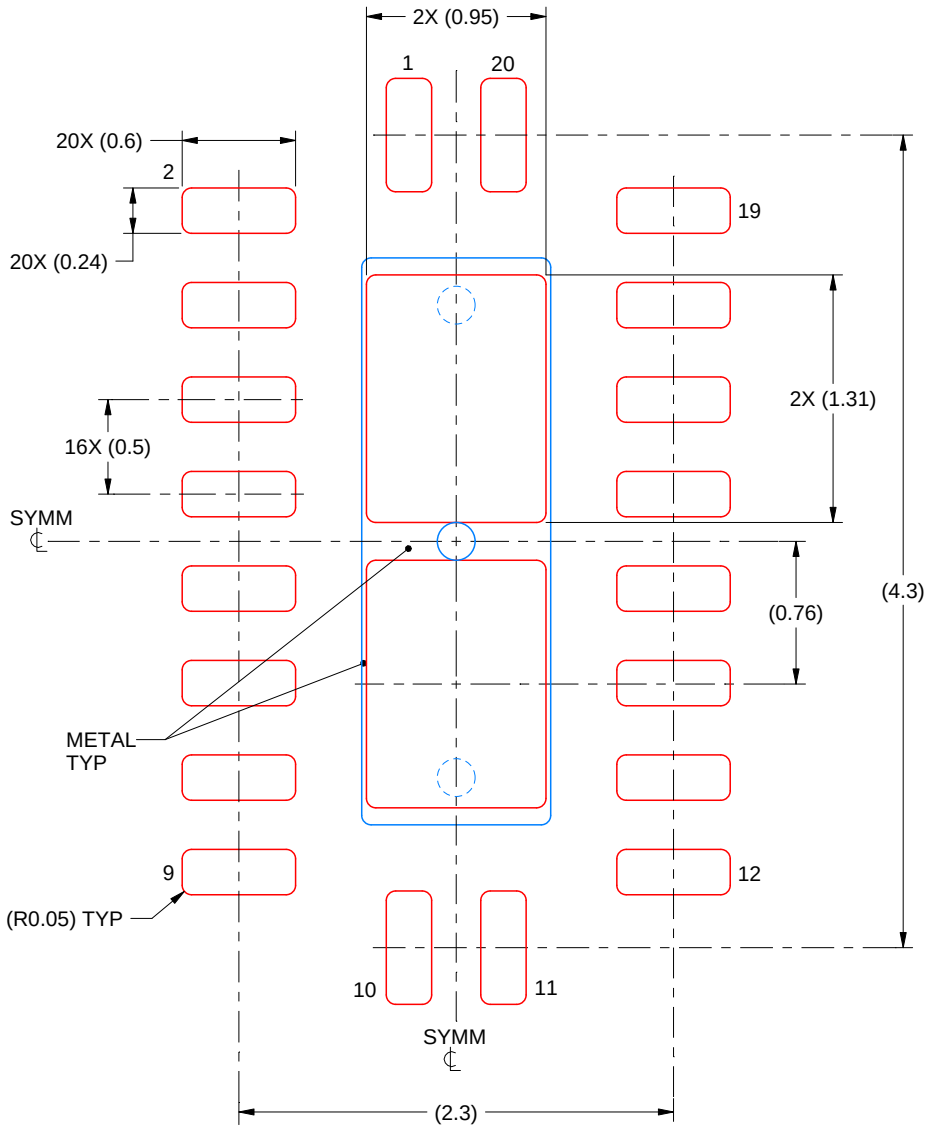


SOLDER MASK DETAILS

4222490/B 02/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4222490/B 02/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265