0.45Ω Dual SPDT Bidirectional Analog Switch

Check for Samples: TS3A5223

FEATURES

- **Low ON Resistance Switches**
  - **0.45 Ω (Typical) at 3.6V**
  - **0.85 Ω(Typical) at 1.8V**
- **Wide Supply Range: 1.65 V to 3.6 V**
- **1.0 V Compatible Logic Interface**
- **High Switch Bandwidth 80 MHz**
- **0.01% THD Across Entire Band**
- **Specified min Break-before-make**
- **Bi-directional Switching**
- **–75 dB Channel-to-Channel Cross Talk**
- **–70 dB Channel-to-Channel OFF Isolation of Very Low Power Dissipation and Leakage Currents**
- **Very Small QFN-10 Package: 1.8mm × 1.4mm**
- **ESD Protection on all Pins**
  - **2kV HBM, 500 V CDM**

APPLICATIONS

- **Portable Electronics**
- **Smarphones, Tablets**
- **Home Electronics**
- **Wireline Communication**

DESCRIPTION

The TS3A5223 is a high-speed dual analog switch with break-before-make and bi-directional signal switching capability. The TS3A5223 can be used as a dual 2:1 multiplexer or a 1:2 dual de-multiplexer.

The TS3A5223 offers very low ON resistance, very low THD, channel-to-channel crosstalk and very high OFF isolation. These features make TS3A5223 suitable for application in Audio signal routing and switching applications.

The TS3A5223 control logic supports 1.0V-3.6V CMOS logic levels. The logic interface allows direct interface with a wide range of CPUs and microcontrollers without increasint the current drawn from supply (ICC) and thus lowering power consumption.

Table 1. TS3A5223 Function Table

SEL1	SEL2	COM1	COM2
0	0	NC1	NC2
1	1	NO1	NO2
1	0	NO1	NC2
0	1	NC1	NO2

TS3A5223 FUNCTIONAL DIAGRAM

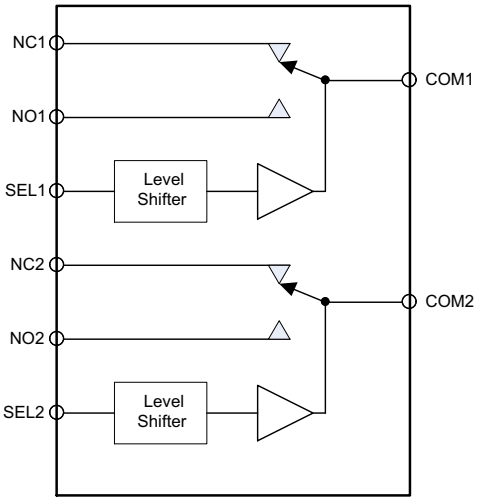
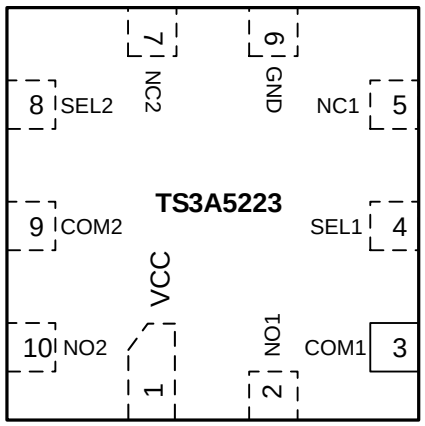


Figure 1. Functional Diagram

TS3A5223 RSW (Top View)



TS3A5223 PIN DESCRIPTION

NAME	PIN NUMBER	DESCRIPTION
VCC	1	Postive supply Input – Connect 1.65V up to 3.6V supply
NC1, NO1, NC2, NO2	5, 2, 7, 10	Channel Input/Output signal Pins
COM1, COM2	3, 9	Channel Input/Output signal Pins
GND	6	Ground reference pin
SEL1, SEL2	4, 8	Select logic pin

ORDERING INFORMATION(1)

T_A	PART NUMBER	PACKAGE		TOP-SIDE MARKING
–40°C to 85°C	TS3A5223RSWR	10-Pin µ-QFN	Reel of 3000	B2_

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Specified at T_A= –40°C to 85°C unless otherwise noted.

			VALUE		UNIT
			MIN	MAX	
VCC	Positive DC Supply Voltage		–0.3	4.3(2)	V
V_{IN-Max}	Pins S1A, S1B, S2A, S2B, OUT1, OUT2, SEL1, SEL2 to GND pin voltage		–0.3	4.3(2)	V
$I_{OUT-Max}$	Pin OUT1, OUT2 max DC current			±300	mA
$I_{OUT-Peak}$	Pin OUT1, OUT2 peak current (1ms pulse at 10% duty cycle)			±500	mA
P_D	Total device power dissipation at T_A = 85°C	10-µQFN RSW		430	mW
ESD	ESD Rating – HBM			2000	V
	ESD Rating – CDM			500	V
T_A	Operating free-air ambient temperature range		–40	85	°C
T_J	Junction temperature range		–55	150	°C
T_{stg}	Storage temperature range		–55	150	°C

(1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Not rated for continuous operation, 0.5% duty cycle at 1 kHz recommended

DISSIPATION RATINGS(1)(2)(3)

BOARD	PACKAGE	θ_{JC}	θ_{JA}(3)	DERATING FACTOR ABOVE T_A = 25ºC	T_A < 25°C	T_A = 70°C	T_A = 85°C
High-K	10-Pin µ-QFN	46°C/W	93°C/W	10.7 mW/ºC	1075W	590mW	430mW

(1) Maximum dissipation values for retaining device junction temperature of 150°C
(2) Refer to TI's design support web page at www.ti.com/thermal for improving device thermal performance
(3) Operating at the absolute T_{J-max} of 150°C can affect reliability– for higher reliability it is recommended to ensure T_J < 125°C

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
VCC	Positive DC Supply Voltage		1.65	3.6	V
V_{Max}	Pins NC1, NO1, NC2, NO2, COM1, COM2, SEL1, SEL2 to GND pin maximum voltage		0	3.6	V
T_A	Operating free-air ambient temperature range		–40	85	ºC
dt/dv	SEL pin Input rise and fall time limit	VCC= 1.6 to 2.7V			sec/V
		VCC = 3.0 to 3.6V			

ELECTRICAL CHARACTERISTICS

Specified over the recommended junction temperature range $T_A = T_J$ = –40°C to 85°C Typical values are at $T_A = T_J$ = 25°C (unless otherwise noted).

PARAMETER		VCC (V)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC CHARACTERISTICS							
V_{IH}	High-level Input voltage SEL1, SEL2 inputs	3.6		0.8			V
		2.3		0.8			
		1.8		0.8			
V_{IL}	Low-level Input voltage SEL1, SEL2	3.6				0.3	V
		2.3				0.3	
		1.8				0.3	
R_{ON}	Switch ON Resistance	3.6	V_S = 0 to VCC, IS = 100 mA, VSEL = 1.0V, 0V		0.45	0.6	Ω
		2.3			0.6	0.8	
		1.8			0.85	1.2	
ΔR_{ON}	Difference of on-state resistance between switches	3.6	V_S = 2V, 0.8V, IS = 100 mA, VSE L= 1.0V, 0V		0.05		
$R_{ON-FLAT}$	ON resistance flatness	3.6	V_S = 0 to VCC, IS = 100mA, VSEL = 1.0V, 0V		0.1	0.2	
		2.3			0.15	0.35	
		1.8			0.4	0.65	
I_{OFF}	NC, NO pin leakage current when not selected	3.6	V_S = 0.3 or 3.0V, VCOM = 3.0 or 0.3V		5	90	nA
$I_{S(ON)}$	NC, NO pin leakage current when selected	3.6	V_S = 0.3 or 3.0V, VCOM = No Load		4	60	nA
I_{SEL}	Select Pin input leakage current	V_S	Vs = 0 or 3.6 V			100	nA
I_{CC}	Quiescent supply current	3.6	VSEL = 0 or VCC		700	2000	nA
I_{CCLV}	Supply current change	3.6	VSEL = 1.0V to VSEL=VCC			200	nA
SWITCHING PARAMETERS(1)(2)							
t_{PHL}	Logic high to low propagation delay	3.6	R_L = 50 Ω, C_L = 35 pF		0.1		ns
		2.5			0.2		
		1.8			0.2		
t_{PLH}	Logic low to high propagation delay	3.6	R_L = 50 Ω, C_L = 35 pF		0.1		ns
		2.5			0.2		
		1.8			0.2		
t_{ON}	Turn-ON time	2.3-3.6	R_L = 50 Ω, C_L = 35 pF, VS = 1.5 V			70	ns
t_{OFF}	Turn-OFF time	2.3-3.6	R_L = 50 Ω, C_L = 35 pF, VS = 1.5 V			75	ns
t_D	Break-before-make time delay	3.6	R_L = 50 Ω, C_L = 35 pF, VS = 1.5 V	2	8		ns
Q_{INJ}	Charge Injection	3.6	C_L = 1 nF, VS = 0 V		40		pC
AC CHARACTERISTICS							
BW	-3dB Bandwidth	1.65V-3.6V	R_L = 50 Ω, C_L = 35 pF		80		MHz
V_{ISO}	Channel OFF isolation	1.65V-3.6V	VS = 1 V rms, f = 100 kHz		–70		dB
V_{Xtalk}	Channel-to-Channel Cross talk	1.65V-3.6V	VS=1V rms, f= 100kHz		–75		dB
THD	Total harmonic distortion	1.65V-3.6V	R_L = 600 Ω, VSEL = 2 Vpk-pk, f = 20 Hz to 20 kHz		0.01%		
C_{SEL}	Select Pin Input Capacitance	3.3V	f =1 MHz		3		pF
C_{ON}	NC, NO, and COM input capacitance when switch is selected	3.3V	f = 1 MHz		115		pF
C_{OFF}	NC, NO, and COM input capacitance when switch is not selected	3.3V	f = 1 MHz		50		pF

(1) Rise and Fall propagation delays, t_{PHL} and t_{PLH}, are measured between 50% values of the input and the corresponding output signal amplitude transition.
(2) Assured by characterization only. Validated during qualification. Not measured in production testing.

TYPICAL CHARACTERISTICS

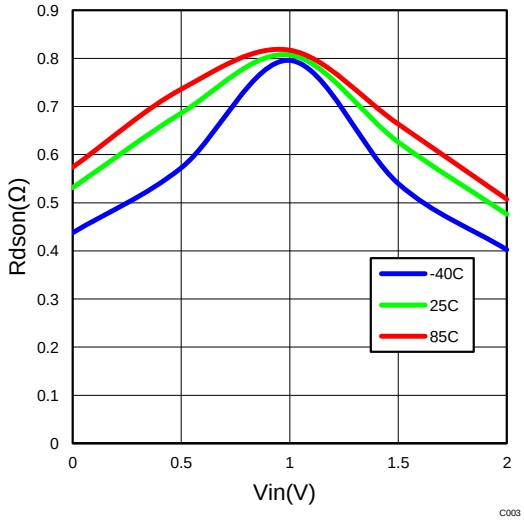


Figure 2. On-Resistance vs. Switch Input Voltage at VCC=1.8V

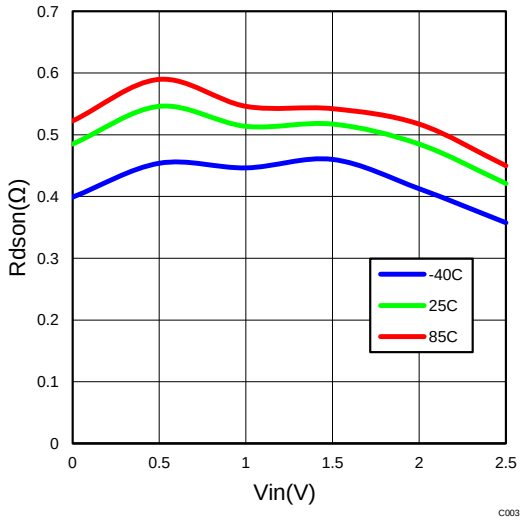


Figure 3. On-Resistance vs. Switch Input Voltage at VCC=2.3V

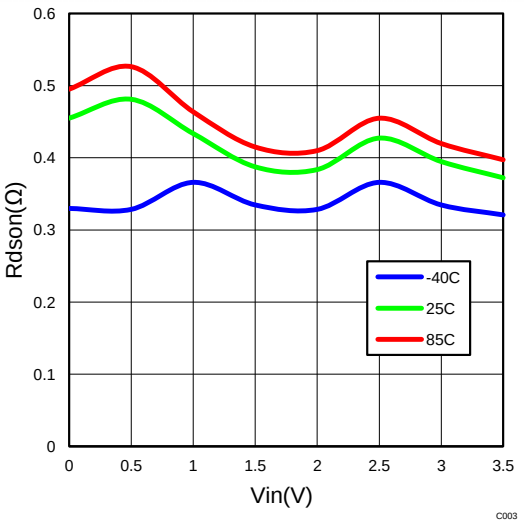


Figure 4. On-Resistance vs. Switch Input Voltage at VCC=3.0V

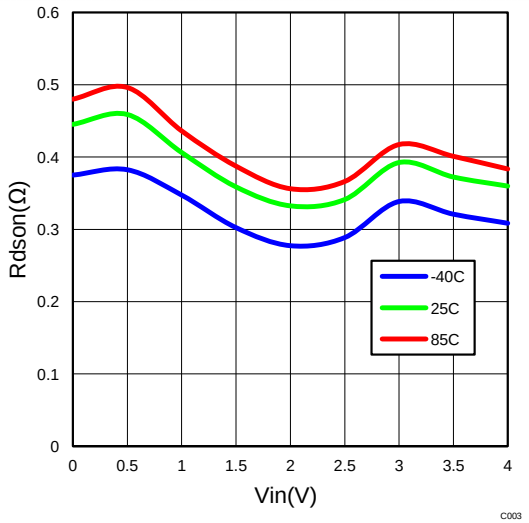


Figure 5. On-Resistance vs. Switch Input Voltage at VCC=3.6V

TYPICAL CHARACTERISTICS (continued)

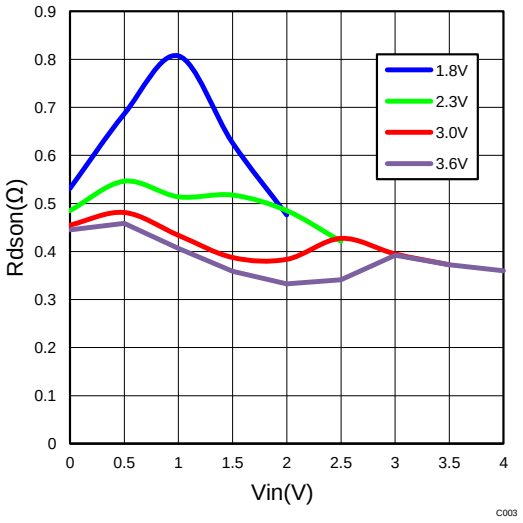


Figure 6. On-Resistance vs. Switch Input Voltage at T_A=25°C

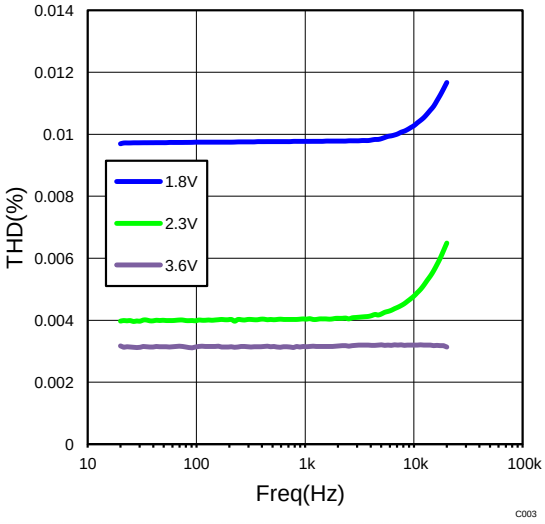


Figure 7. Total Harmonic Distortion

PARAMETER MEASUREMENT INFORMATION

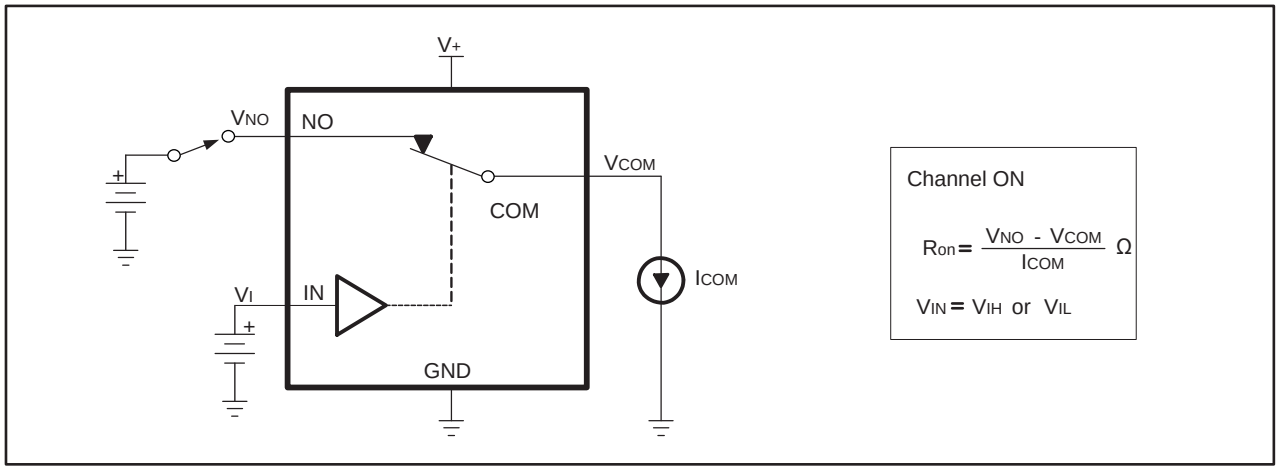
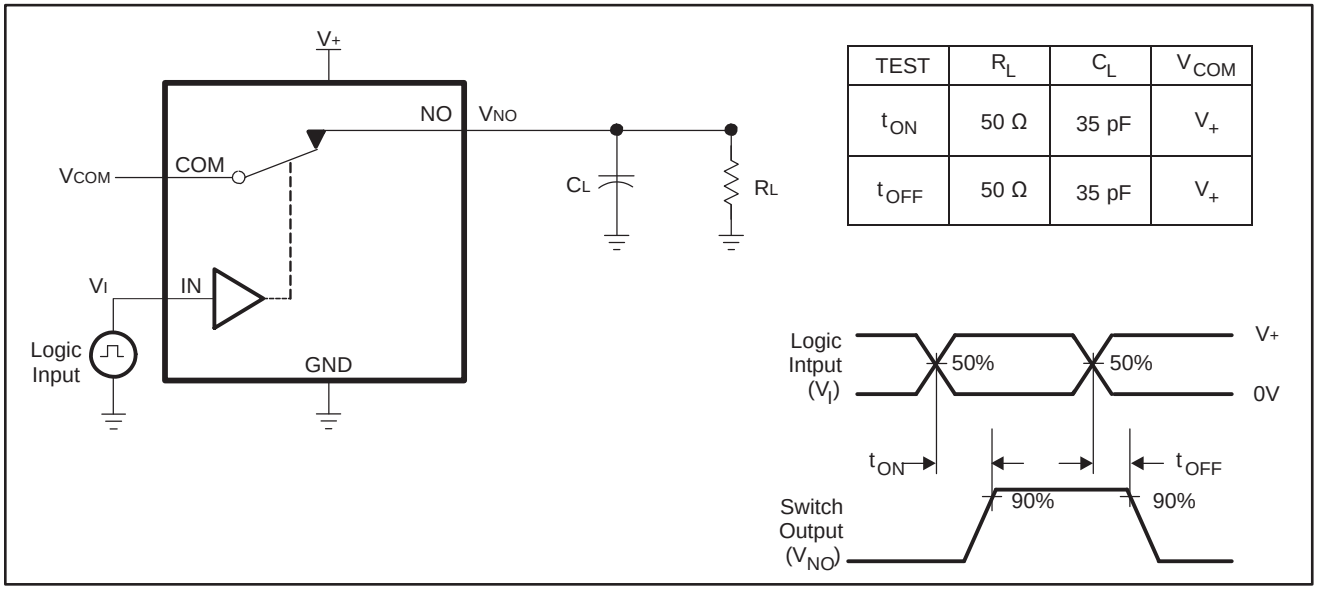


Figure 8. ON-State Resistance (R_{ON})



TEST	R_L	C_L	V_{COM}
t_{ON}	50 Ω	35 pF	V_+
t_{OFF}	50 Ω	35 pF	V_+

Figure 9. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

PARAMETER MEASUREMENT INFORMATION (continued)

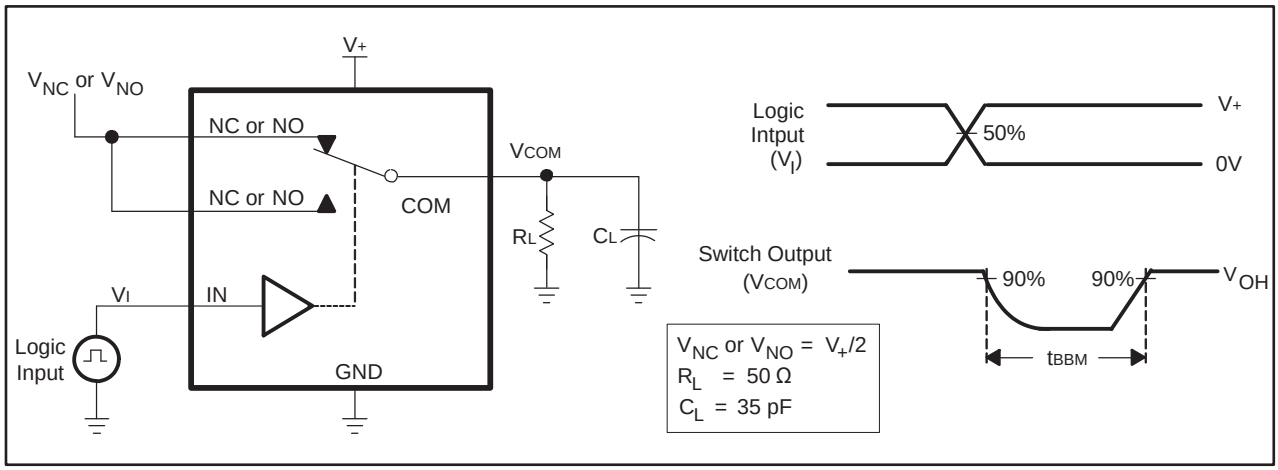


Figure 10. Break-Before-Make Time (t_D)

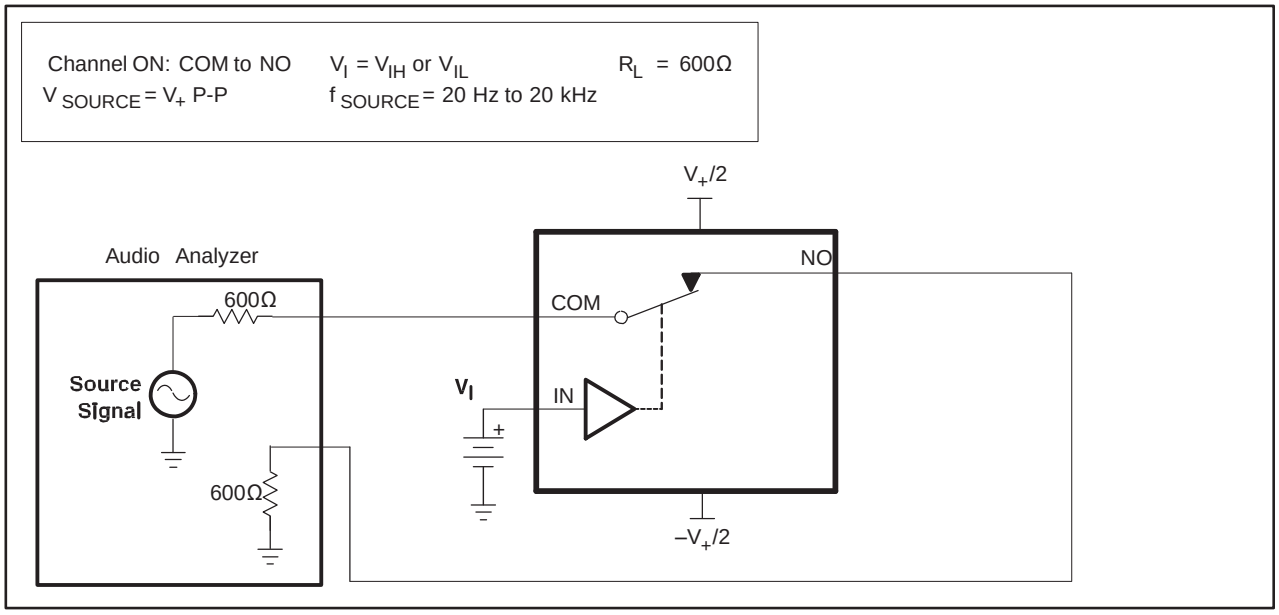


Figure 11. THIRD HARMONIC DISTORTION (THD)

PARAMETER MEASUREMENT INFORMATION (continued)

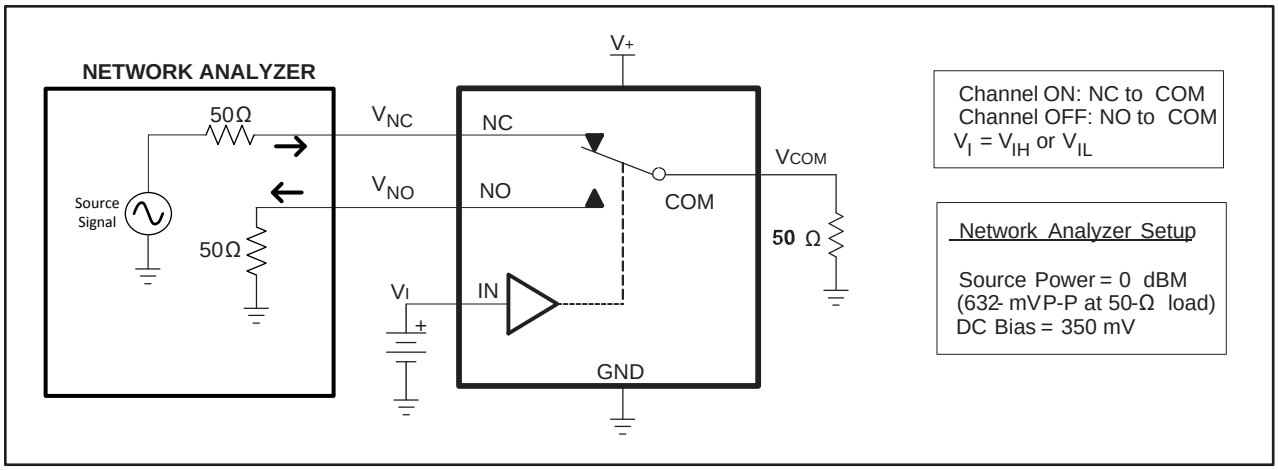


Figure 12. Crosstalk(X_{TALK})

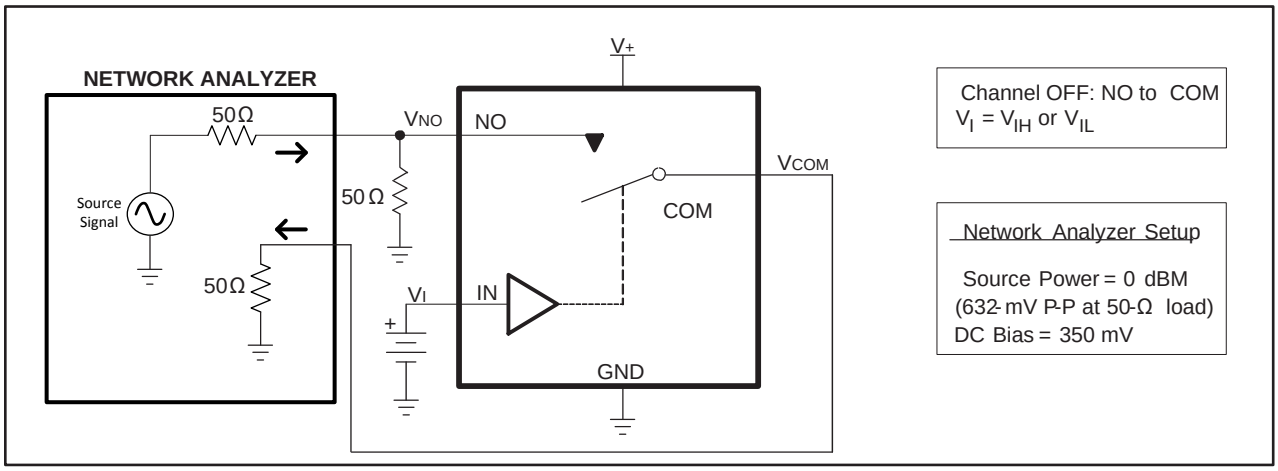


Figure 13. OFF Isolation (O_{ISO})

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TS3A5223RSWR	ACTIVE	UQFN	RSW	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	B2A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

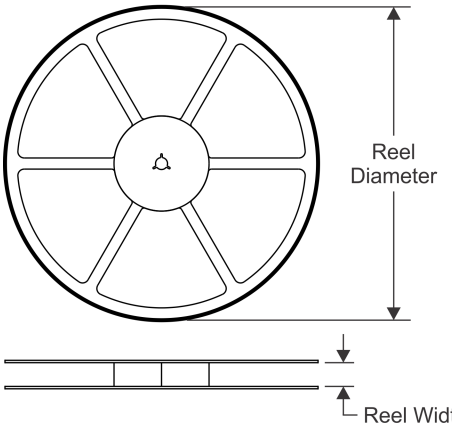
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

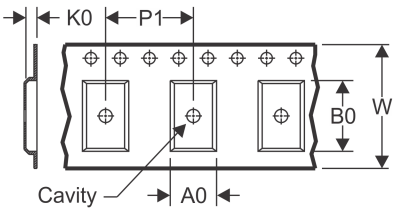
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

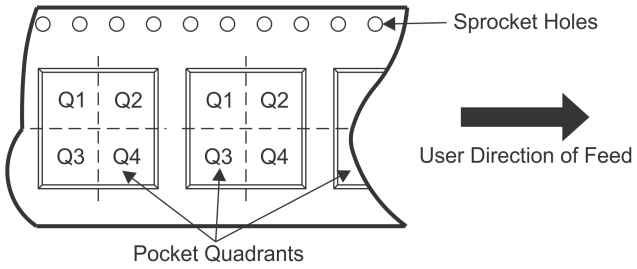


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

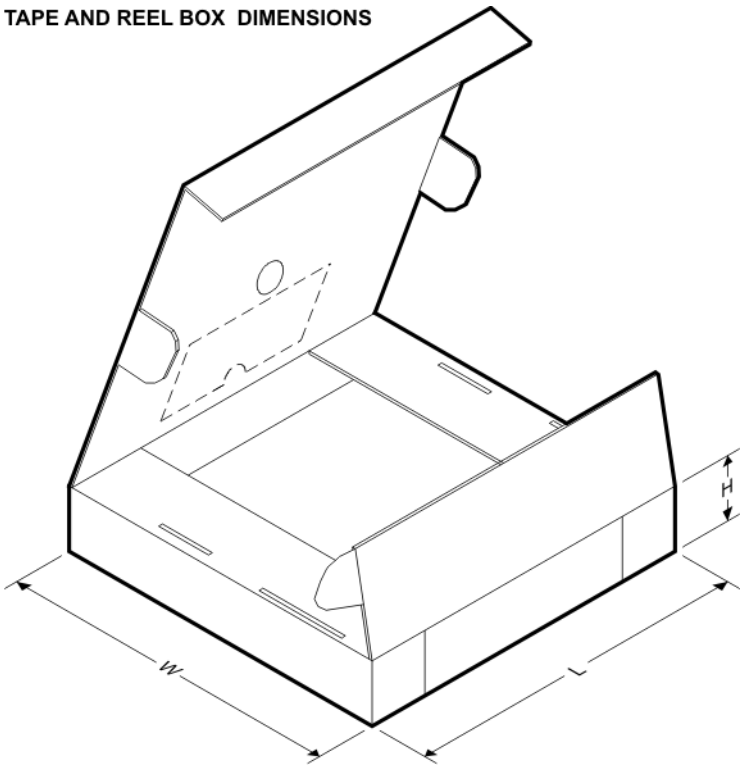
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A5223RSWR	UQFN	RSW	10	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q1

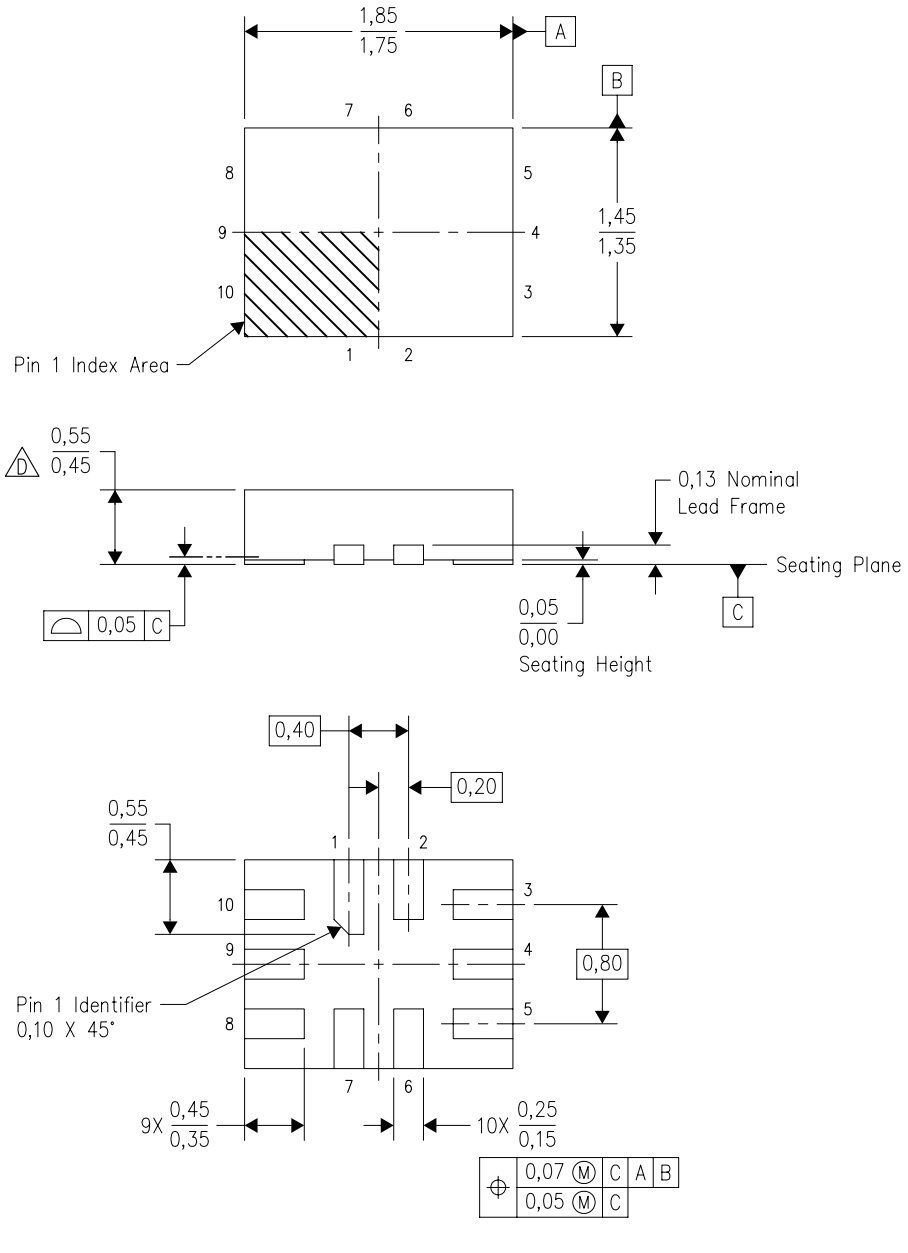
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3A5223RSWR	UQFN	RSW	10	3000	184.0	184.0	19.0

RSW (R–PUQFN–N10) PLASTIC QUAD FLATPACK NO–LEAD



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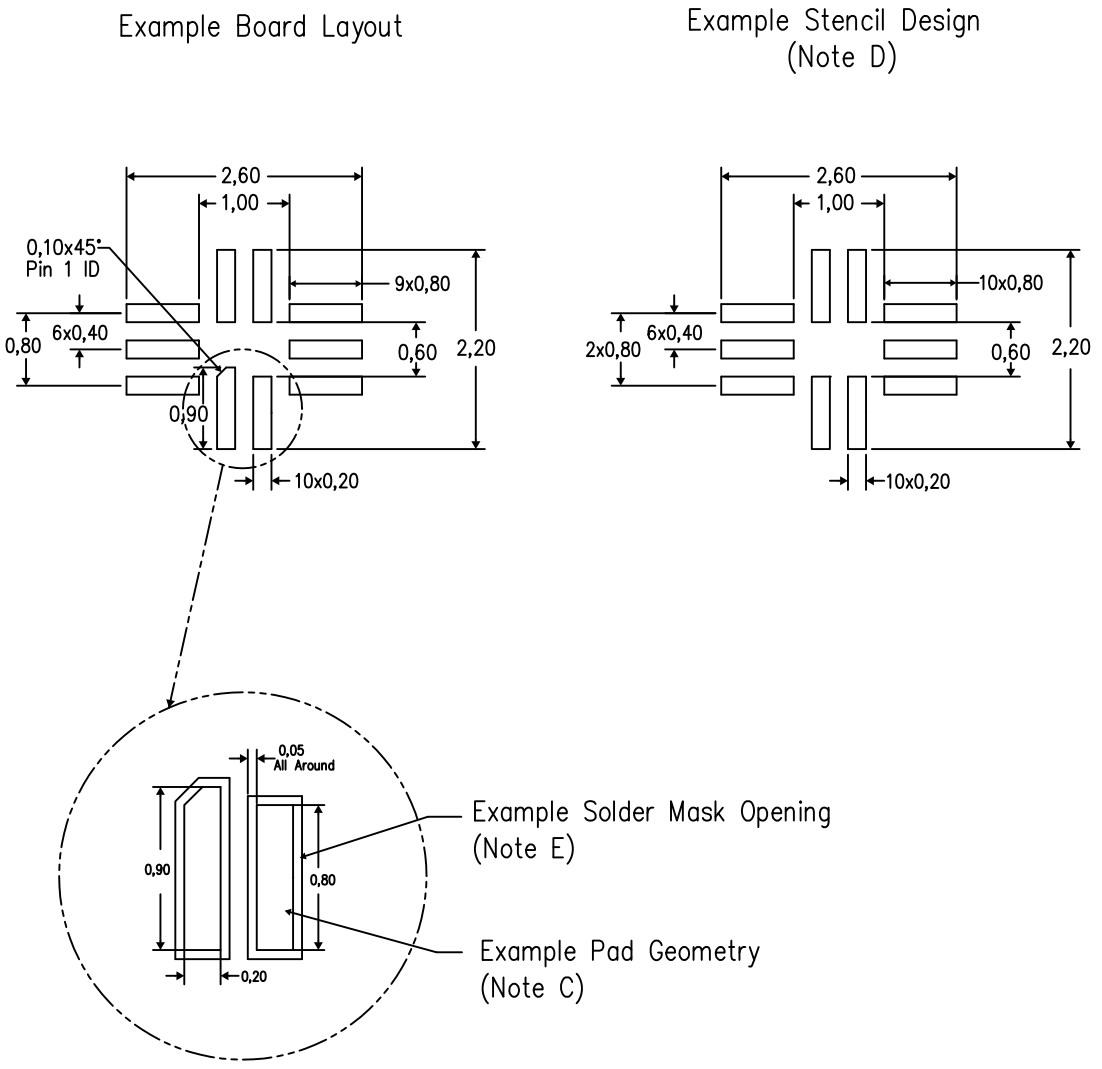
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–lead) package configuration.
D. This package complies to JEDEC MO–288 variation UDEE, except minimum package height.

RSW (R–PUQFN–N10) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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