

SN74AHCT1G00 Single 2-Input Positive-NAND Gate

1 Features

- Operating Range of 4.5 V to 5.5 V
- Maximum t_{pd} of 7.1 ns at 5 V
- Low Power Consumption, 10- μ A Maximum I_{CC}
- ± 8 -mA Output Drive at 5 V
- Inputs Are TTL-Voltage Compatible
- Latch-up Performance Exceeds 250 mA Per JESD 17

2 Applications

- IP Phones
- Notebook PCs
- Printers
- Access Control and Security
- Solar Inverters

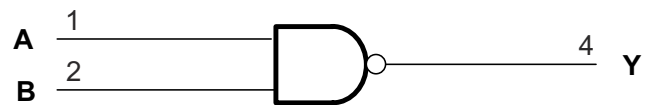
3 Description

The SN74AHCT1G00 device performs the Boolean function $Y = \overline{A} \times \overline{B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

Package Information

| PART NUMBER | PACKAGE ¹ | PACKAGE SIZE ² |
|--------------|----------------------|---------------------------|
| SN74AHCT1G00 | DBV (SOT-23, 5) | 2.8 mm × 2.8 mm |
| | DCK (SC-70, 5) | 2.00 mm × 1.25 mm |

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



Logic Diagram (Positive Logic)

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4 Pin Configuration and Functions

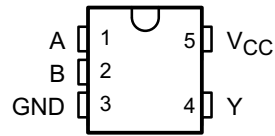


Figure 4-1. DBV or DCK Package 5-PIN SOT-23 OR SC-70 (Top View)

Table 4-1. Pin Functions

| PIN | | TYPE | DESCRIPTION |
|-----|-----------------|------|-------------|
| NO. | NAME | | |
| 1 | A | I | Input A |
| 2 | B | I | Input B |
| 3 | GND | — | Ground Pin |
| 4 | Y | O | Output Y |
| 5 | V _{CC} | — | Power Pin |

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|------------------|---|--|-----------------------|--------|
| V _{CC} | Supply voltage | -0.5 | 7 | V |
| V _I | Input voltage ⁽²⁾ | -0.5 | 7 | V |
| V _O | Output voltage ⁽²⁾ | -0.5 | V _{CC} + 0.5 | V |
| I _{IK} | Input clamp current | V _I < 0 | | -20 mA |
| I _{OK} | Output clamp current | V _O < 0 or V _O > V _{CC} | | -20 mA |
| I _O | Continuous output current | V _O = 0 to V _{CC} | | -25 mA |
| | Continuous current through V _{CC} or GND | -50 | 50 | mA |
| T _{stg} | Storage temperature | -65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

| | | VALUE | UNIT |
|--------------------|-------------------------|--|-------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±1000 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|-----------------|------------------------------------|-----|-----------------|------|
| V _{CC} | Supply voltage | 4.5 | 5.5 | V |
| V _{IH} | High-level input voltage | 2 | | V |
| V _{IL} | Low-level Input voltage | | 0.8 | V |
| V _I | Input voltage | 0 | 5.5 | V |
| V _O | Output voltage | 0 | V _{CC} | V |
| I _{OH} | High-level output current | | -8 | mA |
| I _{OL} | Low-level output current | | 8 | mA |
| Δt/Δv | Input transition rise or fall rate | | 20 | ns/V |
| T _A | Operating free-air temperature | -40 | 125 | °C |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

5.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | SN74AHCT1G00 | | UNIT |
|-------------------------------|--|--------------|-------------|------|
| | | DBV (SOT-23) | DCK (SC-70) | |
| | | 5 PINS | 5 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 278 | 289.2 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 180.5 | 205.8 | |
| R _{θJB} | Junction-to-board thermal resistance | 184.4 | 176.2 | |
| ψ _{JT} | Junction-to-top characterization parameter | 115.4 | 117.6 | |
| ψ _{JB} | Junction-to-board characterization parameter | 183.4 | 175.1 | |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | N/A | N/A | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report ([SPRA953](#)).

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | –40°C to 85°C | | –40°C to 125°C | | UNIT |
|---------------------------------|--|-----------------|-----------------------|------|------|---------------|------|----------------|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | I _{OH} = –50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | V | |
| | I _{OH} = –8 mA | | 3.94 | | 3.8 | | 3.8 | | | |
| V _{OL} | I _{OL} = 50 μA | 4.5 V | | | 0.1 | | 0.1 | 0.1 | V | |
| | I _{OL} = 8 mA | | | 0.36 | | 0.44 | 0.44 | | | |
| I _I | V _I = 5.5 V or GND | 0 V to 5.5 V | | | ±0.1 | | ±1 | ±1 | μA | |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | | | 1 | | 10 | 10 | μA | |
| ΔI _{CC} ⁽¹⁾ | One input at 3.4 V, Other inputs at V _{CC} or GND | 5.5 V | | | 1.35 | | 1.5 | 1.5 | mA | |
| C _i | V _I = V _{CC} or GND | 5 V | | 2 | 10 | | 10 | 10 | pF | |

(1) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

5.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see [Load Circuits and Voltage Waveforms](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | T _A = 25°C | | –40°C to 85°C | | –40°C to 125°C | | UNIT |
|------------------|--------------|-------------|------------------------|-----------------------|-----|---------------|-----|----------------|-----|------|
| | | | | TYP | MAX | MIN | MAX | MIN | MAX | |
| t _{PLH} | A or B | Y | C _L = 15 pF | 5 | 6.2 | 1 | 7.1 | 1 | 8 | ns |
| t _{PHL} | | | | 5 | 6.2 | 1 | 7.1 | 1 | 8 | |
| t _{PLH} | A or B | Y | C _L = 15 pF | 5.5 | 7.9 | 1 | 9 | 1 | 10 | ns |
| t _{PHL} | | | | 5.5 | 7.9 | 1 | 9 | 1 | 10 | |

5.7 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|-----------------|--------------------|------|------|
| C _{pd} | No load, f = 1 MHz | 10.5 | pF |

5.8 Typical Characteristics

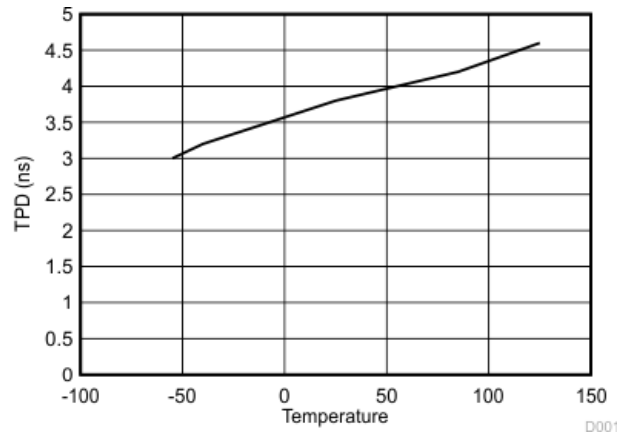
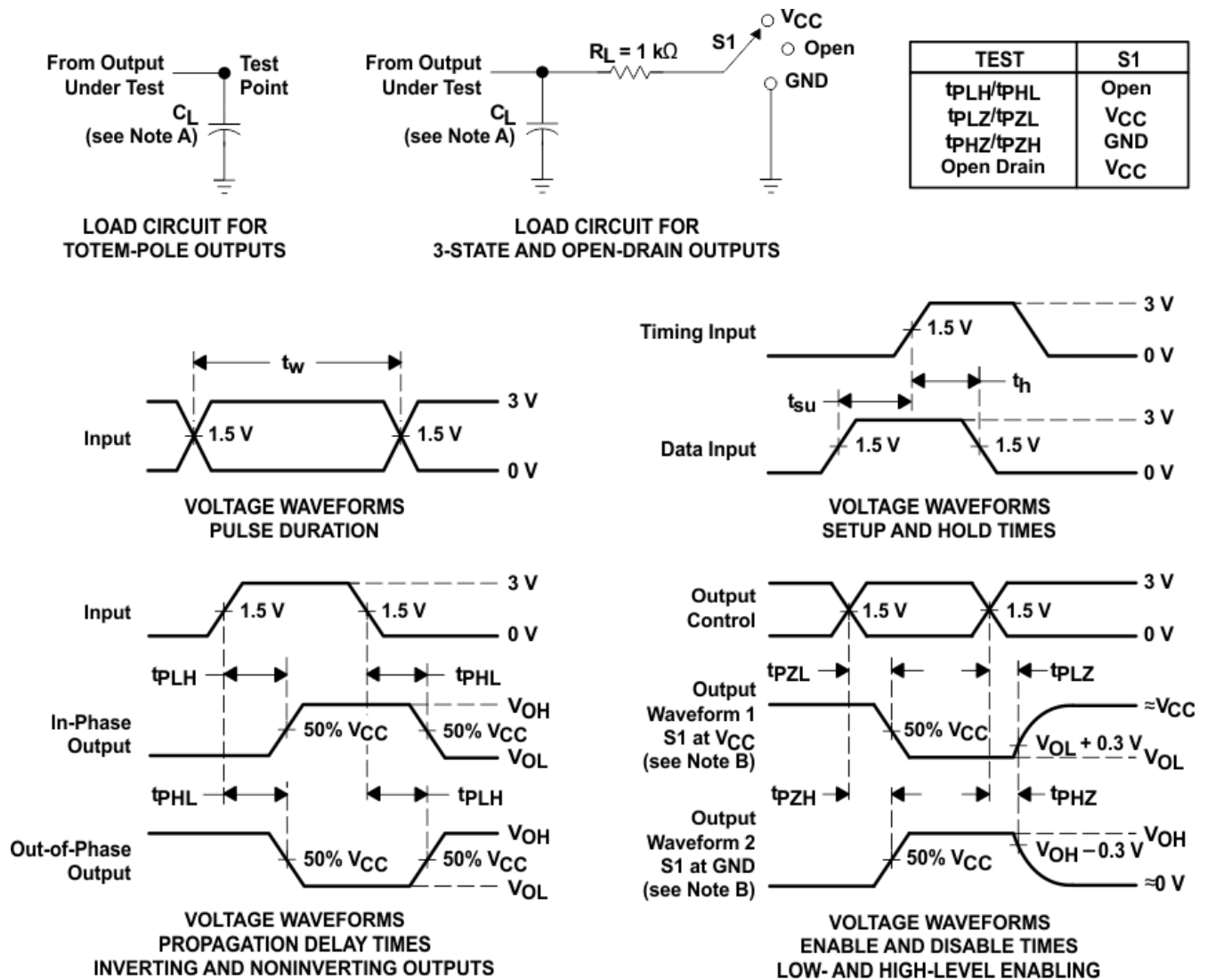


Figure 5-1. TPD vs Temperature

6 Parameter Measurement Information



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuits and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SN74AHCT1G00 device performs the Boolean function $Y = \overline{A \times B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The device has TTL inputs that allow up translation from 3.3 V to 5 V. The inputs are high impedance when $V_{CC} = 0$ V.

7.2 Functional Block Diagram

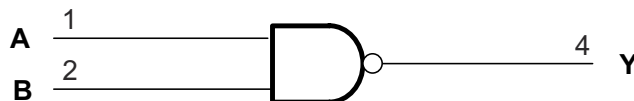


Figure 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

The device is ideal for operating in a 5-V logic system. The low propagation delay allows fast switching and higher speeds of operation. In addition, the low power consumption makes this device a good choice for portable and battery power-sensitive applications.

7.4 Device Functional Modes

Table 7-1. Function Table

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| H | H | L |
| L | X | H |
| X | L | H |

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74AHCT1G00 is a low drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The TTL inputs can accept voltages down to 3.3 V and translate up to 5 V.

8.2 Typical Application

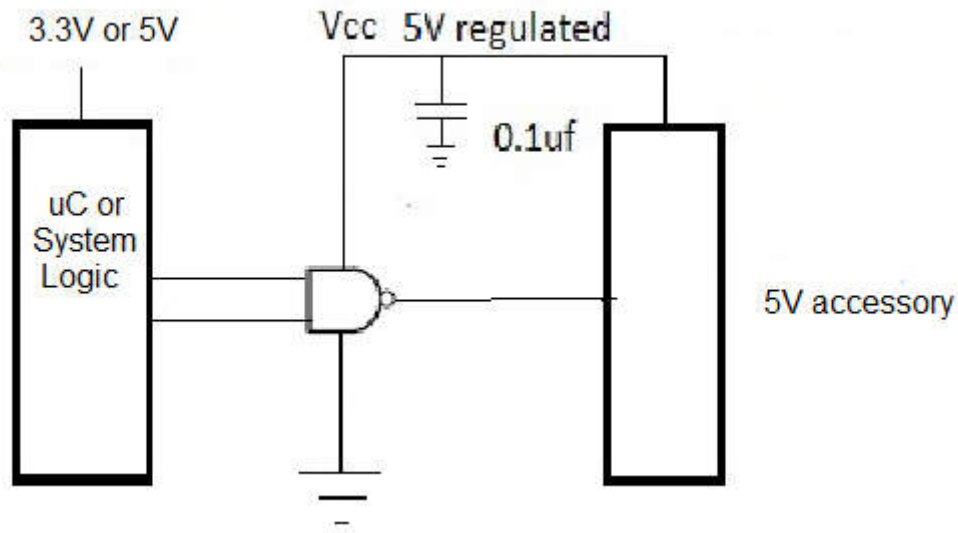


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so consider routing and load conditions to prevent ringing.

8.3 Detailed Design Procedure

- Recommended input conditions:
 - Specified high and low levels. See (V_{IH} and V_{IL}) in [Section 5.3](#).
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC} .
- Recommended output conditions:
 - Load currents should not exceed 25 mA per output and 50 mA total for the part.
 - Outputs should not be pulled above V_{CC} .

8.4 Application Curves

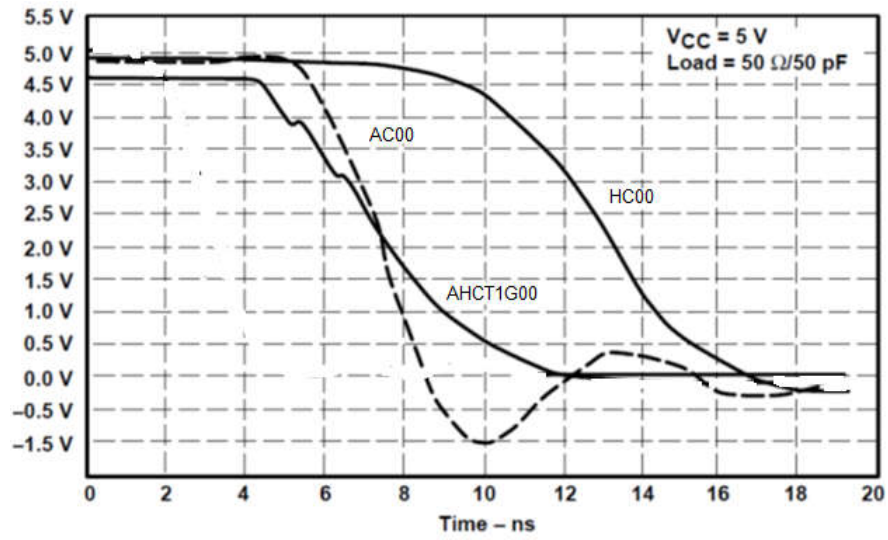


Figure 8-2. Switching Characteristics Comparison

9 Device and Documentation Support

9.1 Documentation Support (Analog)

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [CMOS Power Consumption and Cpd Calculation application note](#)
- Texas Instruments, [Designing With Logic application note](#)
- Texas Instruments, [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices application note](#)
- Texas Instruments, [Implications of Slow or Floating CMOS Inputs application note](#)

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

| Changes from Revision O (October 2023) to Revision P (February 2024) | Page |
|--|-------------|
| • Updated thermal values for DBV package from RθJA = 208.2 to 278, RθJC(top) = 76.1 to 180.5, RθJB = 52.5 to 184.4, ΨJT = 4 to 115.4, ΨJB = 51.8 to 183.4, RθJC(bot) = N/A, all values in °C/W | 5 |

| Changes from Revision N (March 2015) to Revision O (October 2023) | Page |
|--|-------------|
| • Added package size to <i>Package Information</i> table..... | 1 |
| • Updated thermal values for DCK package from RθJA = 287.6 to 289.2, RθJC(top) = 97.7 to 205.8, RθJB = 65 to 176.2, ΨJT = 2 to 117.6, ΨJB = 64.2 to 175.1, RθJC(bot) = N/A, all values in °C/W | 5 |

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|--------------------------|-------------------------|
| 74AHCT1G00DBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | B00G | Samples |
| 74AHCT1G00DCKRE4 | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BA3 | Samples |
| 74AHCT1G00DCKRG4 | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BA3 | Samples |
| SN74AHCT1G00DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU SN | Level-1-260C-UNLIM | -40 to 125 | (B003, B00G, B00J, B00S) | Samples |
| SN74AHCT1G00DCK3 | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Non-Green | SNBI | Level-1-260C-UNLIM | -40 to 85 | BAY | Samples |
| SN74AHCT1G00DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU SN | Level-1-260C-UNLIM | -40 to 125 | (BA3, BAG, BAJ, BAS) | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AHCT1G00 :

- Automotive : [SN74AHCT1G00-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| 74AHCT1G00DBVRG4 | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| 74AHCT1G00DCKRG4 | SC70 | DCK | 5 | 3000 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74AHCT1G00DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74AHCT1G00DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74AHCT1G00DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74AHCT1G00DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| 74AHCT1G00DBVRG4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| 74AHCT1G00DCKRG4 | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74AHCT1G00DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74AHCT1G00DBVR | SOT-23 | DBV | 5 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74AHCT1G00DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74AHCT1G00DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |

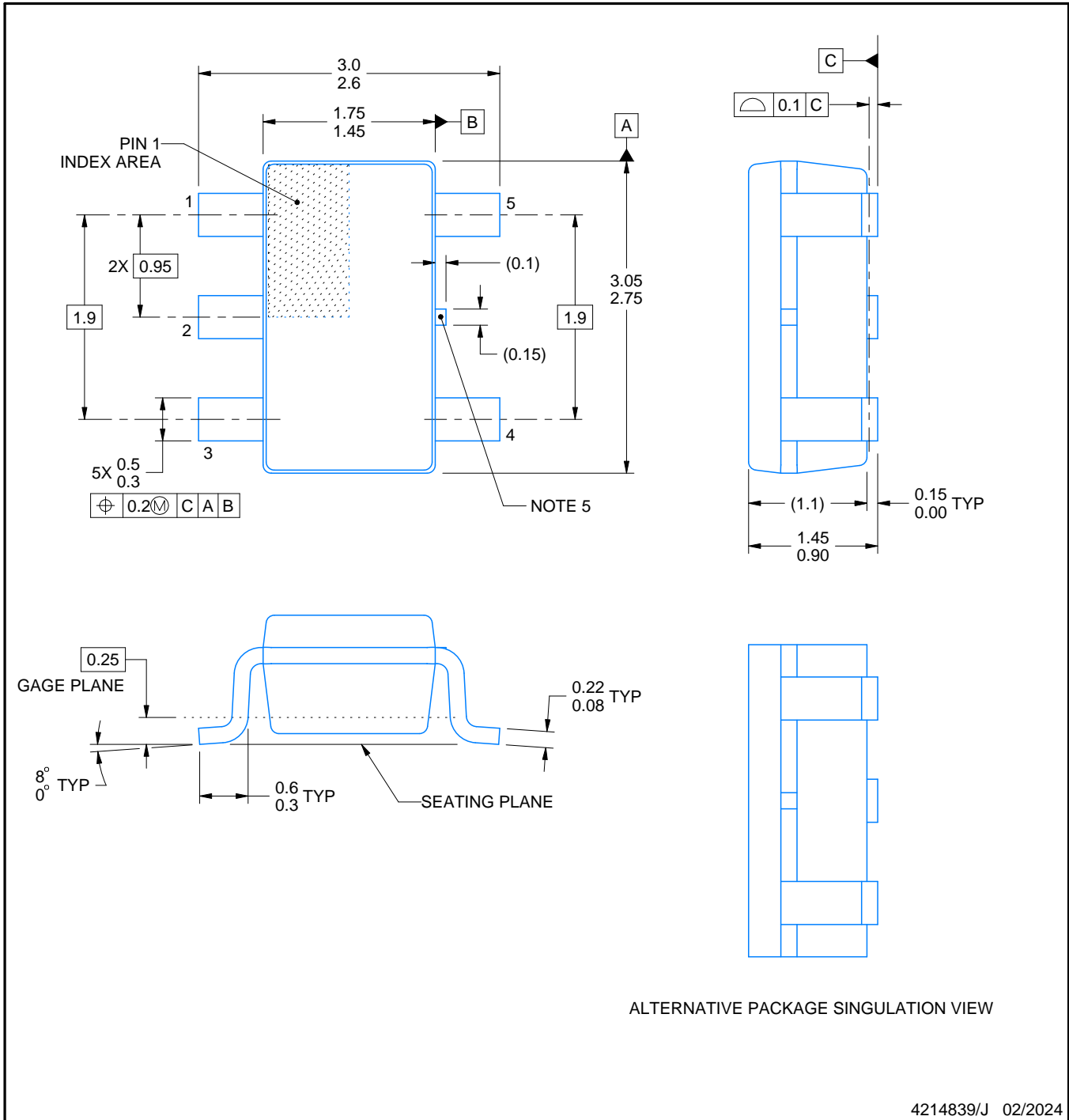
DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

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EXAMPLE BOARD LAYOUT

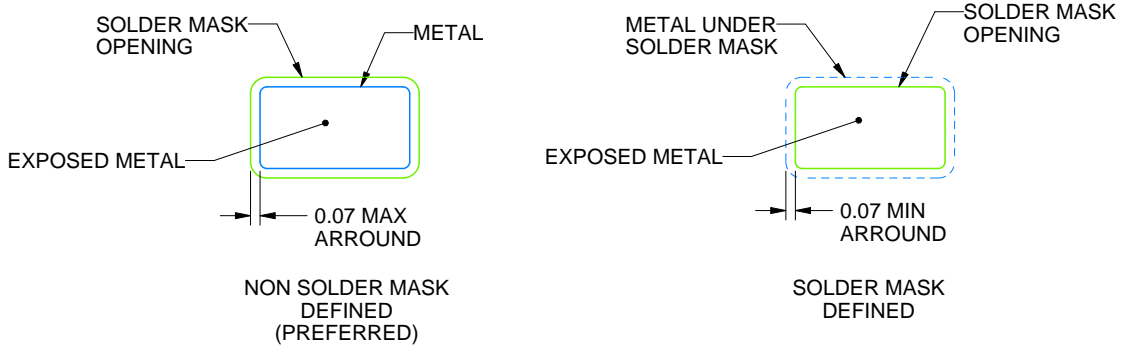
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DCK0005A



PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/D 07/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.

EXAMPLE BOARD LAYOUT

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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NOTES: (continued)

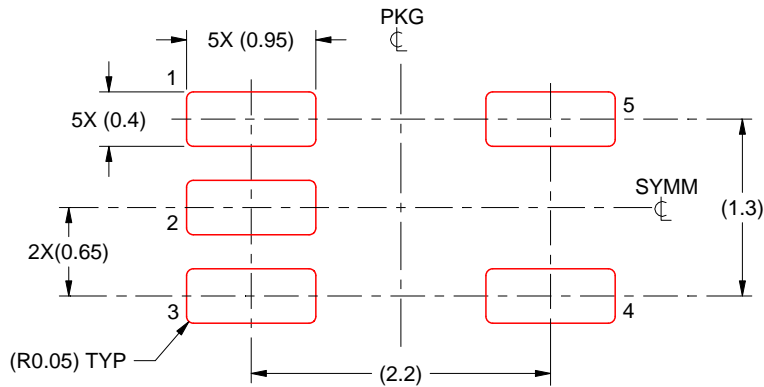
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/D 07/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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