## FEATURES

- **Controlled Baseline**
  - **One Assembly Site**
  - **One Test Site**
  - **One Fabrication Site**
- **Extended Temperature Performance of −55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree** [(1)]
- **Operating Range of 2 V to 5.5 V**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- **Max t_{pd} of 10 ns at 5 V**
- **Low Power Consumption, 10 μA Max I_{CC}**
- **±8 mA Output Drive at 5 V**
- **Schmitt Trigger Action at All Inputs Makes the Circuit Tolerant for Slower Input Rise and Fall Time**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
-
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DBV PACKAGE (TOP VIEW)   **DCK PACKAGE (TOP VIEW)**   **DRL PACKAGE (TOP VIEW)**
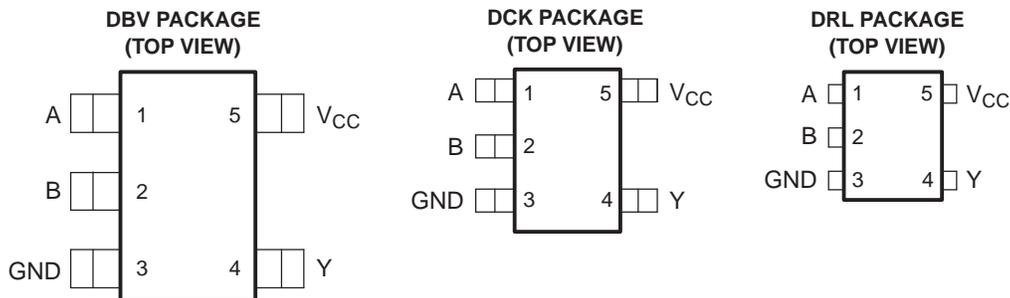
See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

The SN74AHC1G86 is a single 2-input exclusive-OR gate. The device performs the Boolean function $Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$ in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

ORDERING INFORMATION[(1)]

T_A	PACKAGE[(2)]		ORDERABLE PART NUMBER	TOP-SIDE MARKING[(3)]
−55°C to 125°C	SOT (SC-70) - DCK	Reel of 3000	SN74AHC1G86MDCKREP	CGB

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) The actual top-side marking has one additional character that designates the assembly/test site.

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FUNCTION TABLE

INPUTS		OUTPUT
A	**B**	**Y**
L	L	L
L	H	H
H	L	H
H	H	L

EXCLUSIVE-OR LOGIC

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

EXCLUSIVE OR

These are five equivalent exclusive-OR symbols valid for an SN74AHC1G86 gate in positive logic; negation may be shown at any two ports.
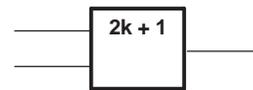
LOGIC-IDENTITY ELEMENT

The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

EVEN-PARITY ELEMENT

The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT

The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

Absolute Maximum Ratings[(1)]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	7	V
V_I	Input voltage range[(2)]		−0.5	7	V
V_O	Output voltage range[(2)]		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		−20	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O = 0$ to V_{CC}		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND	V_{CC} or GND		±50	mA
θ_{JA}	Package thermal impedance[(3)]	DCK package		252	°C/W
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-Level output current	V_{CC} = 2 V		−50	µA
		V_{CC} = 3.3 V ± 0.3 V		−4	mA
		V_{CC} = 5 V ± 0.5 V		−8	
I_{OL}	Low-Level output current	V_{CC} = 2 V		50	µA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20	
T_A	Operating free-air temperature		−55	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25°C$			$T_A = -55°C$ TO $125°C$		UNIT
			MIN	TYP	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50$ μA	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	$I_{OH} = -4$ mA	3 V	2.58			2.48		
	$I_{OH} = -8$ mA	4.5 V	3.94			3.8		
V_{OL}	$I_{OL} = 50$ μA	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	$I_{OL} = 4$ mA	3 V			0.36		0.44	
	$I_{OL} = 8$ mA	4.5 V			0.36		0.44	
I_I	$V_I = 5.5$ V or GND	0 V to 5.5 V			±0.1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, $_O = 0$	5.5 V			1		10	μA
C_i	$V_I = V_{CC}$ or GND	5 V		4	10		10	pF

Switching Characteristics

over operating free-air temperature range, $V_{CC} = 3.3 \pm 0.3$ V (unless otherwise noted) (see Figure 1)

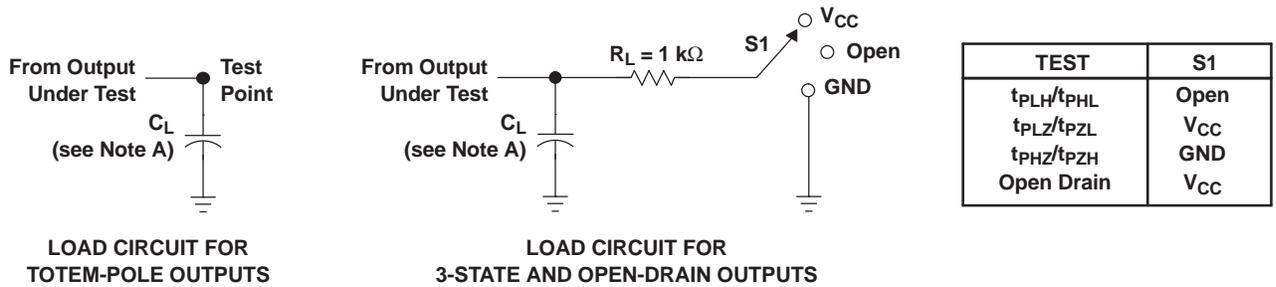| PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25°C$			$T_A = -55°C$ TO $125°C$		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A or B	Y	$C_L = 50$ pF		9.5	14.5	1	16.5	ns
t_{PHL}					9.5	14.5	1	16.5	ns

Switching Characteristics

over operating free-air temperature range, $V_{CC} = 5 \pm 0.5$ V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25°C$			$T_A = -55°C$ TO $125°C$		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A or B	Y	$C_L = 50$ pF		6.3	8.8	1	10	ns
t_{PHL}					6.3	8.8	1	10	

Operating Characteristics

$V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, f = 1 MHz	18	pF

Product Folder Link(s): *SN74AHC1G86-EP*

PARAMETER MEASUREMENT INFORMATION

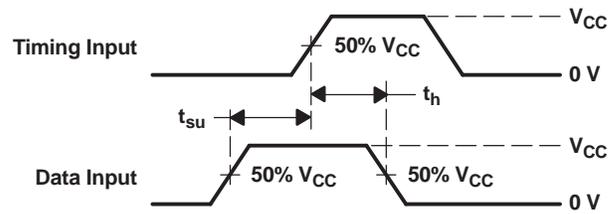| TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

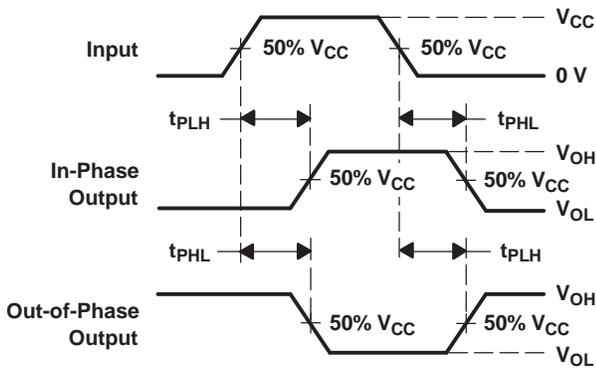LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS
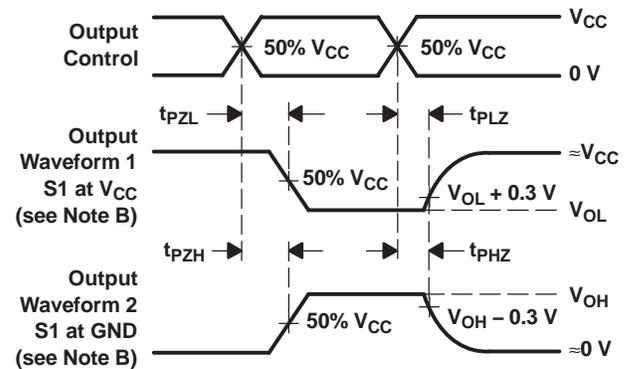
LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS
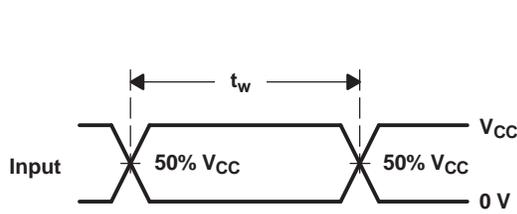
VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
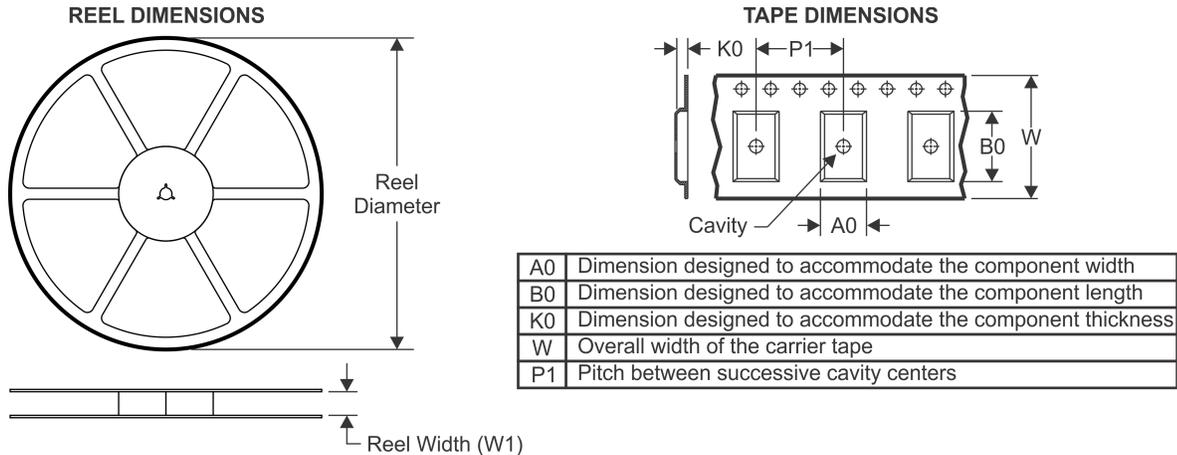INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
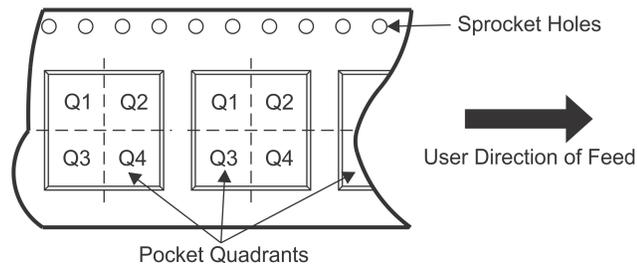ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
       Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
   D. The outputs are measured one at a time, with one input transition per measurement.
   E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

|	
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC1G86MDCKREP	SC70	DCK	5	3000	180.0	8.4	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS
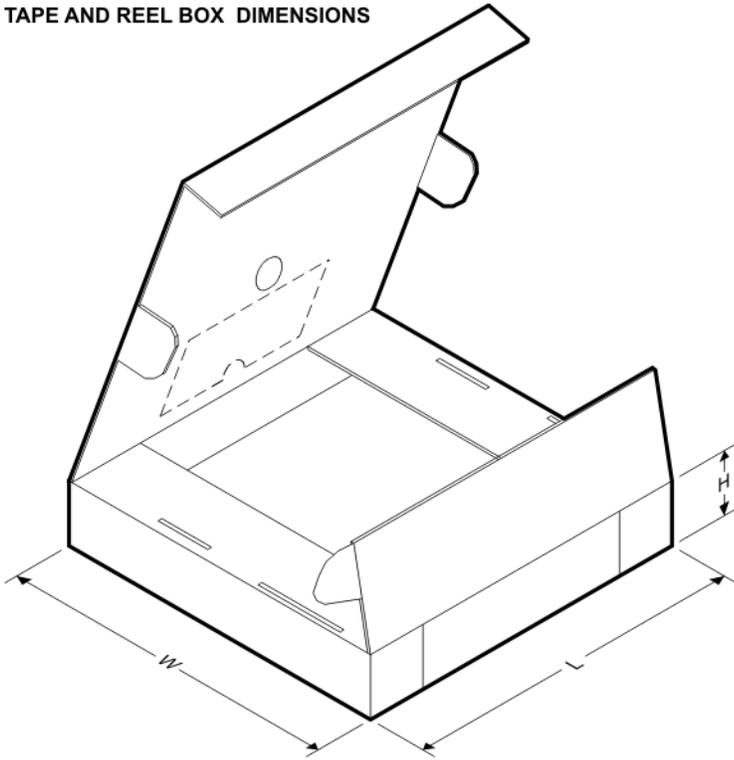
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC1G86MDCKREP	SC70	DCK	5	3000	202.0	201.0	28.0

PIN 1
INDEX AREA

2.4
1.8

1.4
1.1

B

A

1

5

2X 0.65

1.3

2

NOTE 4

(0.15)

(0.1)

1.3

2.15
1.85

3

4

5X 0.33
0.15

⊕ 0.1Ⓜ C A B
NOTE 5

C

◁ 0.1 C

1.1 MAX

(0.9)

0.1
0.0 TYP

0.15

GAGE PLANE

8°
0° TYP

0.46 TYP
0.26

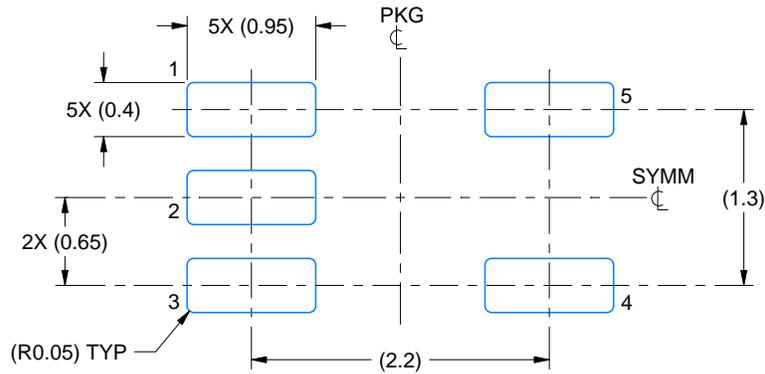0.22 TYP
0.08

SEATING PLANE
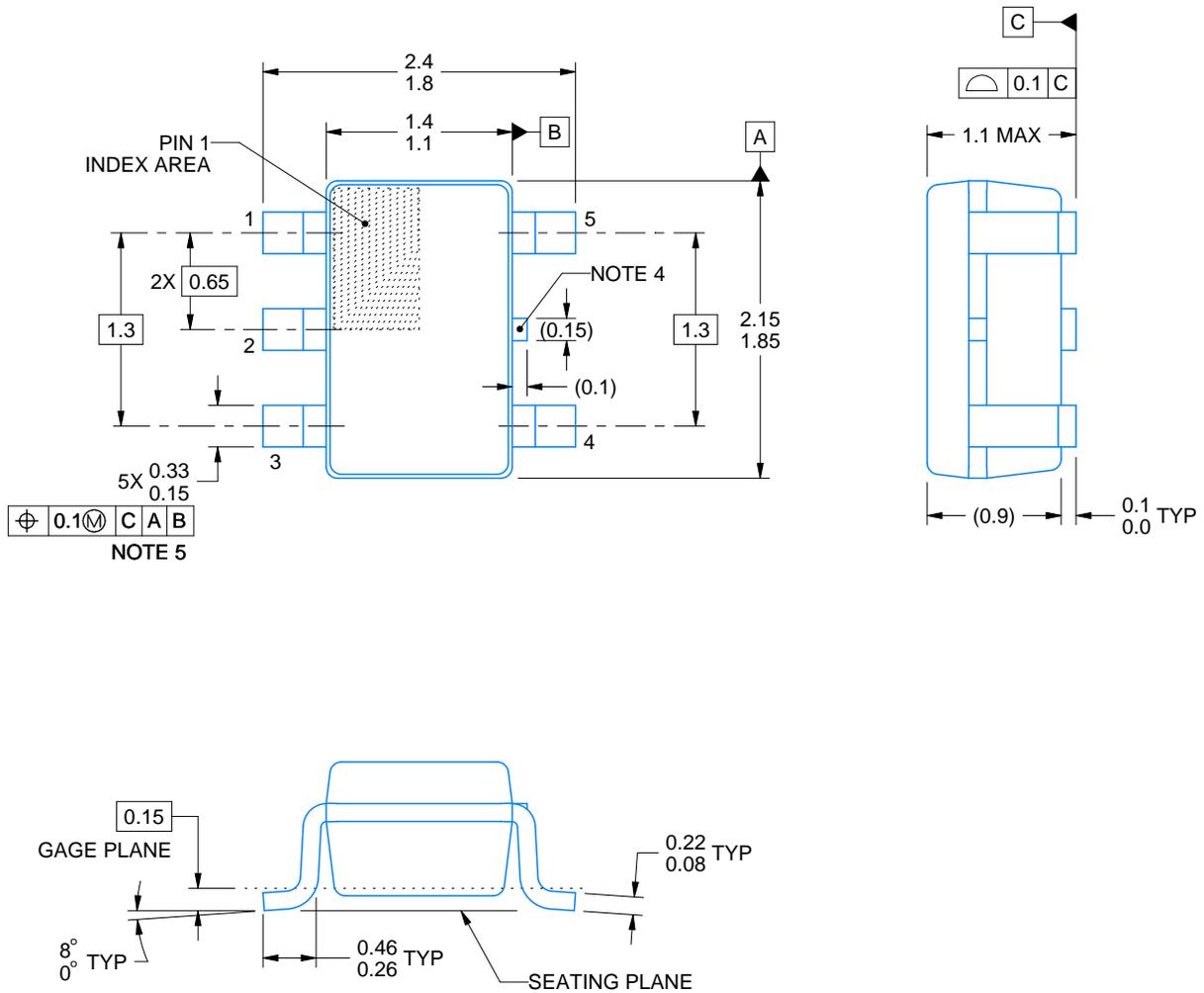
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.

DCK0005A

5X (0.95)
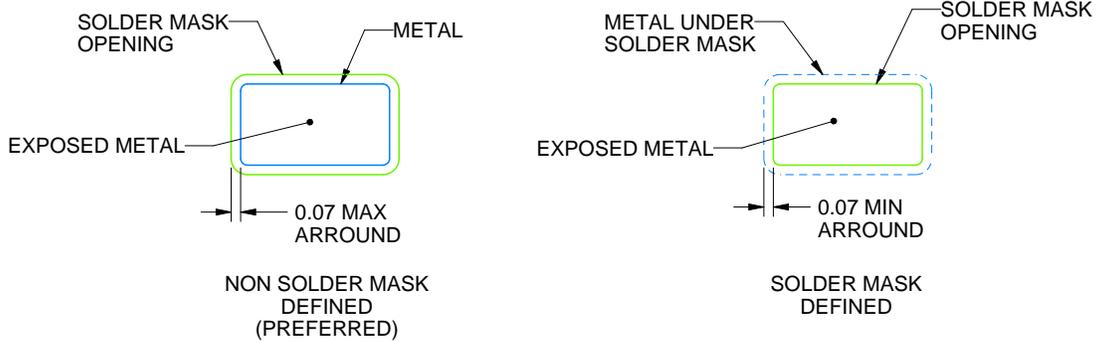
PKG
₵

1

5X (0.4)

5

2

SYMM
₵

(1.3)

2X (0.65)

3

4

(R0.05) TYP

(2.2)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

EXPOSED METAL

0.07 MAX
ARROUND

0.07 MIN
ARROUND

NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED
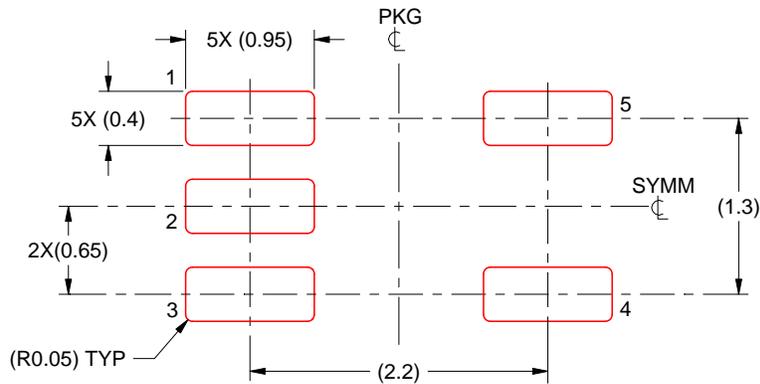
SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

PKG
℄

5X (0.95)

1

5X (0.4)

2

2X(0.65)

3

5

SYMM
℄

(1.3)

4

(R0.05) TYP

(2.2)

SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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