

DisplayPort to TMDS Translator

FEATURES

- DisplayPort Physical Layer Input Port to TMDS Physical Layer Output Port
- Integrated TMDS Level Translator With Receiver Equalization
- Supports Data Rates up to 2.5 Gbps
- Integrated I²C Logic Block for DVI / HDMI Connector Recognition
- Integrated Active I²C Buffer
- Enhanced ESD: 12 kV on all Pins
- Enhanced Commercial Temperature Range: 0°C to 85°C
- 36 Pin 6 × 6 QFN Package

APPLICATIONS

- Personal Computer Market
 - DP/TMDS Hardware Key (Dongle)
 - Desktop PC
 - Notebook PC
 - Docking Station
 - Standalone Video Card

DESCRIPTION

The SN75DP129 is a Dual-Mode DisplayPort input to Transition-Minimized Differential Signaling (TMDS) output. The TMDS output has a built-in level translator, compliant with [Digital Visual Interface 1.0 \(DVI\)](#) and [High Definition Multimedia Interface 1.3 \(HDMI\)](#) standards. The SN75DP129 is specified up to a maximum data rate of 2.5 Gbps, supporting resolutions greater than 1920 x 1200 or HDTV 12-bit color depth at 1080p (progressive scan).

An integrated Active I²C buffer isolates the capacitive loading of the source system from that of the sink and interconnecting cable. This isolation improves overall signal integrity of the system and provides greater design margin within the source system for DVI / HDMI compliance testing.

A logic block was designed into the SN75DP129 to assist with TMDS connector identification. Through the use of the I²C_EN pin, this logic block can be enabled to indicate the translated port is an HDMI port; therefore legally supporting HDMI content.

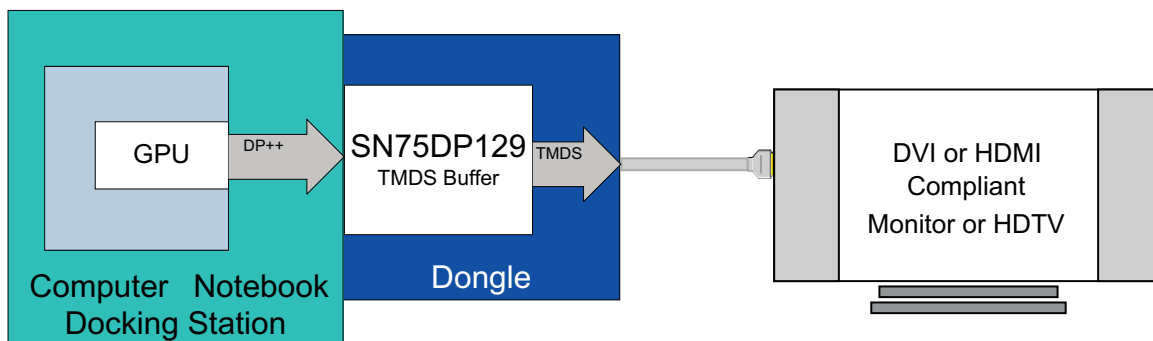


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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TYPICAL APPLICATION



GPU—Graphics Processing Unit

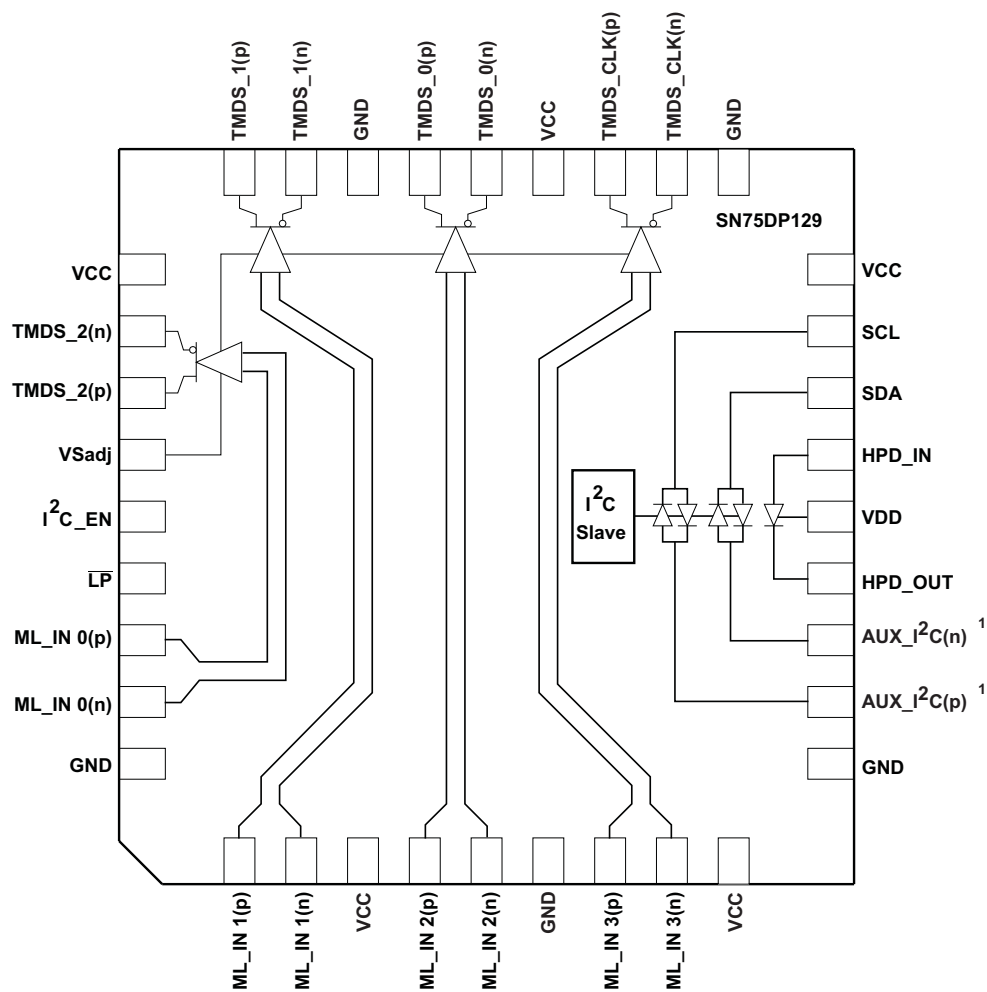
DP++—Dual-Mode DisplayPort

TMDS—Transition-Minimized Differential Signaling

DVI—Digital Visual Interface

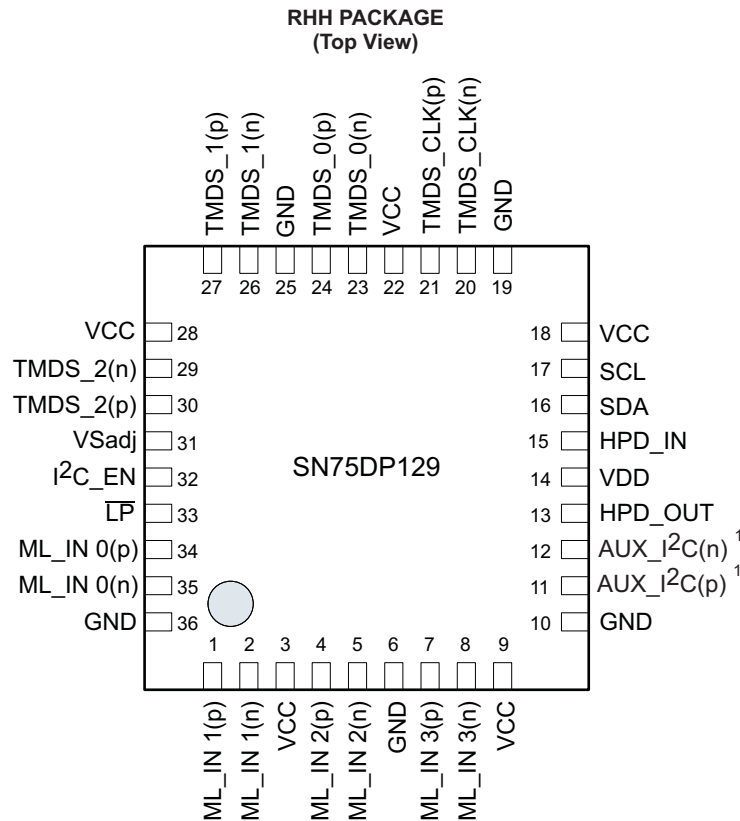
HDMI—High Definition Multimedia Interface

INTERNAL DATA CONNECTION DIAGRAM



(1) I²C bus data (n-SDA) and clock (p-SCL) lines.

PIN CONFIGURATION



(1) I²C bus data (n-SDA) and clock (p-SCL) lines.

TERMINAL FUNCTIONS

| TERMINAL | | I/O | DESCRIPTION | TYPE |
|------------------------|--------------------|-----|---|----------------------|
| NAME | NO. ⁽¹⁾ | | | |
| AUX_I2C ⁽²⁾ | 11(p), 12(n) | I/O | Source Side Bidirectional DisplayPort Auxiliary Data Line | DDC LINK (Source) |
| GND | 6, 10, 19, 25, 36 | | Ground | Ground |
| HPD_IN | 15 | I | Hot Plug Detect (HPD) Input | Hot Plug Detect |
| HPD_OUT | 13 | O | Hot Plug Detect (HPD) Output | Hot Plug Detect |
| I2C_EN | 32 | I | Internal I2C register enable, used for HDMI / DVI connector differentiation | Control |
| LP | 33 | I | Low Power Select Bar | Control |
| ML_IN 0 | 34(p), 35(n) | I | DisplayPort Main Link Channel 0 Differential Input | Main Link Input Pins |
| ML_IN 1 | 1(p), 2(n) | I | DisplayPort Main Link Channel 1 Differential Input | Main Link Input Pins |
| ML_IN 2 | 4(p), 5(n) | I | DisplayPort Main Link Channel 2 Differential Input | Main Link Input Pins |
| ML_IN 3 | 7(p), 8(n) | I | DisplayPort Main Link Channel 3 Differential Input | Main Link Input Pins |
| TMD5_2 | 30(p), 29(n) | O | TMD5 Data 2 Differential Output | Main Link Output |
| TMD5_1 | 27(p), 26(n) | O | TMD5 Data 1 Differential Output | Main Link Output |
| TMD5_0 | 24(p), 23(n) | O | TMD5 Data 0 Differential Output | Main Link Output |
| TMD5_CLK | 21(p), 20(n) | O | TMD5 Data Clock Differential Output | Main Link Output |
| SCL | 17 | I/O | TMD5 Port Bidirectional I2C Clock Line | DDC Link (Sink) |
| SDA | 16 | I/O | TMD5 Port Bidirectional I2C Data Line | DDC Link (Sink) |
| VCC | 3, 9, 18, 22, 28 | | 3.3 V Supply | Voltage Supply |

(1) (p) Positive; (n) Negative

(2) I²C bus data (n-SDA) and clock (p-SCL) lines.

TERMINAL FUNCTIONS (continued)

| TERMINAL | | I/O | DESCRIPTION | TYPE |
|----------|---------|-----|--------------------------------------|----------------|
| NAME | NO. (1) | | | |
| VDD | 14 | | HPD Supply | Voltage Supply |
| VSadj | 31 | I | TMDS-Compliant Voltage Swing Control | Reference |

Input/Output Equivalent Circuits

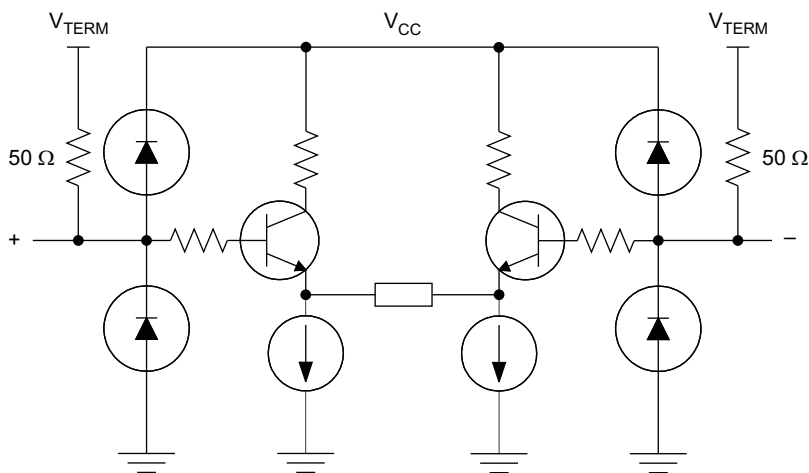


Figure 1. DisplayPort Input Stage

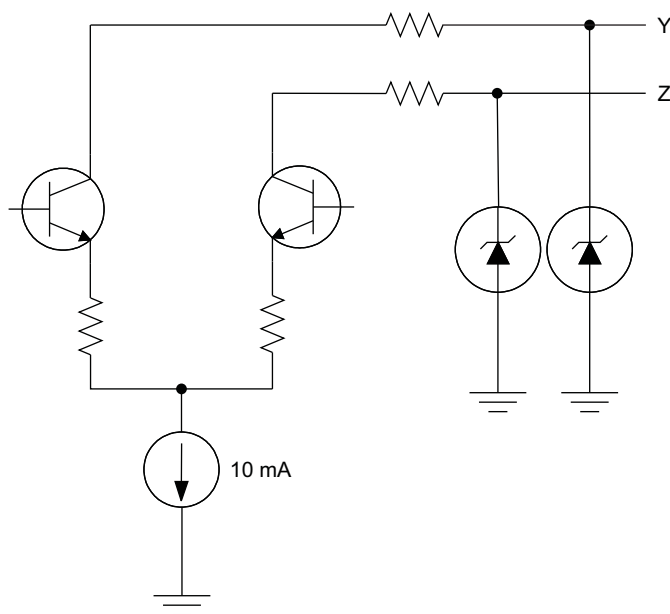


Figure 2. TMDS Output Stage

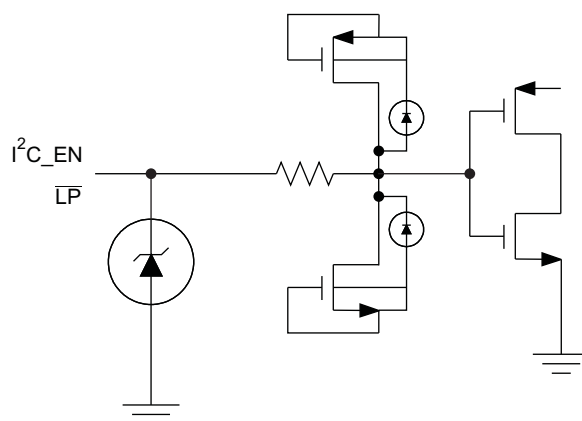


Figure 3. HPD and Control Input Stage

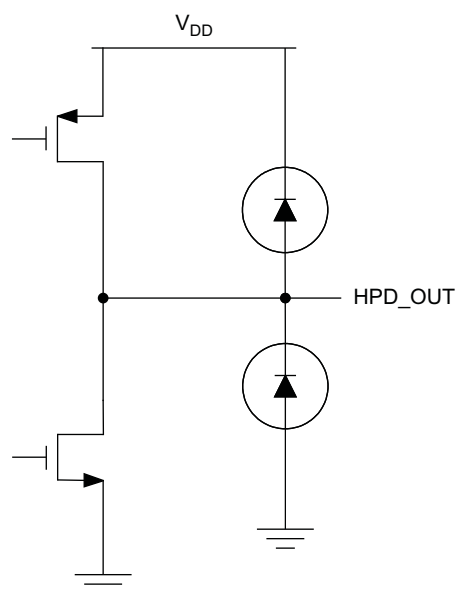


Figure 4. HPD Output Stage

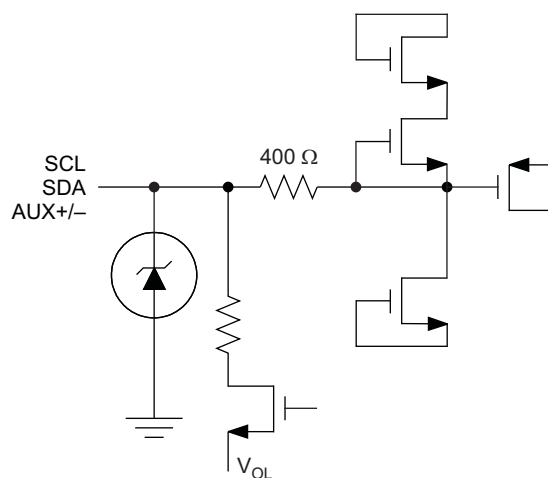


Figure 5. I²C Input and Output Stage

Table 1. Control Pin Lookup Table⁽¹⁾

| SIGNAL | LEVEL | STATE | DESCRIPTION |
|---------------------|---------|-------------------------|--|
| LP | H | Normal Mode | Normal operational mode for device |
| | L | Low Power Mode | Device is forced into a Low Power state causing the outputs to go to a high impedance state. All other inputs are ignored. |
| I ² C_EN | H | HDMI | Internal I ² C register is active and readable, indicating the connector in use is HDMI-compliant. |
| | L | DVI | Internal I ² C register is disabled and unreadable, indicating the connector in use is DVI-compliant. |
| VS _{adj} | 4.65 kΩ | Compliant Voltage Swing | Driver output voltage swing precision control to aid with system compliance. |

(1) (H) Logic High; (L) Logic Low

ORDERING INFORMATION⁽¹⁾

| PART NUMBER | PART MARKING | PACKAGE |
|---------------|--------------|-------------------------|
| SN75DP129RHHR | DP129 | 36-pin QFN Reel (large) |
| SN75DP129RHHT | DP129 | 36-pin QFN Reel (small) |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | VALUE | UNIT |
|-------------------------------------|---|-------------------------------|------|
| Supply voltage range ⁽²⁾ | VCC | –0.3 to 3.6 | V |
| Supply voltage range | VDD | –0.3 to 3.6 | V |
| Voltage range | Main link I/O (ML_IN x, DP_SINK x) differential voltage | 1.5 | V |
| | TMDS I/O | –0.3 to 4 | V |
| | HPD I/O | –0.3 to 5.5 | V |
| | Auxiliary I/O | –0.3 to 5.5 | V |
| | Control I/O | –0.3 to 5.5 | V |
| Electrostatic discharge | Human body model ⁽³⁾ | ±12000 | V |
| | Charged-device model ⁽⁴⁾ | ±1000 | V |
| | Machine model ⁽⁵⁾ | ±200 | V |
| Continuous power dissipation | | See Dissipation Ratings Table | |

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to network ground terminal.
- (3) Tested in accordance with JEDEC Standard 22, Test Method A114-B
- (4) Tested in accordance with JEDEC Standard 22, Test Method C101-A
- (5) Tested in accordance with JEDEC Standard 22, Test Method A115-A

DISSIPATION RATINGS

| PACKAGE | PCB JEDEC STANDARD | T _A ≤ 25°C | DERATING FACTOR ⁽¹⁾ ABOVE T _A = 25°C | T _A = 85°C POWER RATING |
|------------------|--------------------|-----------------------|---|---------------------------------------|
| 36-pin QFN (RHH) | Low-K | 1398 mW | 13.98 mW/°C | 559 mW |
| | High-K | 2941 mW | 29.41 mW/°C | 1176 mW |

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|-----|---------------------|-----|------|
| $R_{\theta JB}$ Junction-to-board thermal resistance | | | 9.44 ⁽¹⁾ | | °C/W |
| $R_{\theta JC}$ Junction-to-case thermal resistance | | | 24.74 | | °C/W |
| P_D Device power dissipation ⁽²⁾ | $\overline{LP} = 3.3\text{ V}$, ML: $V_{ID} = 500\text{ mV}$, 2.5 Gbps PRBS; I^2C : $V_{ID} = 3.3\text{ V}$, 100 Kbps PRBS; HPD = 5 V | | 380 | 490 | mW |
| P_{SD} Device power dissipation under low power | $\overline{LP} = 0\text{ V}$ | | 5 | 20 | μW |

(1) The maximum rating is simulated under 3.6 V V_{CC} and V_{DD} unless otherwise noted.

(2) Power dissipation is the sum of the power consumption from the V_{CC} and V_{DD} pins, plus the 132 mW of power from the AVCC (Receiver Termination Supply).

RECOMMENDED OPERATING CONDITIONS

| | MIN | NOM | MAX | UNIT |
|--|------|-----|------|------|
| V_{CC} Supply voltage | 3 | 3.3 | 3.6 | V |
| V_{DD} Supply voltage | 1.65 | | 3.6 | V |
| T_A Operating free-air temperature | 0 | | 85 | °C |
| MAIN LINK DIFFERENTIAL INPUT PINS | | | | |
| V_{ID} Peak-to-peak input differential voltage | 0.15 | | 1.40 | V |
| d_R Data rate | | | 2.5 | Gbps |
| TMDS DIFFERENTIAL OUTPUT PINS | | | | |
| AV_{CC} TMDS output termination voltage | 3 | 3.3 | 3.6 | V |
| d_R Data rate | | | 2.5 | Gbps |
| R_t Termination resistance | 45 | 50 | 55 | Ω |
| AUXILIARY AND I²C PINS | | | | |
| V_I Input voltage | 0 | | 5.5 | V |
| $d_{R(I2C)}$ I2C data rate | | | 100 | kHz |
| HPD AND CONTROL PINS | | | | |
| V_{IH} High-level input voltage | 2 | | 5.5 | V |
| V_{IL} Low-level input voltage | 0 | | 0.8 | V |

Device Power

The SN75DP129 is designed to operate from one or two supply voltages, depending on the implementation of the integrated Hot Plug Detect (HPD) level translator. The TMDS level translator is powered from a single 3.3-V supply. The HPD translator is powered using the V_{DD} pin and its voltage can range from 1.8 V to 3.3 V. This voltage determines the HIGH-level output voltage of the HPD_OUT pin.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------|--|-----|-----|-----|------|
| I_{CC} Supply current | $LP = 3.6\text{ V}$, $V_{CC} = V_{DD}$, ML: $V_{ID} = 500\text{ mV}$, 2.7 Gbps PRBS AUX: $V_I = 3.3\text{ V}$, 100 kHz PRBS HPD: HPD_IN = 5 V | 50 | 75 | 112 | mA |
| I_{DD} Supply current | | | 1 | 2 | mA |
| I_{SD} Shutdown current | $\overline{LP} = 0\text{ V}$ | | 1 | 5 | μA |

Hot Plug and Cable Adapter Detect

The SN75DP129 has a built-in level shifter for the HPD outputs. The output voltage level of the HPD pin is defined by the voltage level of the VDD pin.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------|--|------|-----|-----|---------|
| $V_{OH3.3}$ | High-level output voltage $I_{OH} = -100 \mu A$, $V_{DD \times 1} = 3.3 V$ | 3 | | 3.3 | V |
| $V_{OH2.5}$ | | 2.25 | | 2.5 | V |
| $V_{OH1.8}$ | | 1.62 | | 1.8 | V |
| V_{OL} | Low-level output voltage $I_{OH} = 100 \mu A$ | 0 | | 0.4 | V |
| I_H | High-level input current $V_{IH} = 2.0 V$, $V_{DD} = 3.6 V$ | -10 | | 10 | μA |
| I_L | Low-level input current $V_{IL} = 0.8 V$, $V_{DD} = 3.6 V$ | -10 | | 10 | μA |

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------|---------------------------------------|-----|-----|-----|------|
| $t_{PD(HPD)}$ | Propagation delay $V_{DD} = 3.6 V$ | 5 | | 30 | ns |

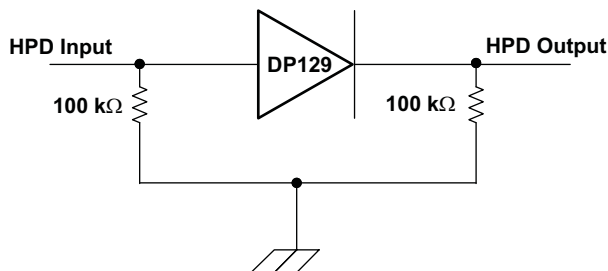


Figure 6. HPD Test Circuit

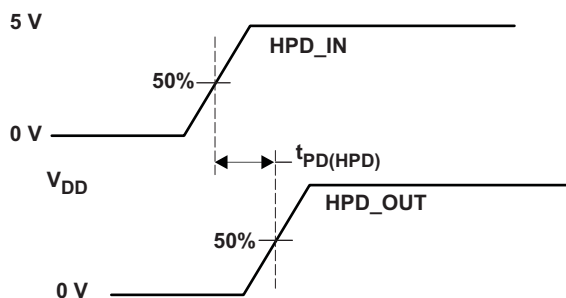


Figure 7. HPD Timing Diagram

AUX / I²C Pins

The SN75DP129 utilizes an active I²C repeater. The repeater isolates the parasitic effects of the system to aid with system level compliance.

In addition to the I²C repeater, the SN75DP129 supports the connector detection I²C register. This register is enabled using the I2C_EN pin. When active, an internal memory register is readable using the AUX_I²C pins. This I²C register block functionality is described in the [APPLICATION INFORMATION](#) section.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|--------------------------|-------------------------------|---|------|-----|-----|---------------|
| I_L | Low input current | | $V_{CC} = 3.6\text{ V}$, $V_I = 0\text{ V}$ | -10 | | 10 | μA |
| $I_{IKG(AUX)}$ | Input leakage current | AUX_I ² C pins | $V_{CC} = 3.6\text{ V}$, $V_I = 3.6\text{ V}$ | -10 | | 10 | μA |
| $C_{IO(AUX)}$ | Input/output capacitance | AUX_I ² C pins | DC bias = 1.65 V, AC = 2.1 V _{p-p} , f = 100 kHz | | | 15 | pF |
| $V_{IH(AUX)}$ | High-level input voltage | AUX_I ² C pins | | 1.6 | | 5.5 | V |
| $V_{IL(AUX)}$ | Low-level input voltage | AUX_I ² C pins | | -0.2 | | 0.4 | V |
| $V_{OL(AUX)}$ | Low-level output voltage | AUX_I ² C pins | $I_O = 4\text{ mA}$ | 0.5 | | 0.6 | V |
| $I_{IKG(I2C)}$ | Input leakage current | I ² C SDA/SCL pins | $V_{CC} = 3.6\text{ V}$, $V_I = 4.95\text{ V}$ | -10 | | 10 | μA |
| $C_{IO(I2C)}$ | Input/output capacitance | I ² C SDA/SCL pins | DC bias = 2.5 V, AC = 3.5 V _{p-p} , f = 100 kHz | | | 15 | pF |
| $V_{IH(I2C)}$ | High-level input voltage | I ² C SDA/SCL pins | | 2.1 | | 5.5 | V |
| $V_{IL(I2C)}$ | Low-level input voltage | I ² C SDA/SCL pins | | -0.2 | | 1.5 | V |
| $V_{OL(I2C)}$ | Low-level output voltage | I ² C SDA/SCL pins | $I_O = 4\text{ mA}$ | | | 0.2 | V |

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------|--|-----------------|-----|-----|-----|---------------|
| t_{PLH1} | Propagation delay time, low to high | Source to Sink | 204 | | 459 | ns |
| t_{PHL1} | Propagation delay time, high to low | Source to Sink | 35 | | 200 | ns |
| t_{PLH2} | Propagation delay time, low to high | Sink to Source | 80 | | 251 | ns |
| t_{PHL2} | Propagation delay time, high to low | Sink to Source | 35 | | 200 | ns |
| t_{f1} | Output signal fall time | Sink Side | 20 | | 72 | ns |
| t_{f2} | Output signal fall time | Source Side | 20 | | 72 | ns |
| f_{SCL} | SCL clock frequency for internal register | Source Side | | | 100 | kHz |
| $t_{W(L)}$ | Clock LOW period for I ² C register | Source Side | 4.7 | | | μs |
| $t_{W(H)}$ | Clock HIGH period for internal register | Source Side | 4.0 | | | μs |
| t_{SU1} | Internal register setup time, SDA to SCL | Source Side | 250 | | | ns |
| $t_{h(1)}$ | Internal register hold time, SCL to SDA | Source Side | 0 | | | μs |
| $t_{(buf)}$ | Internal register bus free time between STOP and START | Source Side | 4.7 | | | μs |
| $t_{su(2)}$ | Internal register setup time, SCL to START | Source Side | 4.7 | | | μs |
| $t_{h(2)}$ | Internal register hold time, START to SCL | Source Side | 4.0 | | | μs |
| $t_{su(3)}$ | Internal register hold time, SCL to STOP | Source Side | 4.0 | | | μs |

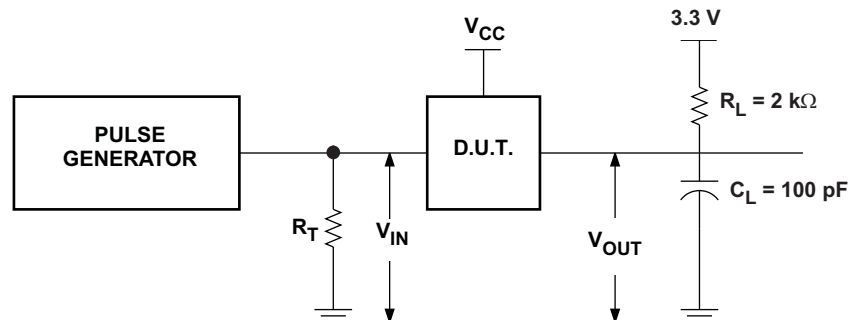


Figure 8. Source Side Test Circuit (AUX_I²C)

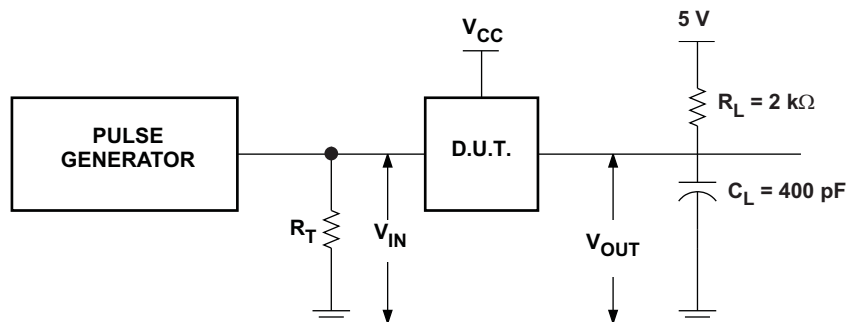


Figure 9. Sink Side Test Circuit (SCL, SDA)

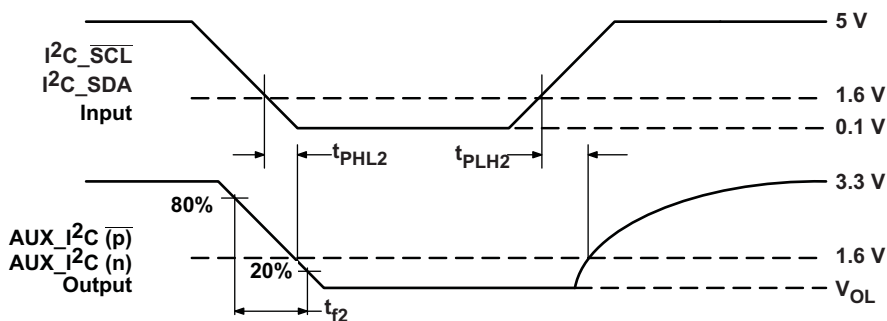


Figure 10. Source Side Output AC Measurements

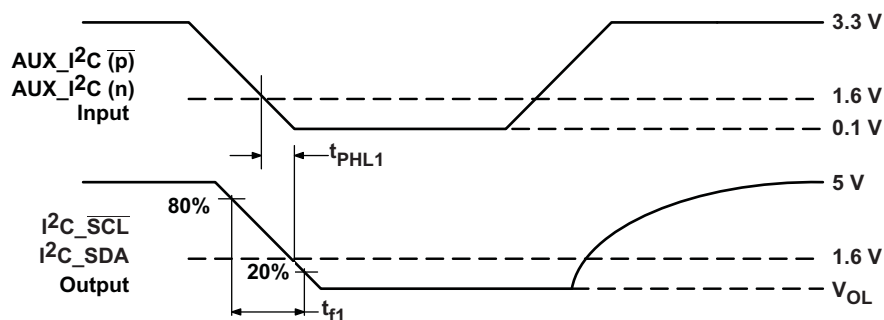


Figure 11. Sink Side Output AC Measurements

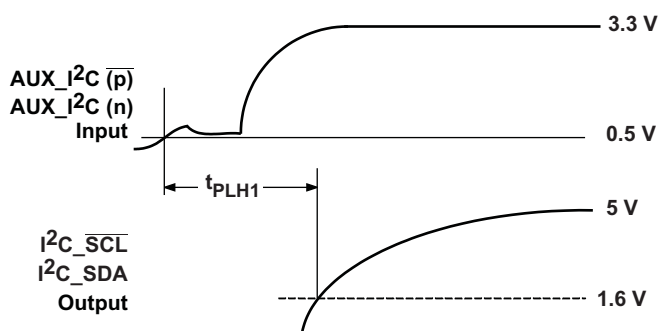


Figure 12. Sink Side Output AC Measurements (continued)

TMDS and Main Link Pins

The main link inputs are designed to be compliant with the DisplayPort 1.1 specification. The TMDS outputs of the SN75DP129 are designed to be compliant with the Digital Visual Interface 1.0 (DVI) and High Definition Multimedia Interface 1.3 (HDMI) specifications. The differential output voltage swing can be fine-tuned with the VSadj (TMDS-compliant Voltage Swing Control) resistor.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|----------|-----|----------|------|
| V _{OH} Single-ended HIGH level output voltage | AVCC = 3.3 V, R _T = 50 Ω | AVCC–10 | | AVCC+10 | mV |
| V _{OL} Single-ended LOW level output voltage | | AVCC–600 | | AVCC–400 | mV |
| V _{SWING} Single-ended output voltage swing | | 400 | | 600 | mV |
| V _{OC(SS)} Change in steady-state common-mode output voltage between logic states | | –5 | | 5 | mV |
| V _{OD(PP)} Peak-to-peak output differential voltage | | 800 | | 1200 | mV |
| V _{(O)SBY} Single-ended standby output voltage | AVCC = 3.3 V, R _T = 50 Ω, LP = 0 | AVCC–10 | | AVCC+10 | mV |
| I _{(O)OFF} Single-ended power down output current | 0 V ≤ V _{CC} ≤ 1.5 V, AVCC = 3.3 V, R _T = 50 Ω | –10 | | 10 | μA |
| I _{OS} Short circuit output current | V _{ID} = 500 mV | –15 | | 15 | mA |
| R _{INT} Input termination impedance | | 45 | 50 | 55 | Ω |
| V _{term} Input termination voltage | | 1 | | 2 | V |

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|-----|-----|-----|------|
| t _{PLH} Propagation delay time | AVCC = 3.3 V, R _T = 50 Ω, f = 1 MHz | 250 | 350 | 600 | ps |
| t _{PHL} Propagation delay time | | 250 | 350 | 600 | ps |
| t _R Rise time | | 60 | 90 | 140 | ps |
| t _F Fall time | | 60 | 90 | 140 | ps |
| t _{SK(P)} Pulse skew | | | 8 | 15 | ps |
| t _{SK(D)} Intra-pair skew | | | 20 | 40 | ps |
| t _{SK(O)} Inter-pair skew | | | 20 | 65 | ps |
| t _{JTD(PP)} Peak-to-peak output residual data jitter | AVCC = 3.3 V, R _T = 50 Ω, dR = 2.5 Gbps | | 14 | 50 | ps |
| t _{JTC(PP)} Peak-to-peak output residual clock jitter | AVCC = 3.3 V, R _T = 50 Ω, f = 250 MHz | | 8 | 30 | ps |

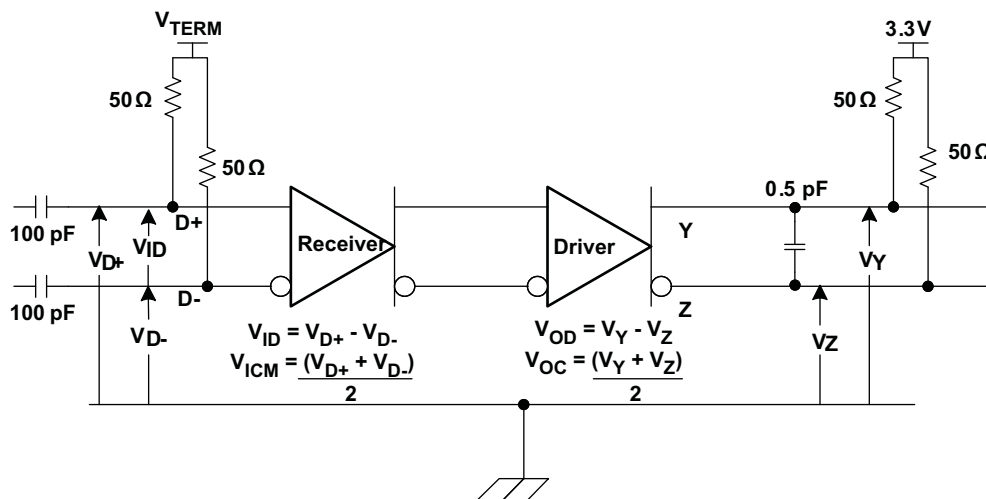


Figure 13. TMD5 Main Link Test Circuit

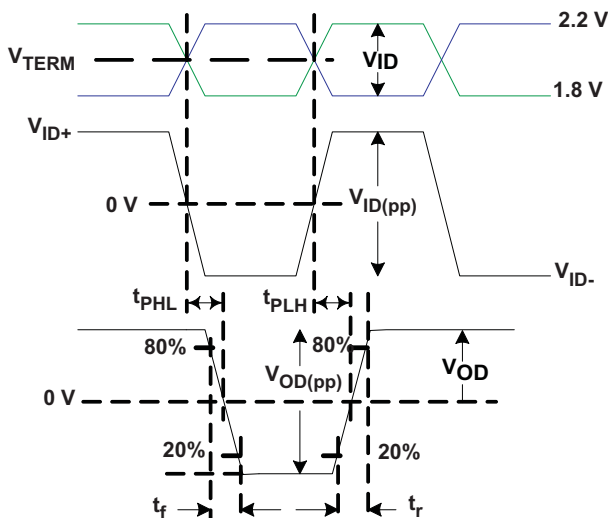


Figure 14. TMD5 Main Link Timing Measurements

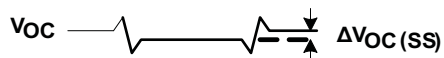
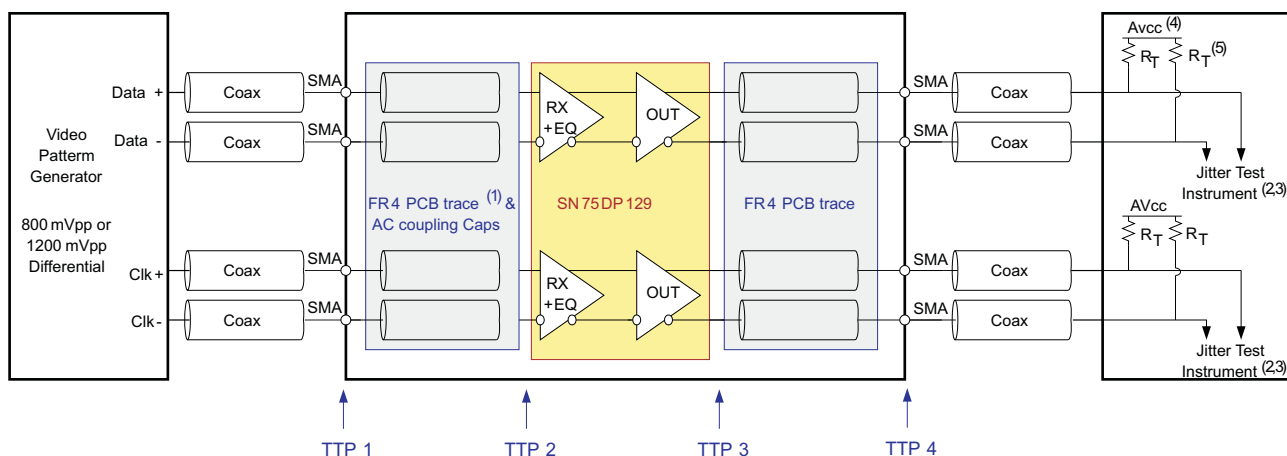


Figure 15. TMD5 Main Link Common Mode Measurements



- (1) The FR4 trace between TTP1 and TTP2 is designed to emulate 8 inches of FR4, a connector, and another 8 inches of FR4.
- (2) All jitter is measured at a BER of 10^{-12}
- (3) Residual jitter reflects the total jitter measured at TTP4 minus the jitter measured at TTP1.
- (4) AVCC = 3.3 V
- (5) $R_T = 50 \Omega$

Figure 16. TMD5 Jitter Measurements

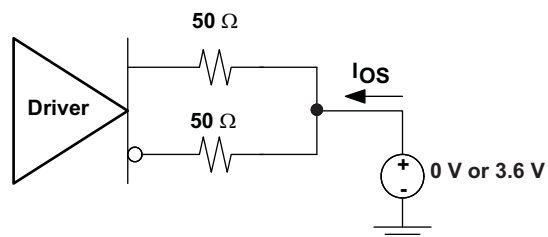


Figure 17. TMD5 Main Link Short Circuit Output Circuit

TYPICAL CHARACTERISTICS

Power dissipation is the sum of the power consumption from the VCC and VDD pins, plus the 132 mW of power from the AVCC (Receiver Termination Supply).

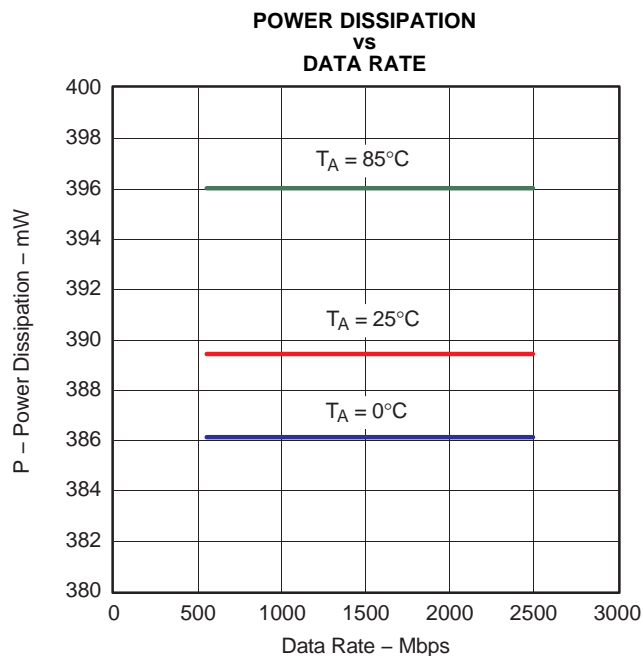


Figure 18.

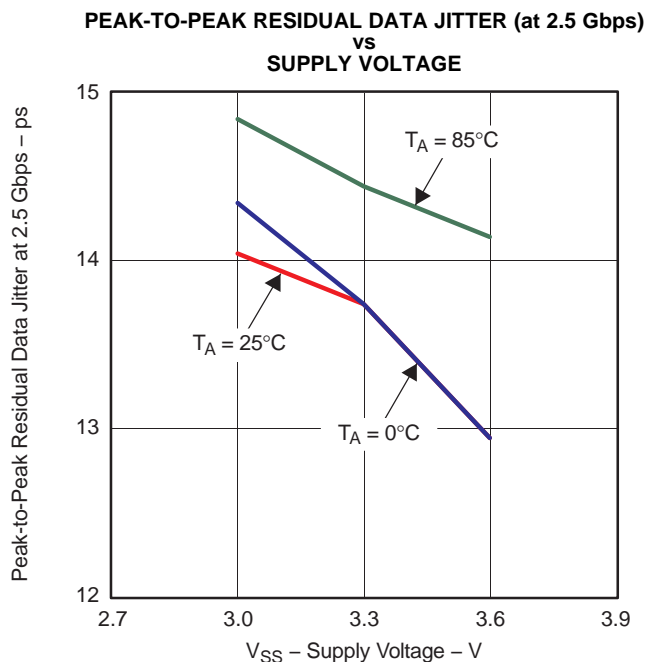


Figure 19.

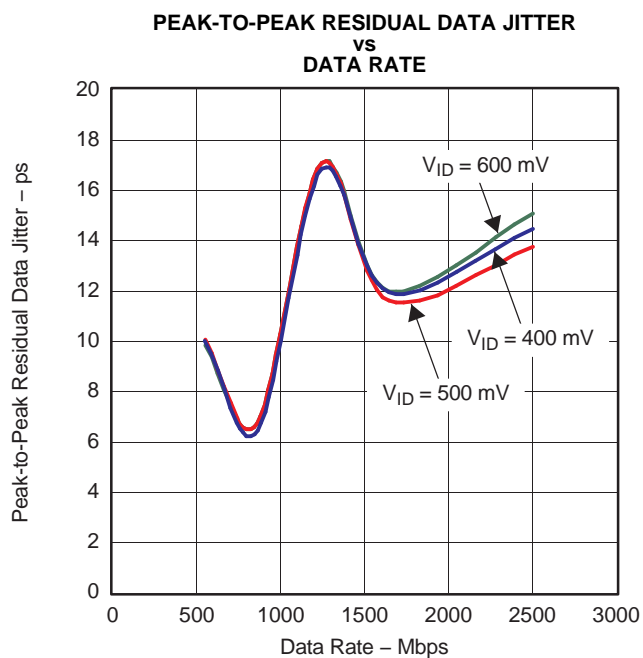


Figure 20.

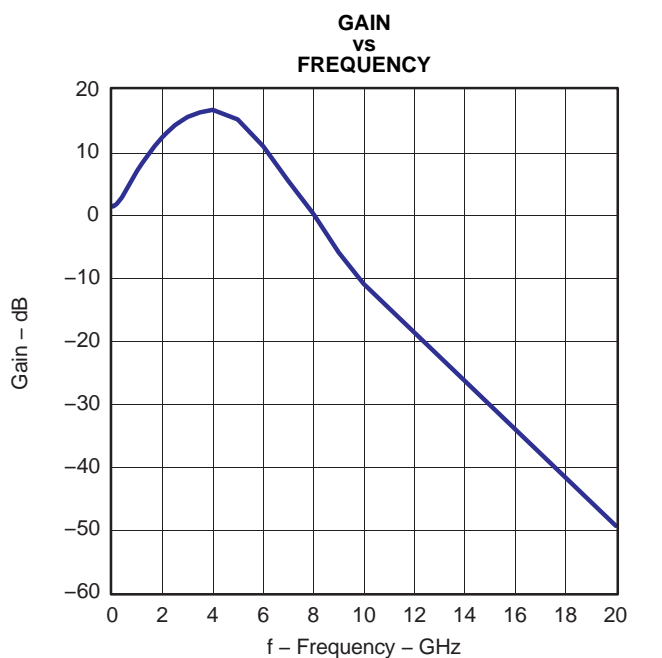
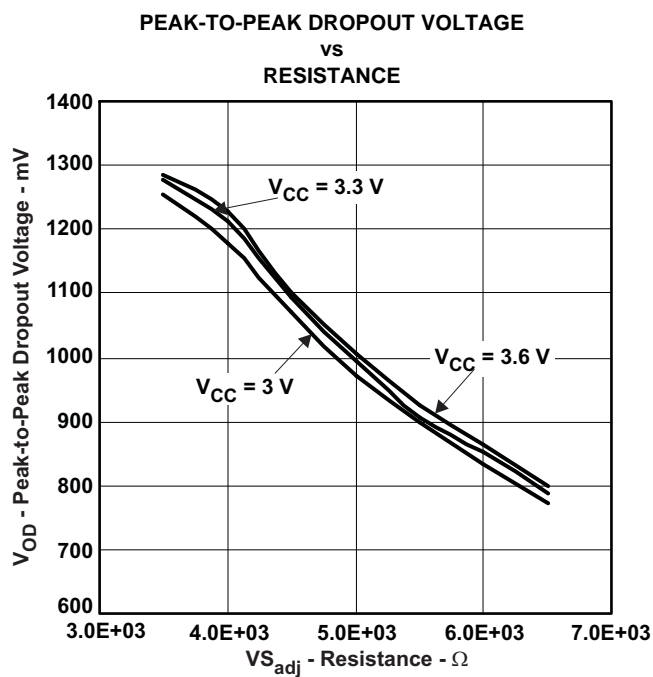


Figure 21.

TYPICAL CHARACTERISTICS (continued)

Power dissipation is the sum of the power consumption from the VCC and VDD pins, plus the 132 mW of power from the AVCC (Receiver Termination Supply).



APPLICATION INFORMATION

I²C INTERFACE NOTES

The I²C interface can access the internal memory of the SN75DP129. I²C is a two-wire serial interface developed by Philips Semiconductor (see [I²C-Bus Specification, Version 2.1, January 2000](#)). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is *idle*, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open drain I/O pins, SDA and SCL. A *master* device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A *slave* device receives and/or transmits data on the bus under control of the master device. The SN75DP129 works as a slave and supports the standard mode transfer (100 kbps) as defined in the I²C-Bus Specification.

The basic I²C start and stop access cycles are shown in [Figure 23](#).

The basic access cycle consists of the following:

- A start condition
- A slave address cycle
- Any number of data cycles
- A stop condition

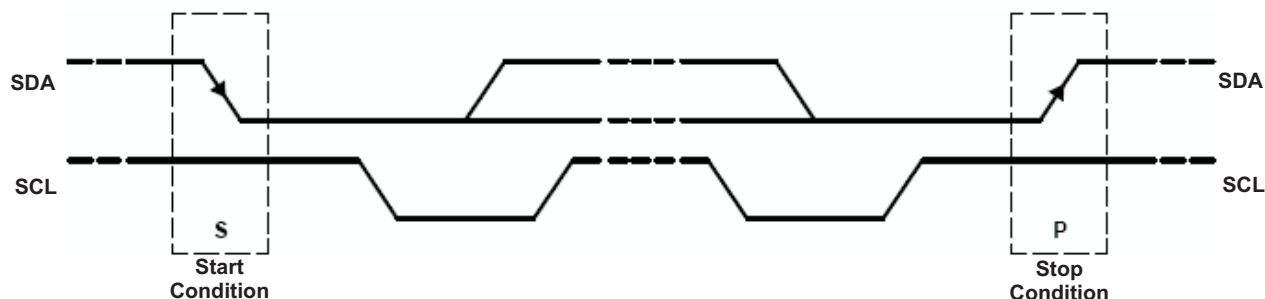
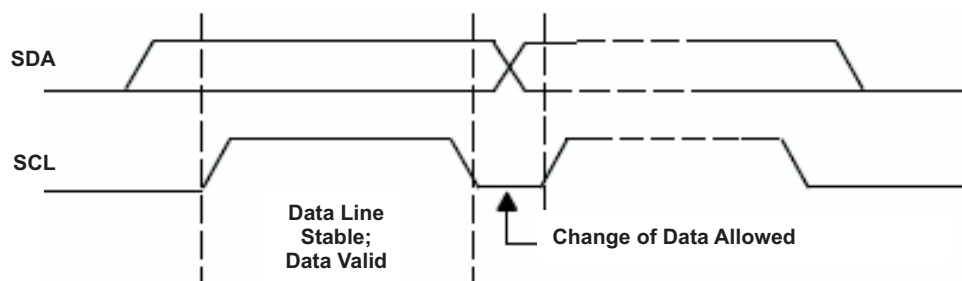
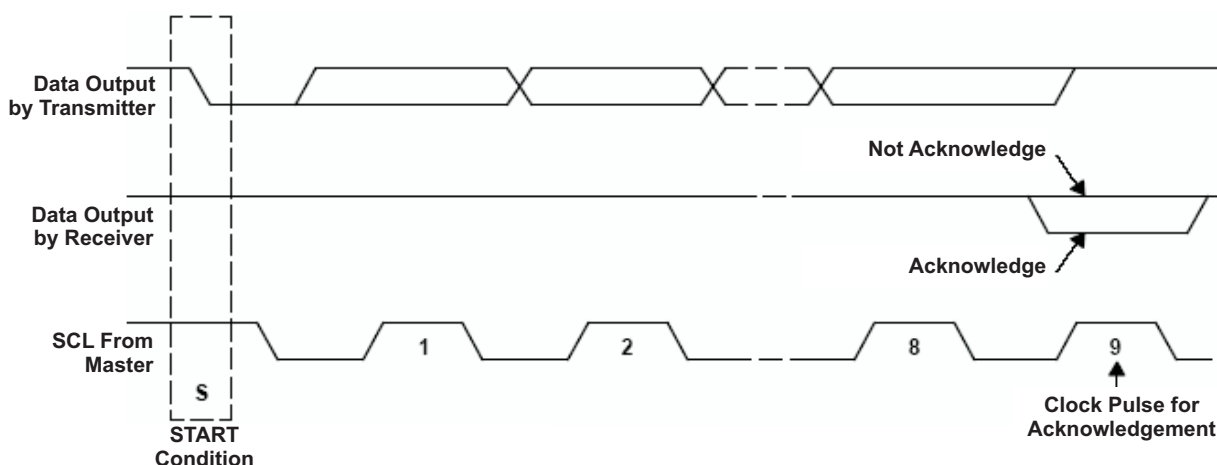
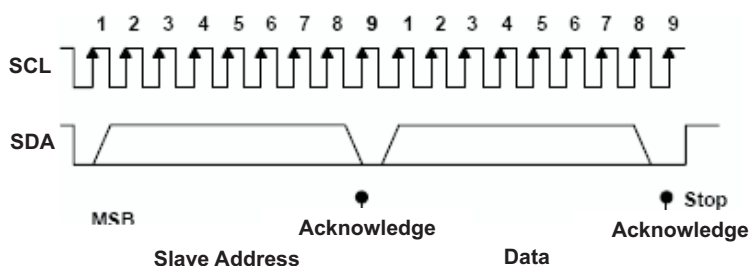


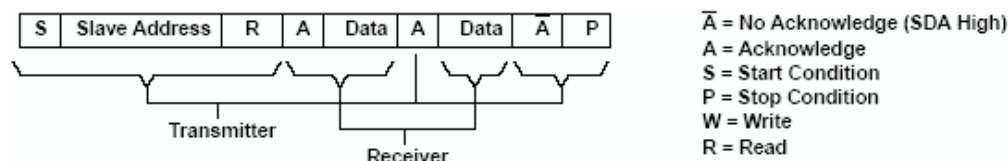
Figure 23. I²C Start and Stop Conditions

GENERAL I²C PROTOCOL

- The master initiates data transfer by generating a *start condition*. The *start condition* is when a high-to-low transition occurs on the SDA line the SCL line is high, as shown in [Figure 25](#). All I²C-compliant devices should recognize a *start condition*.
- The master generates the SCL pulses and transmits the 7-bit address and the *read/write direction bit* R/W on the SDA line. During all transmissions, the master ensures that data is *valid*. A *valid data* condition requires the SDA line to be stable during the entire high period of the clock pulse (see [Figure 24](#)). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an *acknowledge* (see [Figure 25](#)) by pulling the SDA line low during the entire high period of the ninth SCL cycle. On detecting this acknowledge, the master knows that a communication link with a slave has been established.
- The master generates further SCL cycles to transmit data to the slave (R/W bit 0) or *receive* data from the slave (R/W bit 1). In either case, the *receiver* needs to acknowledge the data sent by the *transmitter*. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary (see [Figure 26](#)).
- To signal the end of the data transfer, the master generates a *stop condition* by pulling the SDA line from low to high while the SCL line is high (see [Figure 26](#)). This releases the bus and stops the communication link with the addressed slave. All I²C compatible devices must recognize the stop condition. Upon the receipt of a *stop condition*, all devices know that the bus is released, and they wait for a *start condition*, followed by a matching address.

Figure 24. I²C Bit TransferFigure 25. I²C AcknowledgeFigure 26. I²C Address and Data Cycles

During a read cycle, the slave receiver acknowledges the initial address byte if it decodes the address as its address. Following this initial acknowledge by the slave, the master device becomes a receiver and acknowledges data bytes sent by the slave. When the master has received all of the requested data bytes from the slave, the not acknowledge (A) condition is initiated by the master by keeping the SDA signal high just before it asserts the stop (P) condition. This sequence terminates a read cycle as shown in Figure 27 and Figure 28. See the [Reading from the SN75DP129, an example](#) section for more information.

Figure 27. I²C Read Cycle

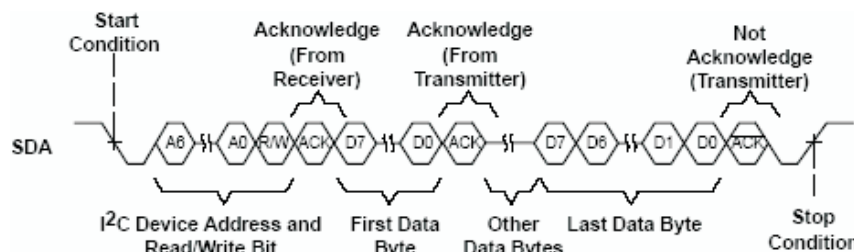


Figure 28. Multiple Byte Read Transfer

Slave Address

Both SDA and SCL must be connected to a positive supply voltage via a pull-up resistor. These resistors should comply with the I²C specification that ranges from 2 kΩ to 19 kΩ. When the bus is free, both lines are high. The address byte is the first byte received following the START condition from the master device. The 7 bit address is factory preset to 1000000. [Table 2](#) lists the calls that the SN75DP129 will respond to.

Table 2. SN75DP129 Slave Address

| FIXED ADDRESS | | | | | | | READ/WRITE BIT |
|---------------|-------|-------|-------|-------|-------|-------|----------------|
| BIT 7 (MSB) | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 (R/W) |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Sink Port Selection Register and Source Plug-In Status Register Description (Sub-Address)

The SN75DP129 operates using a multiple byte transfer protocol similar to [Figure 28](#). The internal memory of the SN75DP129 contains the phrase *DP-HDMI ADAPTOR<EOT>* converted to ASCII characters. The internal memory address registers and the corresponding values can be found in [Table 3](#).

During a read cycle, the SN75DP129 sends the data (within its selected sub-address) in a single transfer to the master device requesting the information. See the [Reading from the SN75DP129, an Example](#) section of this data sheet for the proper procedure.

Table 3. SN75DP129 Sink Port and Source Plug-In Status Registers Selection

| ADDRESS | 0x00 | 0x01 | 0x02 | 0x03 | 0x04 | 0x05 | 0x06 | 0x07 | 0x08 | 0x09 | 0x0A | 0x0B | 0x0C | 0x0D | 0x0E | 0x0F | 0x10 |
|---------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| Data | 44 | 50 | 2D | 48 | 44 | 4D | 49 | 20 | 41 | 44 | 41 | 50 | 54 | 4F | 52 | 04 | FF |

READING FROM THE SN75DP129, AN EXAMPLE

The read operation consists of several steps. The I²C master begins the communication with the transmission of the start sequence, followed by the slave address of the SN75DP129 and logic address of **00h**. The SN75DP129 acknowledges its presence to the master and begins to transmit the memory registers contents. After each byte is transferred, the SN75DP129 waits for an acknowledge (ACK) or a not-acknowledge (NACK) from the master. If an ACK is received, the next byte of data is transmitted. If a NACK is received, the data transmission sequence is expected to end and the master should send the stop command.

The SN75DP129 continues to send data until the master fails to acknowledge each byte transmission. If an ACK is received after the transmission of byte **0x0F**, the SN75DP129 transmits byte **0x10** and continues to transmit byte **0x10** for all further ACK's until a NACK is received.

SN75DP129 Read Phase

| | |
|---------------------------------|----------|
| Step 1⁽¹⁾ | 0 |
| I ² C Start (Master) | S |

(1) The SN75DP129 also supports an accelerated read mode in which steps 1 through 6 can be skipped.

| | | | | | | | | |
|---|----------|----------|----------|----------|----------|----------|----------|----------|
| Step 2 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| I ² C General Address Write (Master) | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|--------------------------------------|----------|
| Step 3 | 9 |
| I ² C Acknowledge (Slave) | A |

| | | | | | | | | |
|---|----------|----------|----------|----------|----------|----------|----------|----------|
| Step 4 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| I ² C Logic Address (Master) | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|--------------------------------------|----------|
| Step 5 | 9 |
| I ² C Acknowledge (Slave) | A |

| | |
|--------------------------------|----------|
| Step 6 | 0 |
| I ² C Stop (Master) | P |

| | |
|---------------------------------|----------|
| Step 7 | 0 |
| I ² C Start (Master) | S |

| | | | | | | | | |
|--|----------|----------|----------|----------|----------|----------|----------|----------|
| Step 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| I ² C General Address Read (Master) | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

| | |
|--------------------------------------|----------|
| Step 9 | 9 |
| I ² C Acknowledge (Slave) | A |

| | | | | | | | | |
|------------------------------------|----------|----------|----------|----------|----------|----------|----------|----------|
| Step 10 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| I ² C Read Data (Slave) | Data | Data | Data | Data | Data | Data | Data | Data |

Where Data is determined by the Logic values Contained in the Sink Port Register

| | |
|---|----------|
| Step 11 | 9 |
| I ² C Not-Acknowledge (Master) | X |

Where X is an A (Acknowledge) or \bar{A} (Not-Acknowledge)

An A causes the pointer to increment and step 10 is repeated.

An \bar{A} causes the slave to stop transmitting and proceeds to step 12.

| | |
|--------------------------------|----------|
| Step 12 | 0 |
| I ² C Stop (Master) | P |

Revision History

| Changes from Original (January 2008) to Revision A | Page |
|--|------|
| • Changed device power dissipation from 250 mW typ to 380 mW typ..... | 8 |
| • Changed device power dissipation from 400 mW max to 490 mW max..... | 8 |
| • Changed propagation delay time, high to low, sink to source from 140 ns max to 200 ns max..... | 10 |
| • Changed t_{PHL1} to t_{PLH1} in Figure 12 | 11 |
| • Changed t_{PHL} propagation delay time from 800 ps max to 600 ps max..... | 12 |
| • Changed $t_{JITD(PP)}$ peak-to-peak output residual data jitter from 20 ps typ to 14 ps typ..... | 12 |
| • Changed $t_{JITC(PP)}$ peak-to-peak output residual clock jitter from 10 ps typ to 8 ps typ..... | 12 |
| • Added peak-to-peak dropout voltage vs resistance curves..... | 16 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN75DP129RHHR | ACTIVE | VQFN | RHH | 36 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | 0 to 85 | DP129 | Samples |
| SN75DP129RHHT | ACTIVE | VQFN | RHH | 36 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | 0 to 85 | DP129 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN75DP129RHHR | VQFN | RHH | 36 | 2500 | 330.0 | 16.4 | 6.3 | 6.3 | 1.5 | 12.0 | 16.0 | Q2 |
| SN75DP129RHHT | VQFN | RHH | 36 | 250 | 180.0 | 16.4 | 6.3 | 6.3 | 1.5 | 12.0 | 16.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS

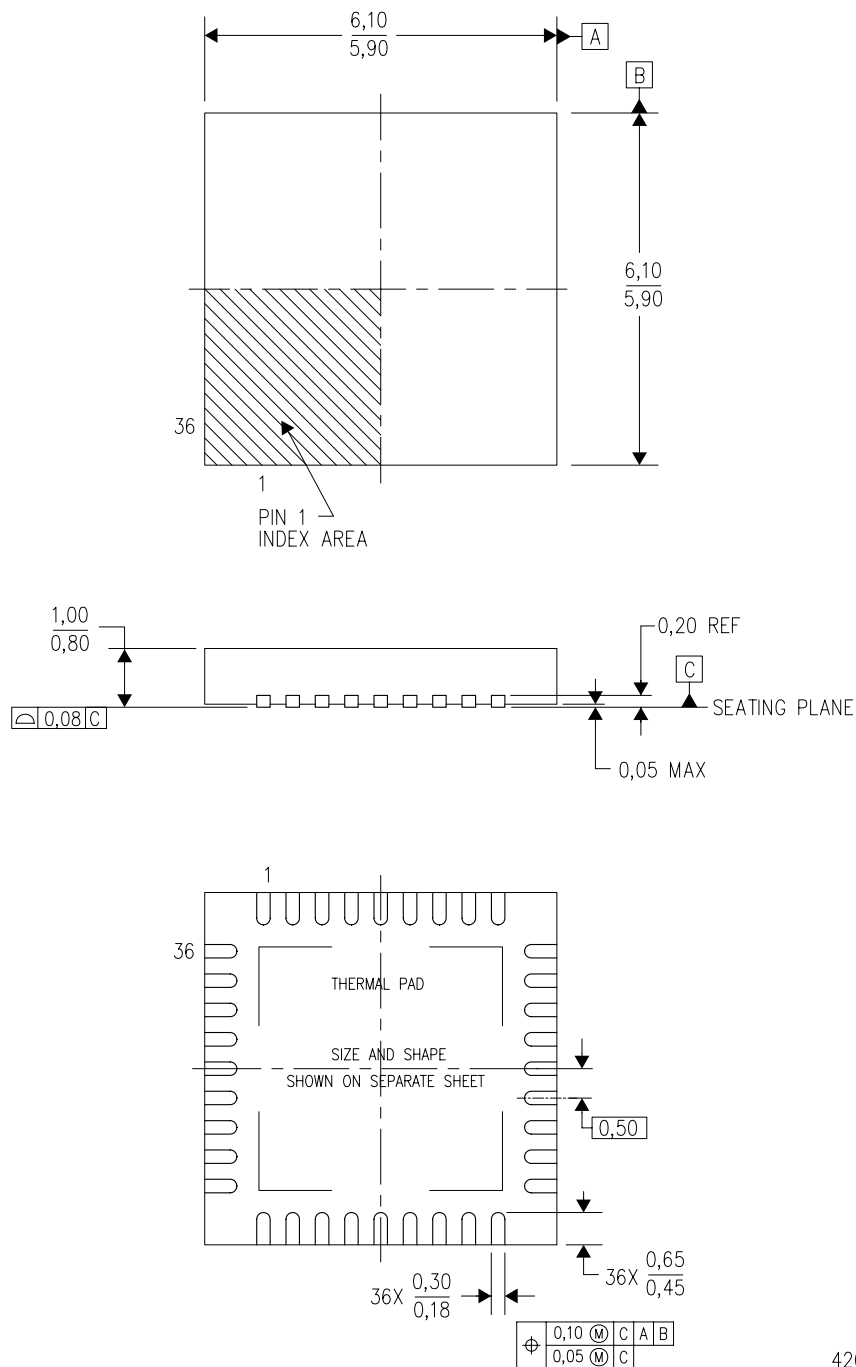


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN75DP129RHHR | VQFN | RHH | 36 | 2500 | 367.0 | 367.0 | 38.0 |
| SN75DP129RHHT | VQFN | RHH | 36 | 250 | 210.0 | 185.0 | 35.0 |

RHH (S-PVQFN-N36)

PLASTIC QUAD FLATPACK NO-LEAD



4205094/E 06/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) Package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Falls within JEDEC MO-220.

RHH (S-PVQFN-N36)

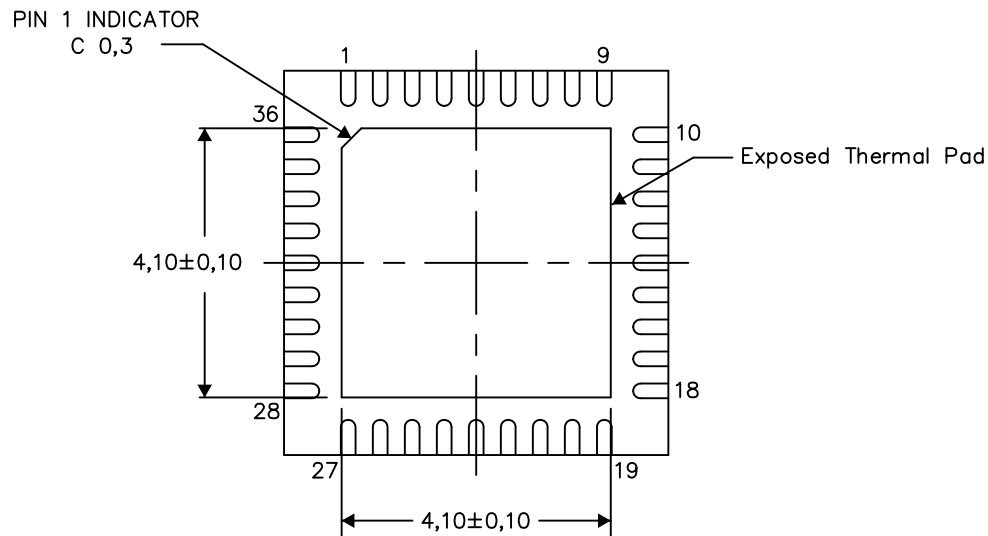
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

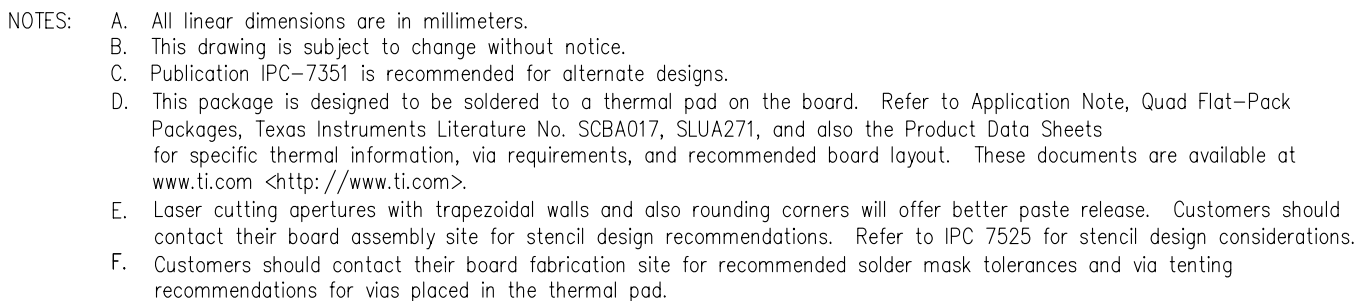


Bottom View

Exposed Thermal Pad Dimensions

4206362-3/M 11/13

NOTE: All linear dimensions are in millimeters



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