PCM5242 4.2-V_{RMS} DirectPath™, 114-dB Audio Stereo Differential-Output DAC with 32-bit, 384-kHz PCM Interface

1 Features

- Differential DirectPath™ Ground Biased Outputs
- Market-Leading Low Out-of-Band Noise
- Selectable Digital-Filter Latency and Performance
- No DC Blocking Capacitors Required
- Integrated Negative Charge Pump
- Intelligent Muting System; Soft Up or Down Ramp and Analog Mute for 120dB Mute SNR
- Integrated High-Performance Audio PLL With BCK Reference to Generate SCK Internally
- Accepts 16-, 24-, and 32-Bit Audio Data
- PCM Data Formats: I^2S, Left-Justified, Right-Justified, TDM
- SPI or I^2C Control
- Software or Hardware Configuration
- Automatic Power-Save Mode When LRCK And BCK Are Deactivated
- 1.8V or 3.3V Failsafe LVCMOS Digital Inputs
- Single Supply Operation:
  - 3.3V Analog, 1.8V or 3.3V Digital
- Integrated Power-On Reset
- Small 32-terminal QFN Package

2 Applications

- HiFi Smartphone
- A/V Receivers
- DVD, BD Players
- HDTV Receivers

3 Description

The PCM5242 is a monolithic CMOS integrated circuit that includes a stereo digital-to-analog converter and additional support circuitry in a small QFN package. The PCM5242 uses the latest generation of TI's advanced segment-DAC architecture to achieve excellent dynamic performance and improved tolerance to clock jitter.

The PCM5242 integrates a fully programmable miniDSP core, allowing developers to integrate filters, dynamic range controls, custom interpolators and other differentiating features to their products.

The PCM5242 provides 4.2V_{RMS} ground-centered differential outputs, allowing designers to eliminate DC blocking capacitors on the output, as well as external muting circuits traditionally associated with single supply line drivers.

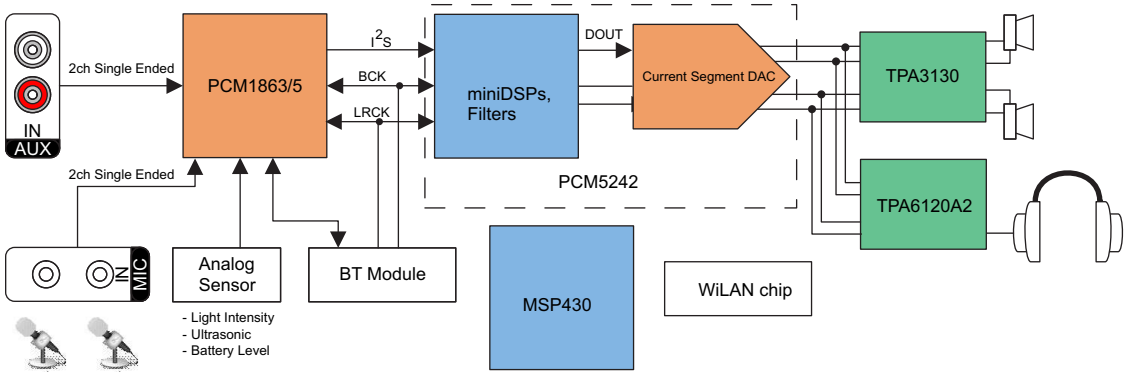
The integrated PLL on the device removes the requirement for a system clock (commonly known as master clock), allowing a 3-wire I^2S connection and reducing system EMI.

Device Information(1)

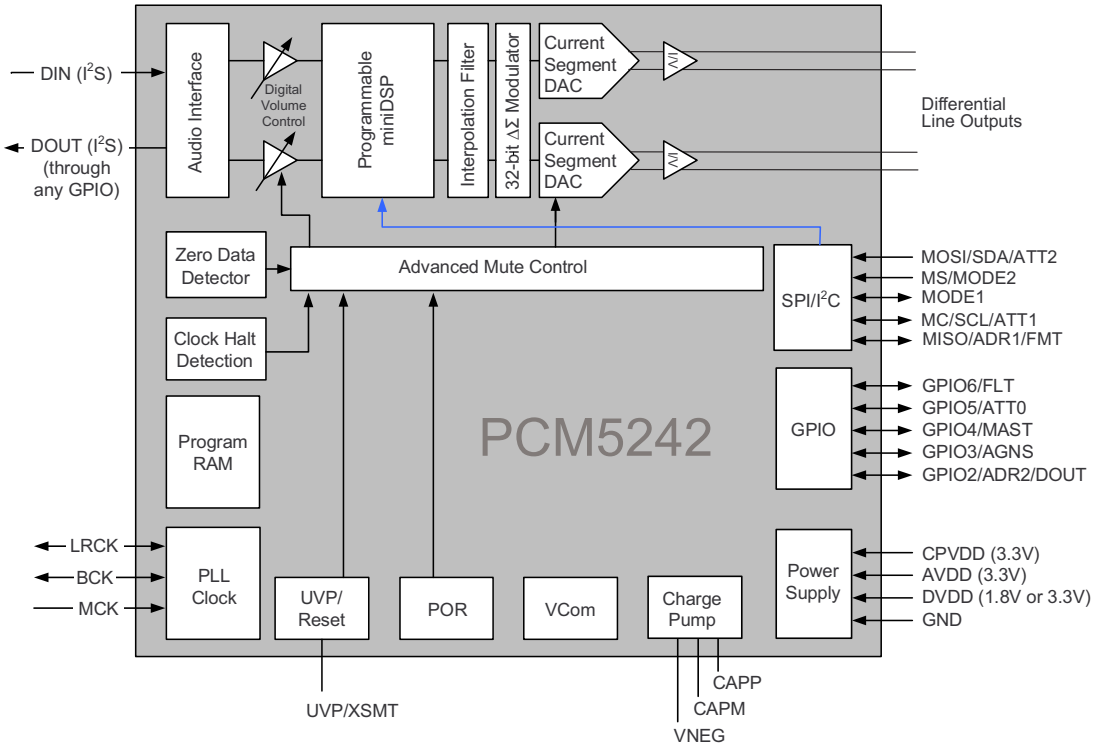
PART NAME	PACKAGE	BODY SIZE (NOM)
PCM5242	VQFN (32)	5.00mm × 5.00mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified System Diagram



Simplified Block Diagram



Typical Performance (3.3V Power Supply)

Parameter	PCM5242
SNR	114dB
Dynamic Range	114dB
THD+N at - 1dBFS	–94dB
Full Scale Differential Output	4.2V_{RMS} (GND center)
Normal 8× Oversampling Digital Filter Latency: 20t_S	
Low Latency 8× Oversampling Digital Filter Latency: 3.5t_S	
Sampling Frequency	8kHz to 384kHz
System Clock Multiples (f_{SCK}): 64, 128, 192, 256, 384, 512, 768, 1024, 1152, 1536, 2048, 3072; up to 50 MHz	

Table of Contents

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision Initial (July 2014) to Revision A	Page

- Changed From: A 4-page Product Preview To: A Production datasheet ... 1
- Changed Description text in the first paragraph From: "The PCM5242 devices are a family.." To: "The PCN5242 is a monolithic.." ... 1
- Changed Description text in third paragraoh From: "The PCM5242 provides 2.1V_{RMS}.." To: "The PCM5242 provides 4.2V_{RMS}.. ... 1

6 Pin Configuration and Functions

6.1 Control Mode Effect On Pin Assignments

The PCM5242 supports control from I2C, SPI and Hardware Modes (referred to as HW mode). Selection of modes is done using Mode1 and Mode2 pins. (See Table 1)

SPI Mode is selected by pulling MODE1 to DVDD.

I^2C Mode is selected by pulling MODE1 to DGND and Mode2 to DVDD.

Hardware Control Mode is selected by pulling both MODE1 and MODE2 pins to DGND.

6.2 Pin Assignments

32-Pin RHB (QFN, Top View)

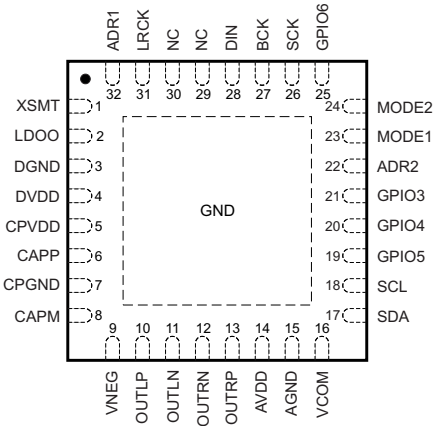


Figure 1. I^2C Control

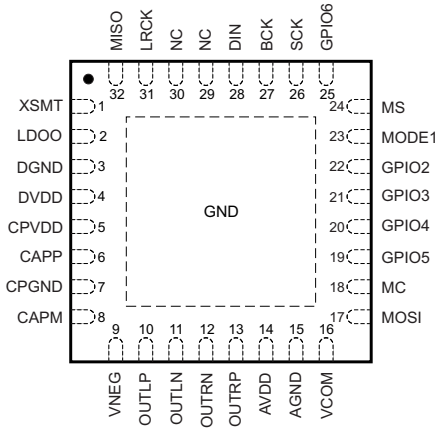


Figure 2. SPI Control

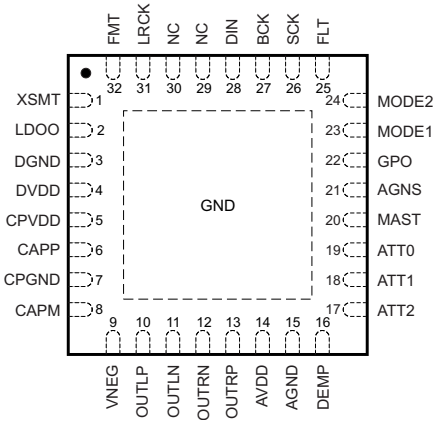


Figure 3. Hardware Control

Table 1. PCM5242 Pin Functions

PIN			PIN	I/O	DESCRIPTION
MODE, NAME					
I^2C	SPI	HW			
XSMT			1	I	Soft mute control(1) Soft mute (Low) / soft un-mute (High)
LDOO			2	-	Internal logic supply rail pin for decoupling, 1.8V
DGND			3	-	Digital ground
DVDD			4	-	Digital power supply, 3.3V or 1.8V
CPVDD			5	-	Charge pump power supply, 3.3V
CAPP			6	O	Charge pump flying capacitor pin for positive rail
CPGND			7	-	Charge pump ground
CAPM			8	O	Charge pump flying capacitor pin for negative rail
VNEG			9	O	Negative charge pump rail pin for decoupling, -3.3V
OUTLP			10		Positive Differential Analog output from DAC left channel
OUTLN			11		Negative Differential Analog output from DAC left channel
OUTRN			12		Negative Differential Analog output from DAC right channel
OUTRP			13		Positive Differential Analog output from DAC right channel.
AVDD			14	-	Analog power supply, 3.3V
AGND			15	-	Analog ground

(1) Failsafe LVCMOS Schmitt trigger input.

Pin Assignments (continued)

Table 1. PCM5242 Pin Functions (continued)

PIN				I/O	DESCRIPTION	
MODE, NAME			PIN			
I²C	SPI	HW				
VCOM			16	O	I²C, SPI	VCOM output (Optional mode selected by register; default setting is VREF mode.) When in VREF mode (default), this pin ties to GND. When in VCOM mode, decoupling capacitor to GND is required.
		DEMP		I	HW	DEMP: De-emphasis control for 44.1kHz sampling rate: Off (Low) / On (High)
SDA	MOSI	ATT2	17	I/O	I²C	Data for I²C(2)(1)
				I	SPI	Input data for SPI(1)
					HW	Digital gain and attenuation control pin
SCL	MC	ATT1	18	I	I²C	Input clock for I²C(1)
					SPI	Input clock for SPI(1)
					HW	Digital gain and attenuation control pin
GPIO5		ATT0	19	I/O	I²C, SPI	General purpose digital input and output port (3)
					HW	Digital gain and attenuation control pin
GPIO4		MAST	20	I/O	I²C, SPI	General purpose digital input and output port (3)
					HW	I²S Master clock select pin : Master (High) BCK/LRCK outputs, Slave (Low) BCK/LRCK inputs
GPIO3		AGNS	21	I/O	I²C, SPI	General purpose digital input and output port (3)
					HW	Analog gain selector : 0dB $2V_{RMS}$ output (Low), -6dB $1V_{RMS}$ output (High)
ADR2	GPIO2	GPO	22	I/O	I²C	2nd LSB address select bit for I²C(3)
					SPI	General purpose digital input and output port (3)
				O	HW	General Purpose Output (Low level)
MODE1			23	I		Mode control selection pin(1) MODE1 = Low, MODE2 = Low : Hardwired mode MODE1 = Low, MODE2 = High: I²C mode MODE1 = High: SPI mode
MODE2	MS	MODE2	24		I²C, HW	MODE2 (See definition in Mode 1 description)
				I	SPI	MS pin (chip select for SPI)
GPIO6		FLT	25	I/O	I²C, SPI	General purpose digital input and output port
				I	HW	Filter select : Normal latency (Low) / Low latency (High)
SCK			26	I	System clock input(1)	
BCK			27	I/O	Audio data bit clock input (slave) or output (master)(1)	
DIN			28	I	Audio data input(1)	
NC			29	-	No connect	
			30	-		
LRCK			31	I/O	Audio data word clock input (slave) or output (master)(1)	
ADR1	MISO (GPIO1)	FMT	32	I/O	I²C	LSB address select bit for I²C
					SPI	Primary output data for SPI readback. Secondary; general purpose digital input/output port controlled by register
					HW	Audio format selection : I²S (Low) / Left justified (High)

(2) Open-drain configuration in out mode.
(3) Internal Pulldown

Table 2. Gain and Attenuation in Hardwired Mode

ATT PIN CONDITION (ATT2 : ATT1 : ATT0)	GAIN AND ATTENUATION LEVEL
(0 0 0)	0 dB
(0 0 1)	+ 3 dB
(0 1 0)	+ 6 dB
(0 1 1)	+ 9 dB
(1 0 0)	+ 12 dB
(1 0 1)	+ 15 dB
(1 1 0)	- 6 dB
(1 1 1)	- 3 dB

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply Voltage	AVDD, CPVDD, DVDD	–0.3	3.9	V
	LDOO wtih DVDD at 1.8V	–0.3	2.25	
Digital Input Voltage	DVDD at 1.8V	–0.3	2.25	
	DVDD at 3.3V	–0.3	3.9	
Analog Input Voltage		–0.3	3.9	

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage Temperature		–40	125	°C
$V_{(ESD)}$	Electrostatic Discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–2500	2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	–1500	1500	

(1) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

				MIN	NOM	MAX	UNIT
AVDD	Analog power supply voltage range	Referenced to AGND(1)	VCOM mode	3.0	3.3	3.46	V
			VREF mode	3.2	3.3	3.46	
DVDD	Digital power supply voltage range	Referenced to DGND(1)	1.8V DVDD	1.65	1.8	1.95	V
			3.3V DVDD	3.1	3.3	3.46	
CPVDD	Charge pump supply voltage range	Referenced to CPGND(1)		3.1	3.3	3.46	V
MCLK	Master Clock Frequency					50	MHz
LOL, LOR	Stereo line output load resistance			2	10		kΩ
C_{Lout}	Digital output load capacitance				10		pF
T_J	Operating Junction Temperature Range			–25		85	°C

(1) All grounds on board are tied together; they must not differ in voltage by more than 0.2V max, for any combination of ground signals.

7.4 Thermal Information

THERMAL METRIC		RHB (32 PINS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	72.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	17.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	35.0	
ψ_{JT}	Junction-to-top characterization parameter	0.4	
ψ_{JB}	Junction-to-board characterization parameter	34.5	
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	n/a	

7.5 Electrical Characteristics

All specifications at T_A = 25°C, AV_{DD} = CPV_{DD} = DV_{DD} = 3.3V, f_S = 48kHz, system clock = 512f_S and 24-bit data unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution		16	24	32	Bits
Digital Input/Output						
	Logic Family: 3.3V LVCMOS compatible					
V_{IH}	Input logic level		0.7×DV_{DD}			V
V_{IL}					0.3×DV_{DD}	
I_{IH}	Input logic current	V_{IN} = V_{DD}			10	µA
I_{IL}		V_{IN} = 0V			–10	
V_{OH}	Output logic level	I_{OH} = –4mA	0.8×DV_{DD}			V
V_{OL}		I_{OL} = 4mA			0.22×DV_{DD}	
	Logic Family 1.8V LVCMOS compatible					
V_{IH}	Input logic level		0.7×DV_{DD}			V
V_{IL}					0.3×DV_{DD}	
I_{IH}	Input logic current	V_{IN} = V_{DD}			10	µA
I_{IL}		V_{IN} = 0V			–10	
V_{OH}	Output logic level	I_{OH} = –2mA	0.8×DV_{DD}			V
V_{OL}		I_{OL} = 2mA			0.22×DV_{DD}	
Dynamic Performance (PCM Mode)(1)(2)						
	THD+N at -1 dB(2)	f_S = 48kHz		–94	–87	dB
		f_S = 96kHz		–94		
		f_S = 192kHz		–94		
	Dynamic range(2)	EIAJ, A-weighted, f_S = 48kHz	108	114		
		EIAJ, A-weighted, f_S = 96kHz		114		
		EIAJ, A-weighted, f_S = 192kHz		114		
	Signal-to-noise ratio(2)	EIAJ, A-weighted, f_S = 48kHz		114		
		EIAJ, A-weighted, f_S = 96kHz		114		
		EIAJ, A-weighted, f_S = 192kHz		114		
	Signal to noise ratio with analog mute(2)(3)	EIAJ, A-weighted, f_S = 48kHz	113	123		
		EIAJ, A-weighted, f_S = 96kHz	113	123		
		EIAJ, A-weighted, f_S = 192kHz	113	123		
	Channel Separation	f_S = 48kHz	100 / 95	109 / 103		dB
		f_S = 96kHz	100 / 95	109 / 103		
		f_S = 192kHz	100 / 95	109 / 103		

(1) Filter condition: THD+N: 20Hz HPF, 20kHz AES17 LPF Dynamic range: 20Hz HPF, 20kHz AES17 LPF, A-weighted Signal-to-noise ratio: 20Hz HPF, 20kHz AES17 LPF, A-weighted Channel separation: 20Hz HPF, 20kHz AES17 LPF Analog performance specifications are measured using the System Two Cascade™ audio measurement system by Audio Precision™ in the RMS mode.
(2) Output load is 10kΩ, with 470Ω output resistor and a 2.2nF shunt capacitor (see recommended output filter).
(3) Assert XSMT or both L-ch and R-ch PCM data are BPZ

Electrical Characteristics (continued)

All specifications at T_A = 25°C, AV_{DD} = CPV_{DD} = DV_{DD} = 3.3V, f_S = 48kHz, system clock = 512f_S and 24-bit data unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog Output						
	Single Ended Output voltage			2.1		V_{RMS}
	Differential Output Voltage			4.2		V_{RMS}
	Gain error		–6	±2.0	6	% of FSR
	Gain mismatch, channel-to-channel		–6	±0.5	6	% of FSR
	Bipolar zero error	At bipolar zero	–2	±1.0	2	mV
	Load impedance		5			kΩ
Filter Characteristics–1: Normal (8x)						
	Pass band				0.45f_S	kHz
	Stop band		0.55f_S			
	Stop band attenuation		–60			dB
	Pass-band ripple				±0.02	
	Delay time			20t_S		s
Filter Characteristics–2: Low Latency (8x)						
	Pass band				0.47f_S	kHz
	Stop band		0.55f_S			
	Stop band attenuation		–52			dB
	Pass-band ripple				±0.0001	
	Delay time			3.5t_S		s
Filter Characteristics–3: Asymmetric FIR (8x)						
	Pass band				0.40f_S	kHz
	Stop band		0.72f_S			
	Stop band attenuation		–52			dB
	Pass-band ripple				±0.05	
	Delay time			1.2t_S		s
Filter Characteristics–4: High-Attenuation (8x)						
	Pass band				0.45f_S	kHz
	Stop band		0.45f_S			
	Stop band attenuation			–100		dB
	Pass-band ripple				±0.0005	
	Delay time			33.7t_S		s

Electrical Characteristics (continued)

All specifications at T_A = 25°C, AV_{DD} = CPV_{DD} = DV_{DD} = 3.3V, f_S = 48kHz, system clock = 512f_S and 24-bit data unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply Requirements						
DV_{DD}	Digital supply voltage	Target DV_{DD} = 1.8V	1.65	1.8	1.95	VDC
DV_{DD}	Digital supply voltage	Target DV_{DD} = 3.3V	3.0	3.3	3.6	VDC
AV_{DD}	Analog supply voltage		3.0	3.3	3.6	VDC
CPV_{DD}	Charge-pump supply voltage		3.0	3.3	3.6	VDC
I_{DD}	DV_{DD} supply current at 1.8V	f_S = 48kHz, Input is Bipolar Zero data		11	14	mA
		f_S = 96kHz, Input is Bipolar Zero data		12		
		f_S = 192kHz, Input is Bipolar Zero data		14		
I_{DD}	DV_{DD} supply current at 1.8V	f_S = 48kHz, Input is 1kHz -1dBFS data		11	14	mA
		f_S = 96kHz, Input is 1kHz -1dBFS data		12		
		f_S = 192kHz, Input is 1kHz -1dBFS data		14		
I_{DD}	DV_{DD} supply current at 1.8V(4)	f_S = N/A, Power Down Mode		0.3	0.6	mA
I_{DD}	DV_{DD} supply current at 3.3V	f_S = 48kHz, Input is Bipolar Zero data		12	15	mA
		f_S = 96kHz, Input is Bipolar Zero data		13		
		f_S = 192kHz, Input is Bipolar Zero data		15		
I_{DD}	DV_{DD} supply current at 3.3V	f_S = 48kHz, Input is 1kHz -1dBFS data		12	15	mA
		f_S = 96kHz, Input is 1kHz -1dBFS data		13		
		f_S = 192kHz, Input is 1kHz -1dBFS data		15		
I_{DD}	DV_{DD} supply current at 3.3V(4)	f_S = N/A, Power Down Mode		0.5	0.8	mA
I_{CC}	AV_{DD} + CPV_{DD} Supply Current	f_S = 48kHz, Input is Bipolar Zero data		11	16	mA
		f_S = 96kHz, Input is Bipolar Zero data		11		
		f_S = 192kHz, Input is Bipolar Zero data		11		
I_{CC}	AV_{DD} + CPV_{DD} Supply Current	f_S = 48kHz, Input is 1kHz -1dBFS data		24	32	mA
		f_S = 96kHz, Input is 1kHz -1dBFS data		24		
		f_S = 192kHz, Input is 1kHz -1dBFS data		24		
I_{CC}	AV_{DD} + CPV_{DD} Supply Current(4)	f_S = N/A, Power Down Mode		0.2	0.4	mA
	Power Dissipation, DV_{DD} = 1.8V	f_S = 48kHz, Input is Bipolar Zero data		59.4	78	mW
		f_S = 96kHz, Input is Bipolar Zero data		61.2		
		f_S = 192kHz, Input is Bipolar Zero data		64.8		
	Power Dissipation, DV_{DD} = 1.8V	f_S = 48kHz, Input is 1kHz -1dBFS data		99	130.8	mW
		f_S = 96kHz, Input is 1kHz -1dBFS data		100.8		
		f_S = 192kHz, Input is 1kHz -1dBFS data		104.4		
	Power Dissipation, DV_{DD} = 1.8V(4)	f_S = N/A, Power Down Mode		1.2		mW
	Power Dissipation, DV_{DD} = 3.3V	f_S = 48kHz, Input is Bipolar Zero data		79.2	103	mW
		f_S = 96kHz, Input is Bipolar Zero data		82.5		
		f_S = 192kHz, Input is Bipolar Zero data		89.1		
	Power Dissipation, DV_{DD} = 3.3V	f_S = 48kHz, Input is 1kHz -1dBFS data		118.8	155	mW
		f_S = 96kHz, Input is 1kHz -1dBFS data		122.1		
		f_S = 192kHz, Input is 1kHz -1dBFS data		128.7		
	Power Dissipation, DV_{DD} = 3.3V(4)	f_S = N/A, Power Down Mode		2.3	4.0	mW

(4) Power Down Mode, with LRCK, BCK, and SCK halted at Low level.

7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Data Format (PCM Mode)						
	Audio data interface format		I^2S, left justified, right justified and TDM			
	Audio data bit length		16, 20, 24, 32-bit acceptable			
	Audio data format		MSB First, 2s Complement			
f_S (1)	Sampling frequency		8		384	kHz
Clocks						
	System clock frequency		64, 128, 192, 256, 384, 512, 768, 1024, 1152, 1536, 2048, or 3072 f_{SCK}, up to 50Mhz			
	PLL Input Frequency (2)	Clock divider uses fractional divide D > 0, P=1	6.7		20	MHz
		Clock divider uses integer divide D = 0, P=1	1		20	MHz

(1) One sample time si defined as the reciprocal of the sampling frequency. $1t_S = 1/f_S$
(2) With the appropriate P coefficient setting, the PLL accepts up to 50MHz. This clock is then divided to meet the ≤ 20MHz requirement. See PLL Calculation.

7.7 Timing Requirements: SCK Input

Figure 4 shows the timing requirements for the system clock input. For optimal performance, use a clock source with low phase jitter and noise.

			MIN	TYP	MAX	UNIT
t_{SCY}	System clock pulse cycle time		20		1000	ns
t_{SCKH}	System clock pulse width, High	DVDD = 1.8V	8			ns
		DVDD = 3.3V	9			
t_{SCKL}	System clock pulse width, Low	DVDD = 1.8V	8			ns
		DVDD = 3.3V	9			

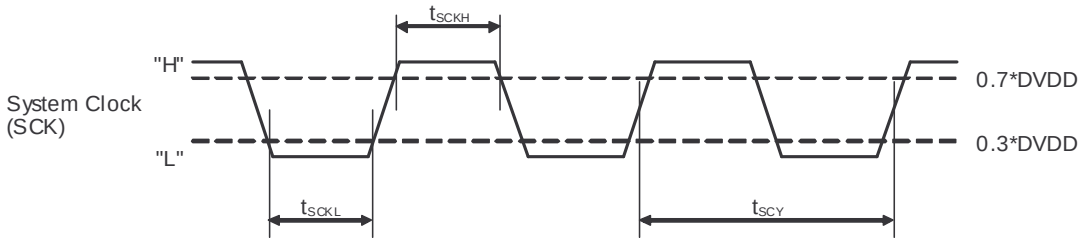


Figure 4. Timing Requirements for SCK Input

7.8 Timing Requirements: PCM Audio Data

		MIN	TYP	MAX	UNIT
t_{BCY}	BCK Pulse Cycle Time	40			ns
t_{BCL}	BCK Pulse Width LOW	16			ns
t_{BCH}	BCK Pulse Width HIGH	16			ns
t_{BL}	BCK Rising Edge to LRCK Edge	8			ns
t_{BCK}	BCK frequency at DVDD = 3.3V			24.576	MHz
$t_{BCK(1.8V)}$	BCK frequency at DVDD = 1.8V			12.288	MHz
t_{LB}	LRCK Edge to BCK Rising Edge	8			ns
t_{DS}	DATA Set Up Time	8			ns
t_{DH}	DATA Hold Time	8			ns
t_{DOD}	DATA delay time from BCK falling edge			15	ns

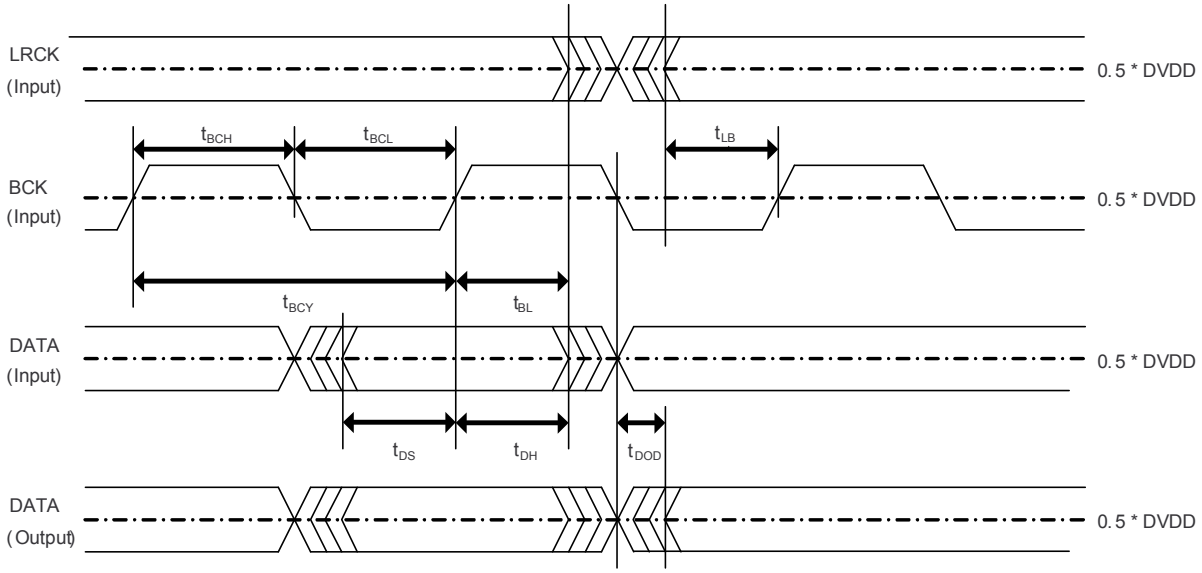


Figure 5. PCM5242 Serial Audio Timing - Slave

In software mode, the PCM5242 can act as an I^2S master, generating BCK and LRCK as outputs from the SCK input.

Table 3. I^2S Master Mode Registers

Register	Function
Page0, Register 9, D(0), D(4), and D(5)	I^2S Master mode select
Register 32, D(6:0)	BCK divider and LRCK divider
Register 33, D(7:0)	

The I²S master timing is shown in Figure 6.

		MIN	TYP	MAX	UNIT
t_{BCY}	BCK Pulse Cycle Time	40			ns
t_{BCL}	BCK Pulse Width LOW	16			ns
t_{BCH}	BCK Pulse Width HIGH	16			ns
t_{BCK}	BCK frequency at DVDD = 3.3V			24.576	MHz
$t_{BCK(1.8V)}$	BCK frequency at DVDD = 1.8V			12.288	MHz
t_{LRD}	LRCKx delay time from BCKx falling edge	–10		20	ns
t_{DS}	DATA Set Up Time	8			ns
t_{DH}	DATA Hold Time	8			ns
t_{DOD}	DATA delay time from BCK falling edge at DVDD = 3.3V			15	ns
$t_{DOD(1.8V)}$	DATA delay time from BCK falling edge at DVDD = 1.8V			20	ns

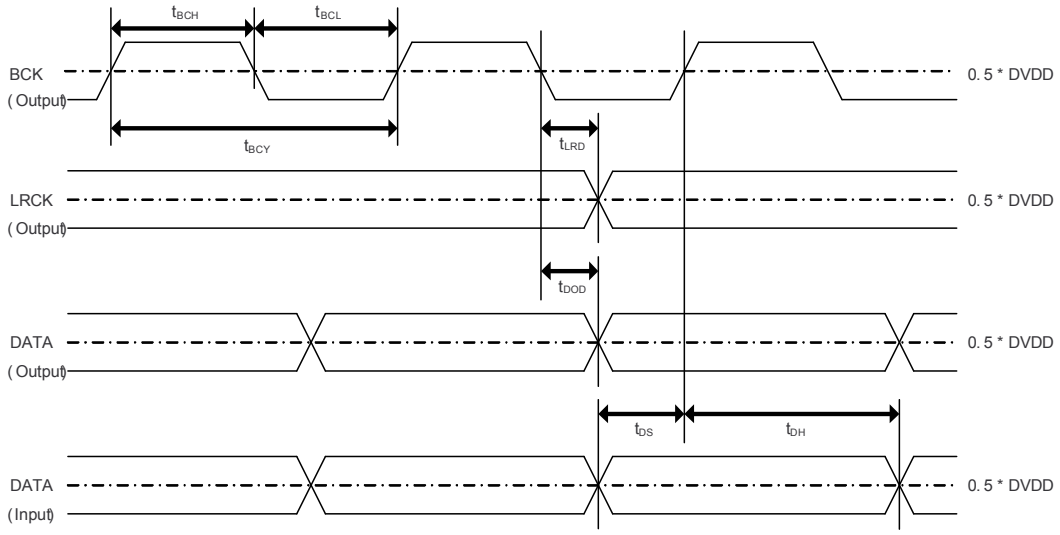


Figure 6. PCM5242 Serial Audio Timing - Master

7.9 Timing Requirements: XSMT

		MIN	TYP	MAX	UNIT
t_r	Rise time			20	ns
t_f	Fall time			20	ns

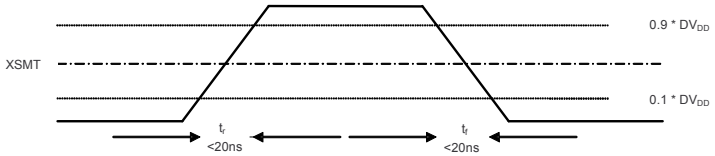


Figure 7. XSMT Timing for Soft Mute and Soft Un-Mute

7.10 Typical Characteristics

All specifications at T_A = 25°C, AV_{DD} = CPV_{DD} = DV_{DD} = 3.3V, f_S = 48kHz, system clock = 512 f_S and 24-bit data unless otherwise noted.

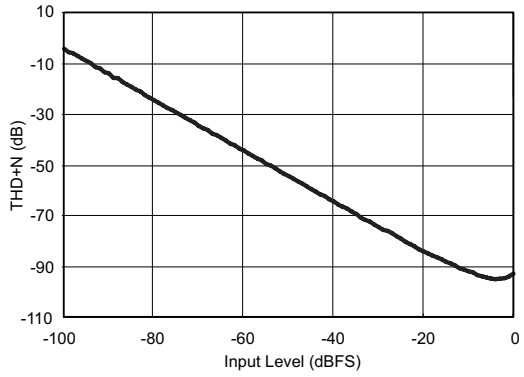


Figure 8. 1 THD+N versus Input Level

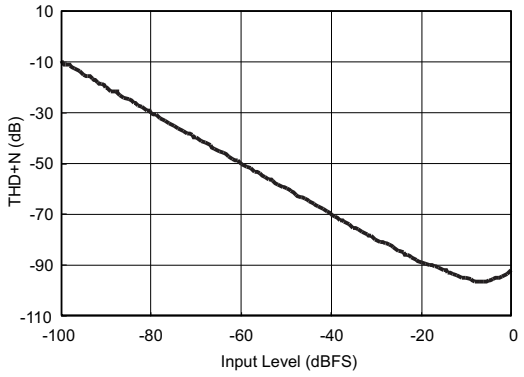


Figure 9. 2 THD+N versus Input Level

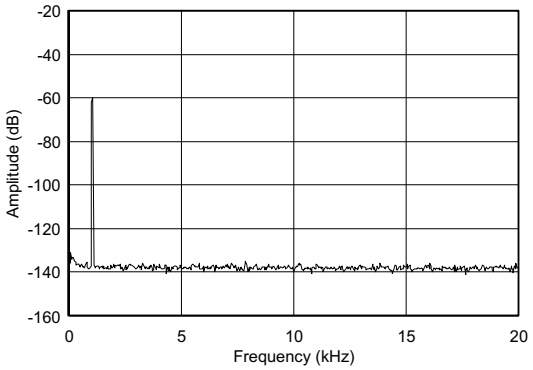


Figure 10. 1 FFT Plot At -60db Input

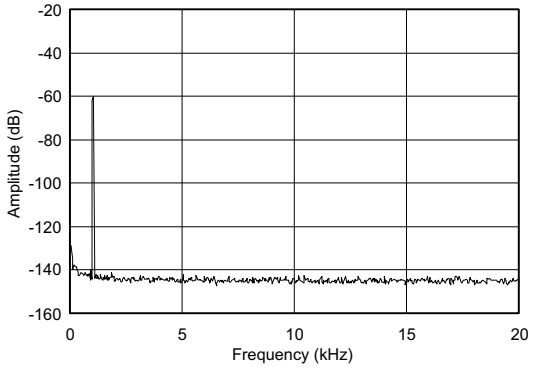


Figure 11. 2 FFT Plot At -60db Input

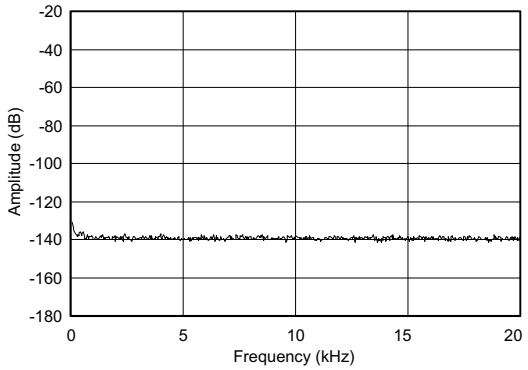


Figure 12. 1 FFT Plot At Bipolar Zero Data (BPZ)

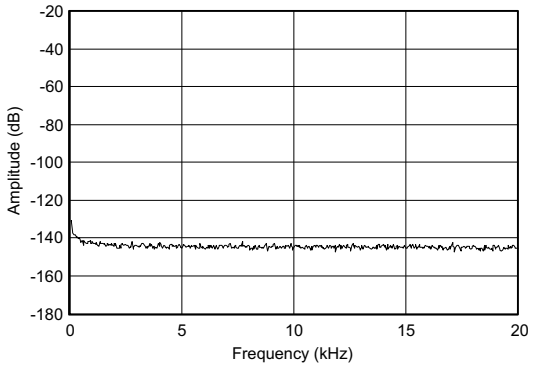


Figure 13. 2 FFT Plot at BPZ

Typical Characteristics (continued)

All specifications at T_A = 25°C, AV_{DD} = CPV_{DD} = DV_{DD} = 3.3V, f_S = 48kHz, system clock = 512 f_S and 24-bit data unless otherwise noted.

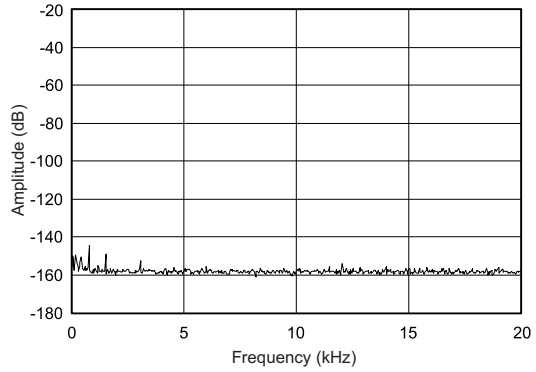


Figure 14. 1 FFT Plot at BPZ With Analog Mute (Amute)

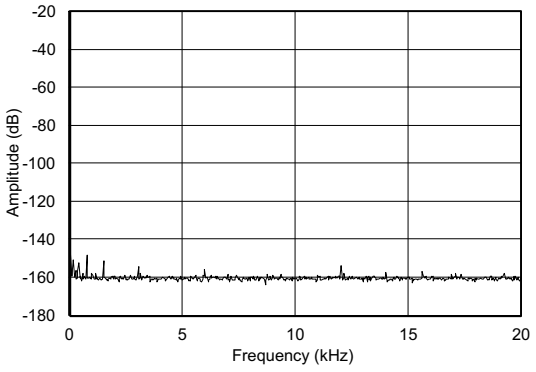


Figure 15. 2 FFT Plot at BPZ With Amute

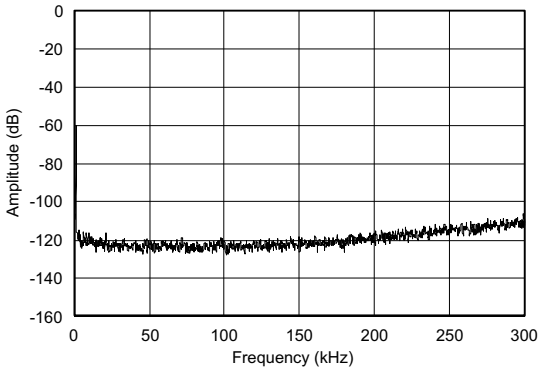


Figure 16. 1 FFT Plot at -60dB to 300khz

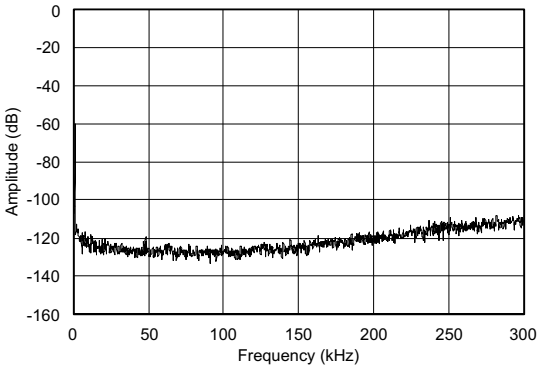


Figure 17. 2 FFT Plot at -60dB to 300khz

8 Detailed Description

8.1 Overview

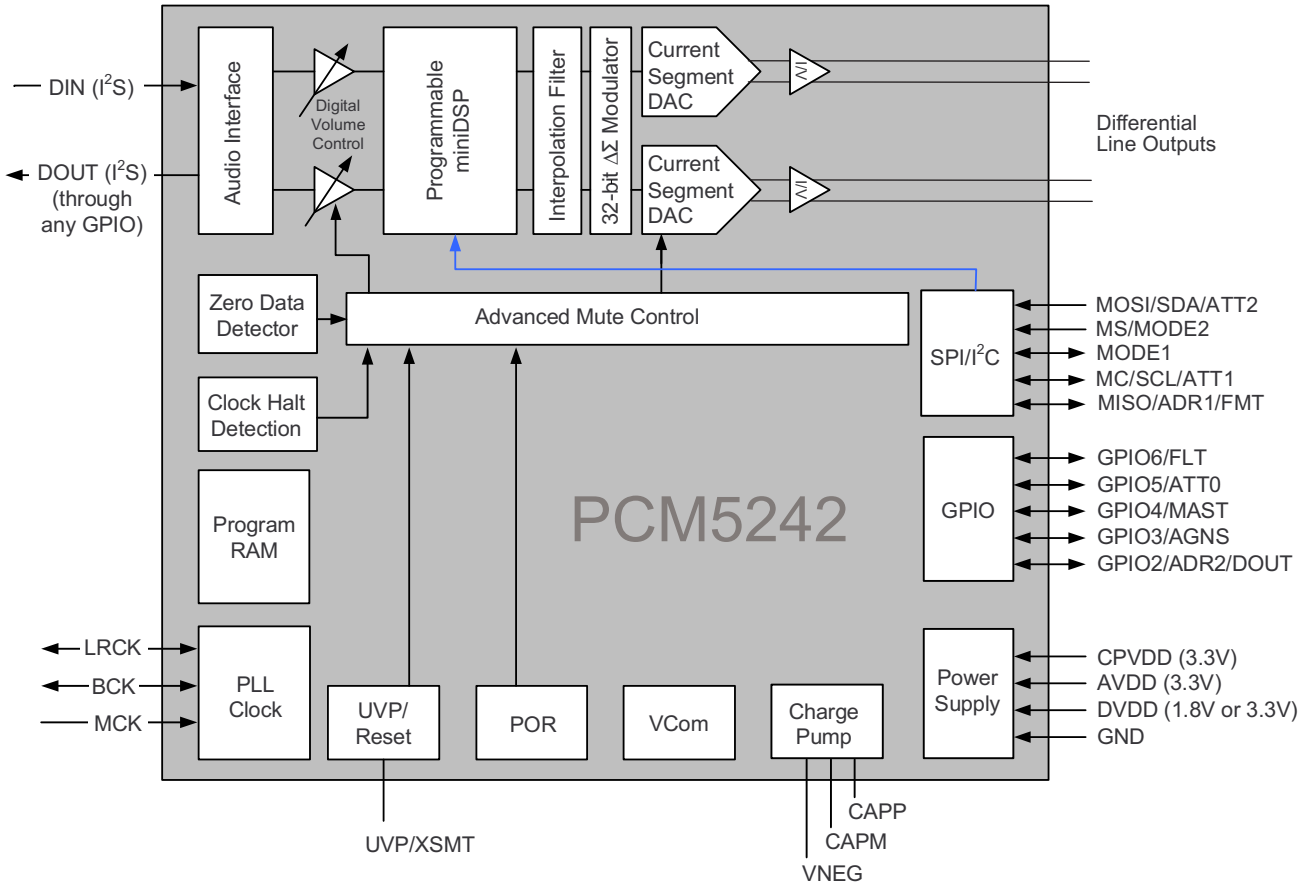
The integrated PLL on the device provided adds the flexibility to remove the system clock (commonly known as master clock), allowing a 3-wire I^2S connection and reducing system EMI. In addition, the PLL is completely programmable, allowing the device to become the I^2S clock master and drive a DSP serial port as a slave. The PLL also accepts a non-standard clock (up to 50MHz) as a source to generate the audio related clock (for example 24.576MHz).

Powersense undervoltage protection utilizes a two-level mute system. Upon clock error or system power failure, the device digitally attenuates the data (or last known good data), then mutes the analog circuit.

Compared with existing DAC technology, the PCM5242 offers up to 20dB lower out-of-band noise, reducing EMI and aliasing in downstream amplifiers/ADCs. (from traditional 100kHz OBN measurements all the way to 3MHz).

The PCM5242 accepts industry-standard audio data formats with 16- to 32-bit data. Sample rates up to 384kHz are supported.

8.2 Functional Block Diagram



8.3 Terminology

Control registers in this datasheet are given by **REGISTER BIT/BYTE NAME (Page.x HEX ADDRESS).** SE refers to "Single Ended" analog inputs, DIFF refers to "Differential" analog inputs. SCK (System Clock) and MCLK (Master Clock) are used interchangeably. Sampling frequency is symbolized by "f_S". Full scale is symbolized by "FS". Sample time as a unit is symbolized by "t_S".

8.4 Audio Data Interface

8.4.1 Audio Serial Interface

The audio interface port is a 3-wire serial port with the signals LRCK, BCK, and DIN. BCK is the serial audio bit clock, used to clock the serial data present on DIN into the serial shift register of the audio interface. Serial data is clocked into the PCM5242 on the rising edge of BCK. LRCK is the serial audio left/right word clock. LRCK polarity for Left/Right is given by the format selected.

Table 4. PCM5242 Audio Data Formats, Bit Depths and Clock Rates

CONTROL MODE	FORMAT	DATA BITS	MAX LRCK FREQUENCY [f_S]	SCK RATE [x f_S]	BCK RATE [x f_S]
Software Control (SPI or I^2S)	I^2S/LJ	32, 24, 20, 16	Up to 192kHz	128 – 3072	64, 48, 32
			384kHz	64, 128	64, 48, 32
	TDM/DSP	32, 24, 20, 16	Up to 48kHz	128 – 3072	125, 256
			96kHz	128 – 512	125, 256
			192kHz	128, 192, 256	128
Hardware Control	I^2S/LJ	32, 24, 20, 16	Up to 192kHz	128 – 3072	64, 48, 32
			384kHz	64, 128	64, 48, 32

The PCM5242 requires the synchronization of LRCK and system clock, but does not need a specific phase relation between LRCK and system clock.

If the relationship between LRCK and system clock changes more than ±5 SCK, internal operation is initialized within one sample period and analog outputs are forced to the bipolar zero level until resynchronization between LRCK and system clock is completed.

If the relationship between LRCK and BCK are invalid more than 4 LRCK periods, internal operation is initialized within one sample period and analog outputs are forced to the bipolar zero level until resynchronization between LRCK and BCK is completed.

8.4.2 PCM Audio Data Formats

The PCM5242 supports industry-standard audio data formats, including standard I^{2}S and left-justified. Data formats are selected via Register (Pg0Reg40). All formats require binary 2s-complement, MSB-first audio data; up to 32-bit audio data is accepted.

The PCM5242 also supports right-justified and TDM/DSP in software control mode. I^{2}S, LJ, RJ, and TDM/DSP are selected using Register (Pg0Reg40). All formats require binary 2s complement, MSB-first audio data. Up to 32 bits are accepted. Default setting is I^{2}S and 24 bit word length.

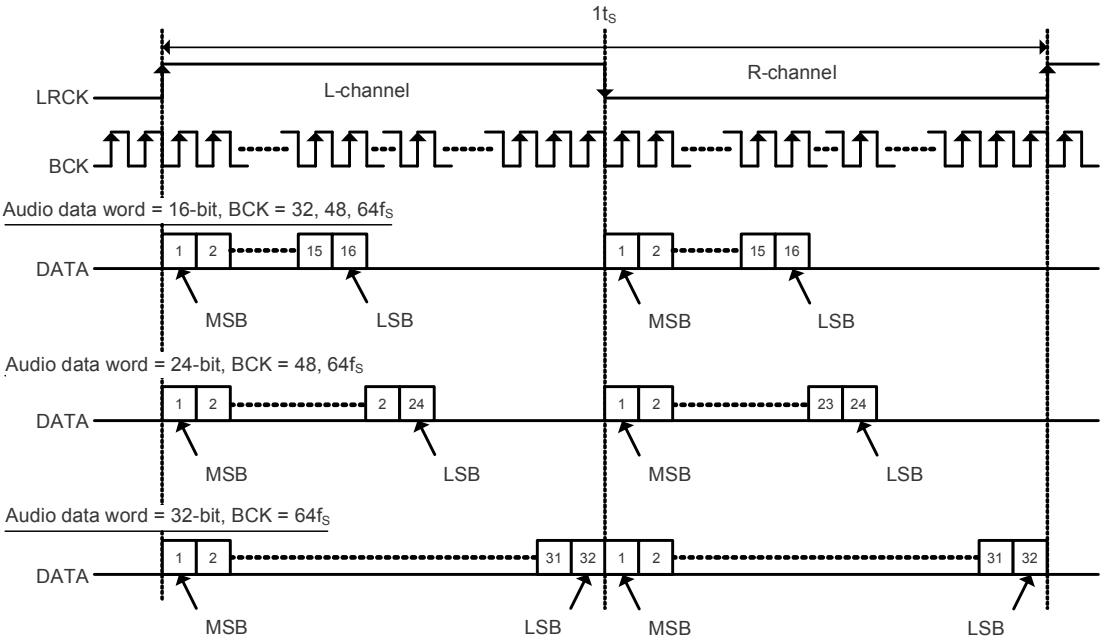
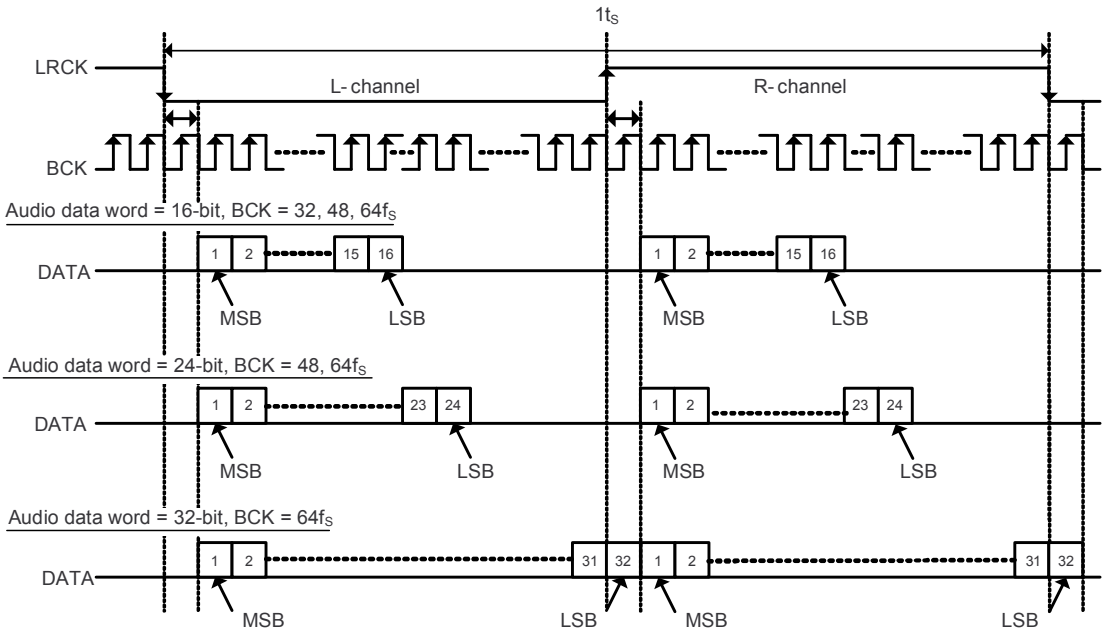


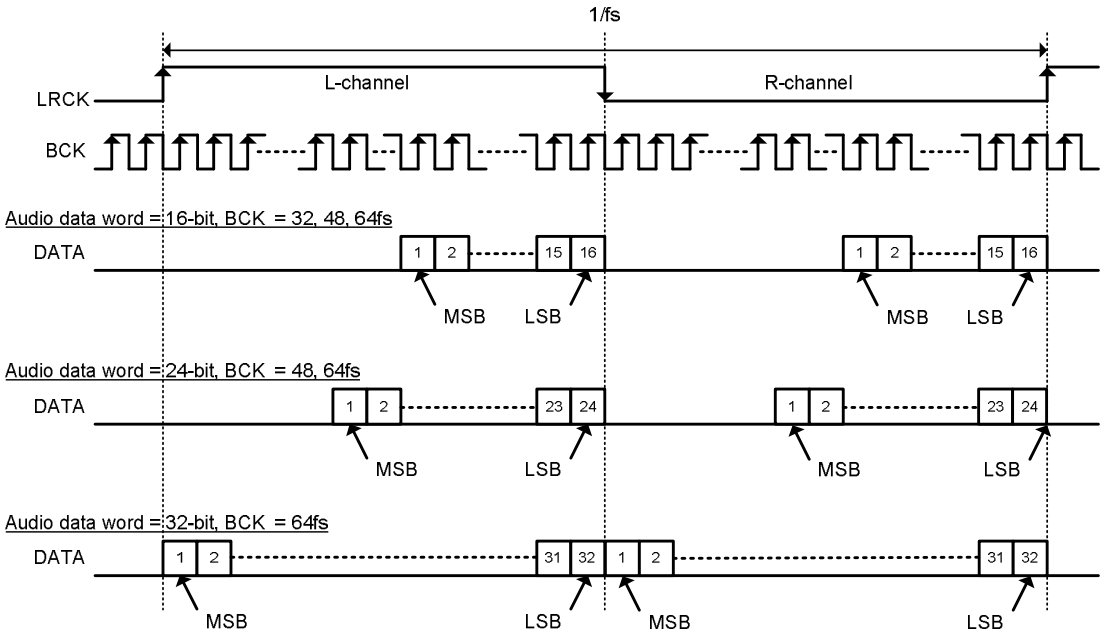
Figure 18. Left Justified Audio Data Format



I^{2}S Data Format; L-channel = LOW, R-channel = HIGH

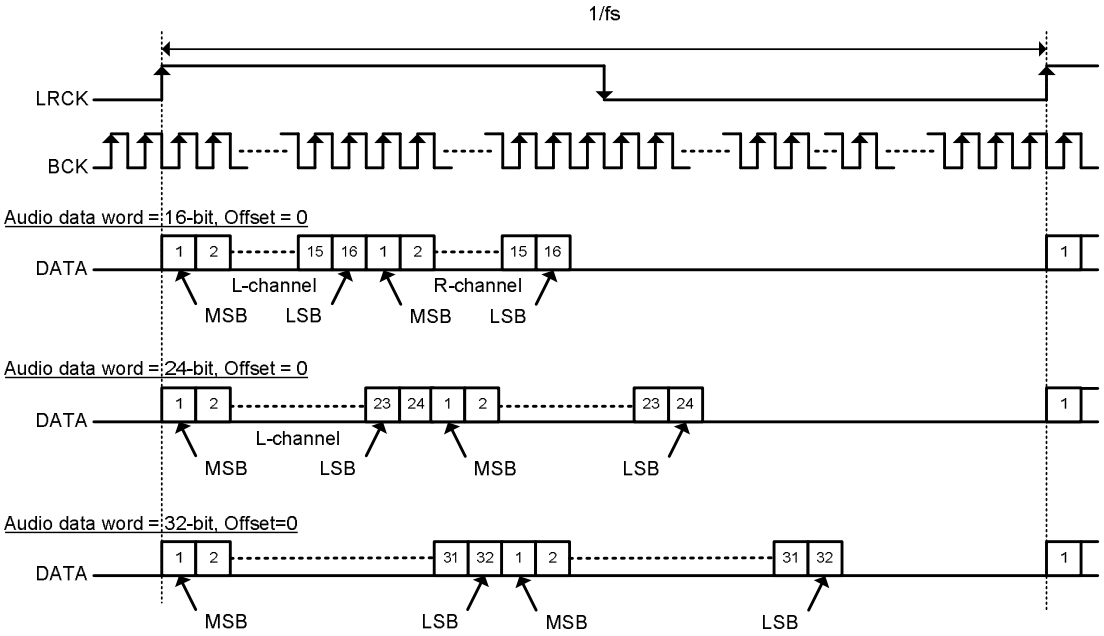
Figure 19. I^{2}S Audio Data Format

The following data formats are only available in software mode.



Right Justified Data Format; L-channel = HIGH, R-channel = LOW

Figure 20. Right Justified Audio Data Format

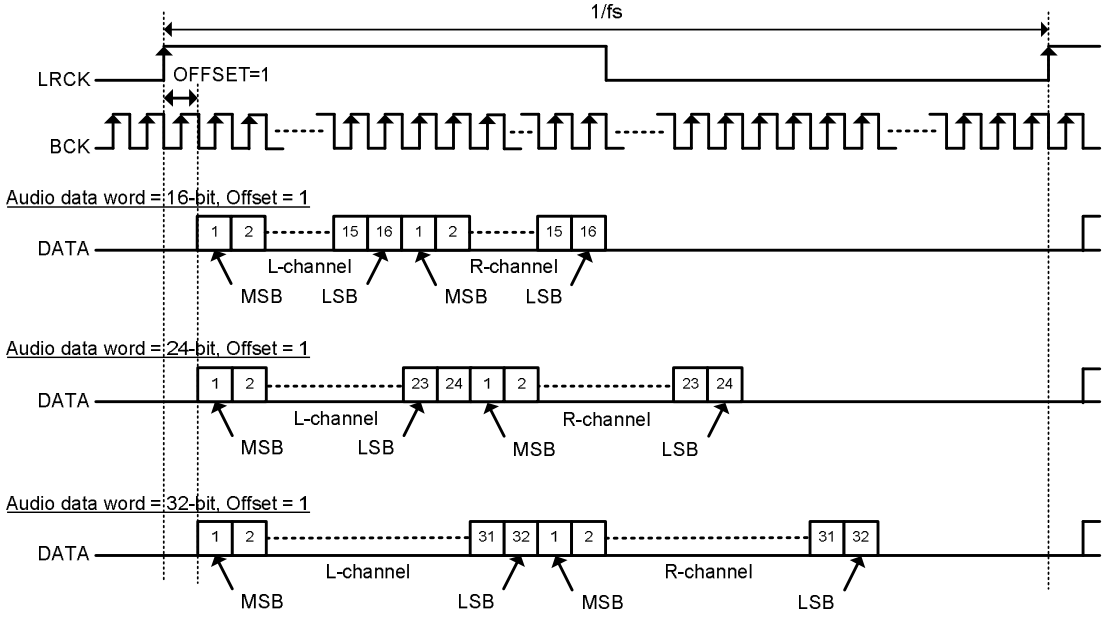


TDM/DSP Data Format; L-channel = FIRST, R-channel = LAST with OFFSET = 0

Figure 21. TDM/DSP 1 Audio Data Format

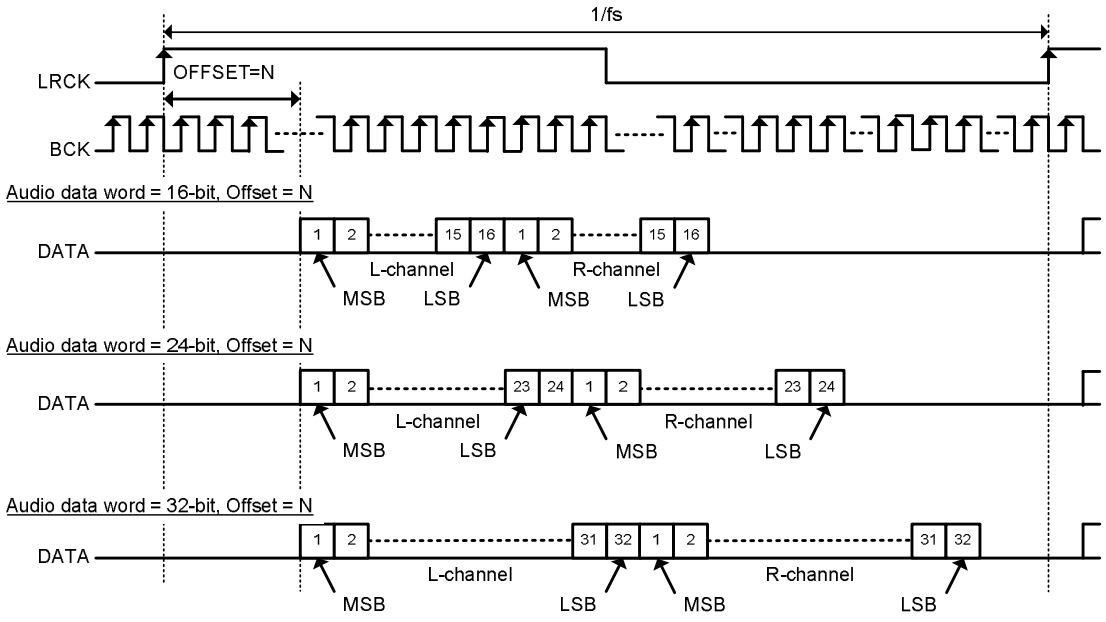
NOTE

In TDM Modes, Duty Cycle of LRCK should be 1x BCK at minimum. Rising edge is considered frame start.



TDM/DSP Data Format; L-channel = FIRST, R-channel = LAST with OFFSET = 1

Figure 22. TDM/DSP 2 Audio Data Format



TDM/DSP Data Format; L-channel = FIRST, R-channel = LAST with OFFSET = N

Figure 23. TDM/DSP 3 Audio Data Format

8.4.3 Zero Data Detect

The PCM5242 has a zero-detect function. When the device detects the continuous zero data for both left and right channels, or separate channels, Analog mutes are set to both OUTL and OUTR, or separate OUTL and OUTR. These are controlled by Page0, Register 65, D(2:1) as shown in Table 5.

Continuous Zero data cycles are counted by LRCK, and the threshold of decision for analog mute can be set by Page 0, Register 59, D(6:4) for L-ch, and D(2:0) for Rch as shown in Table 6. Default values are 0 for both channels.

In Hardware mode, the device uses default values.

Table 5. Zero Data Detection Mode

ATMUTECTL	Value	Function
Bit : 2	0	Independently L-ch or R-ch are zero data for zero data detection
	1 (Default)	Both L-ch and R-ch have to be zero data for zero data detection
Bit : 1	0	Zero detection and analog mute are disabled for R-ch
	1 (Default)	Zero detection analog mute are enabled for R-ch
Bit : 0	0	Zero detection analog mute are disabled for L-ch
	1 (Default)	Zero detection analog mute are enabled for L-ch

Table 6. Zero Data Detection Time

ATMUTETIML / ATMUTETIMR	Number of LRCKs	Time @ 48kHz
0 0 0	1024	21 ms
0 0 1	5120	106 ms
0 1 0	10240	213 ms
0 1 1	25600	533 ms
1 0 0	51200	1.066 sec
1 0 1	102400	2.133 sec
1 1 0	256000	5.333 sec
1 1 1	512000	10.66 sec

8.5 XSMT Pin (Soft Mute / Soft Un-Mute)

An external digital host controls the PCM5242 soft mute function by driving the XSMT pin with a specific minimum rise time (t_r) and fall time (t_f) for soft mute and soft un-mute. The PCM5242 requires t_r and t_f times of less than 20ns. In the majority of applications, this is no problem, however, traces with high capacitance may have issues.

When the XSMT pin is shifted from high to low (3.3V to 0V), a soft digital attenuation ramp begins. -1dB attenuation is then applied every sample time from 0dBFS to - ∞. The soft attenuation ramp takes 104 samples.

When the XSMT pin is shifted from low to high (0V to 3.3V), a soft digital “un-mute” is started. 1dB gain steps are applied every sample time from - ∞ to 0dBFS. The un-mute takes 104 samples.

In systems where XSMT is not required, it can be directly connected to AVDD.

8.6 Audio Processing

8.6.1 PCM5242 Audio Processing Options

8.6.1.1 Overview

The PCM5242 features a fully-programmable miniDSP core. The algorithms for the miniDSP must be loaded into the device after power up. The miniDSP has direct access to the digital stereo audio stream, offering the possibility for advanced DSP algorithms with very low group delay. The miniDSP can run up to 1024 instructions on every audio sample at a 48kHz sample rate.

The PCM5242 features a programmable miniDSP core that offers Hybrid-Flows which are a RAM/ROM combination of code. Common functions are embedded in ROM, and custom RAM flows, created by TI can be run on the miniDSP core. The algorithms for the miniDSP must be loaded into the device after power up. The miniDSP can run up to 1024 instructions on every audio sample at a 48kHz sample rate. Development is done using Purepath Console software.

NOTE

At higher sampling frequencies, fewer instruction cycles are available. (For example, 512 instructions can be done in a 96kHz frame.)

The PCM5242 supports two different code sources. ROM based process flow (See the next section for how to select) and RAM based process flow. In program 31 (RAM based), different algorithms can be called from ROM - such as EQ, DRC and Zero Crossing volume control. Please see the PurePath Studio Development Environment for more details.

8.6.1.2 miniDSP Instruction Register

Registers on Page 152-169 are 25-bit instructions for the miniDSP engine. For details see Table 49. 7 bits of Instr(32:25) in Base register +0 are reserved bits. 1 bit of Instr(24) - (LSB) in Base register +0 is MSB bit of 25 bit instruction. These instructions control miniDSP operation. When the fully programmable miniDSP mode is enabled and the DAC channel is powered up, the read and write access to these registers is disabled.

8.6.1.3 Digital Output

The PCM5242 supports an SDOUT output. This can be selected within the process flow, and driven out of a GPIO pin selected in the register map (e.g. Page 0 / Register 80). Users should note that the I^2S output will be attenuated by 0.5dB. A full scale (FS) output will actually be FS-0.5dB. This can be compensated for within the process flow using PurePath Studio. The I^2S output can be a separate audio stream to the analog DAC output, allowing 2.1 and 2.2 systems to be implimented. By default, the SDOUT is not linked to the volume control registers on Page 0 / Register 60, 61, 62. However, it is possible to configure the SDOUT component in Purepath studio to mirror that register.

8.6.1.4 Software

Software development for the PCM5242 is supported through TI's comprehensive PurePath Console; a powerful, easy-to-use tool designed specifically to simplify software development on the PCM5242 miniDSP audio platform. The Graphical Development Environment consists of number of Hybrid Flows that can be downloaded to the device and run on the miniDSP.

Please visit the PCM5242 product folder on www.ti.com to learn more about PurePath Console and the latest status on available, ready-to-use DSP algorithms.

Audio Processing (continued)

8.6.2 Interpolation Filter

The PCM5242 provides 4 types of interpolation filters, selectable by writing to Page 0, Register 43, D(4:0).

Additional RAM based Hybrid Flows can be implemented by selecting Program 31, and downloading instructions and coefficients to the device.

Table 7. ROM Preset Programs

Program number	D(4:0)	Description	Minimum Cycles
0	0 0000	Reserved	
1	0 0001	Normal x8/x4/x2/x1 Interpolation Filter(1)	256
2	0 0010	Low Latency x8/x4/x2/x1 Interpolation Filter(1)	256
3	0 0011	High Attenuation x8/x4/x2 Interpolation Filter(1)	512
4	0 0100	Reserved	
5	0 0101	Preset Process Flow	n/a
6	0 0110	Reserved	
7	0 0111	Asymmetric FIR Interpolation Filter(1)	512
:	:	Reserved	
31	1 1111	RAM program / Hybrid Flows	

(1) f_S 44.1kHz De-emphasis filter is supported.

The PCM5242supports four sampling modes (single rate, dual rate, quad rate, and octal rate) which produce different oversampling rates (OSR) in the interpolation digital filter operation. These are shown in Table 8.

Table 8. Sampling Modes and Oversampling Rates

Sampling Mode	Sampling Frequency (f_S) kHz	Oversampling Rate (OSR)
Single Rate	8	8 or 16
	16	
	32	
	44.1	
	48	
Dual Rate	88.2	4
	96	
Quad Rate	176.4	2
	192	
Octal Rate	384	1 (Bypass)

Table 9. Normal x8 Interpolation Filter, Single Rate

Parameter	Condition	Value (Typical)	Value (Max)	Units
Filter Gain Pass Band	0 ……. $0.45f_S$		±0.01	dB
Filter Gain Stop Band	$0.55f_S$ ….. $7.455f_S$	–60		dB
Filter Group Delay		$20t_S$		S

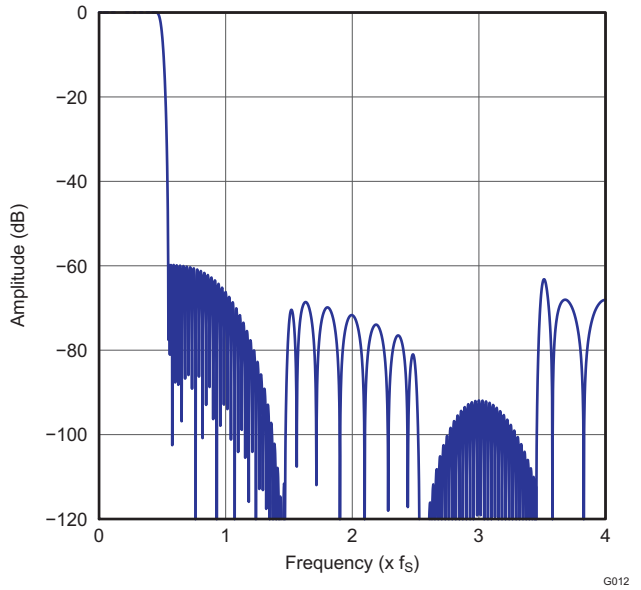


Figure 24. Normal x8 Interpolation Filter Frequency Response

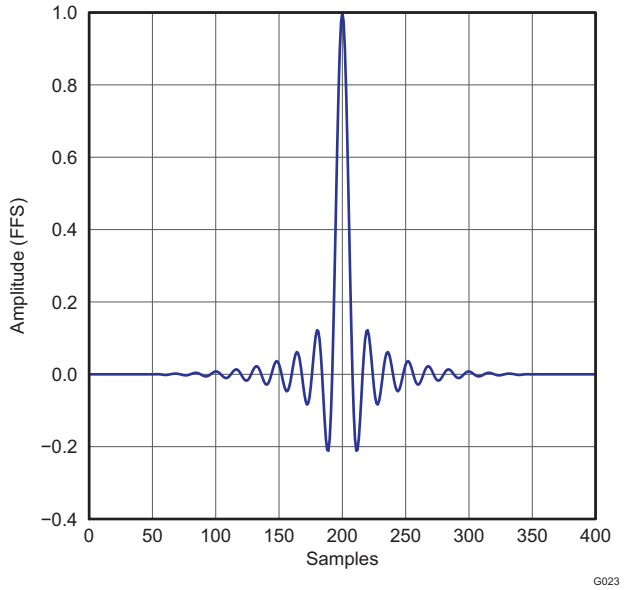


Figure 25. Normal x8 Interpolation Filter Impulse Response

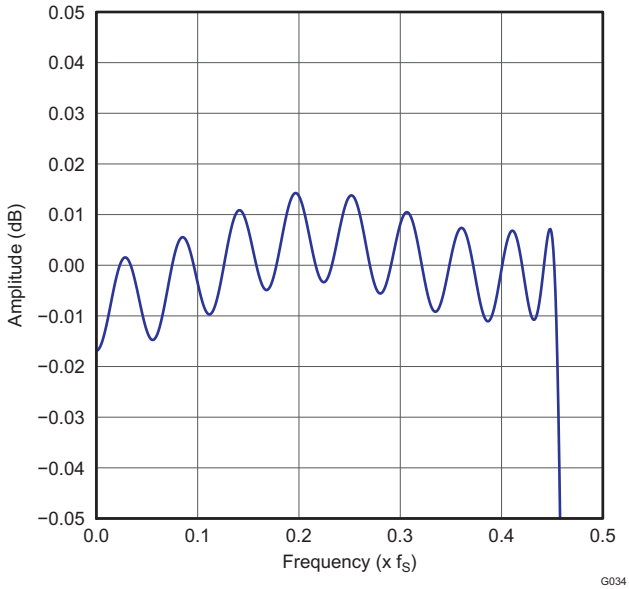


Figure 26. Normal x8 Interpolation Filter Passband Ripple

Table 10. Normal x4 Interpolation Filter, Dual Rate

Parameter	Condition	Value (Typical)	Value (Max)	Units
Filter Gain Pass Band	0 ……. $0.45f_S$		±0.01	dB
Filter Gain Stop Band	$0.55f_S$ ….. $3.455f_S$	–60		dB
Filter Group Delay		$20t_S$		S

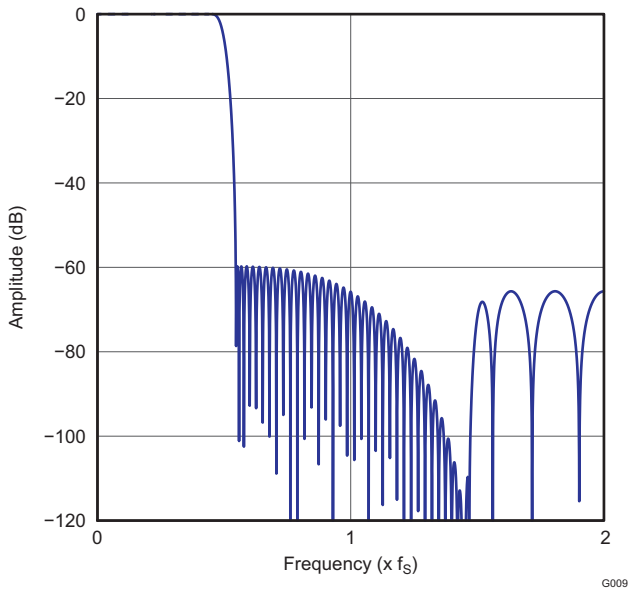


Figure 27. Normal x4 Interpolation Filter Frequency Response

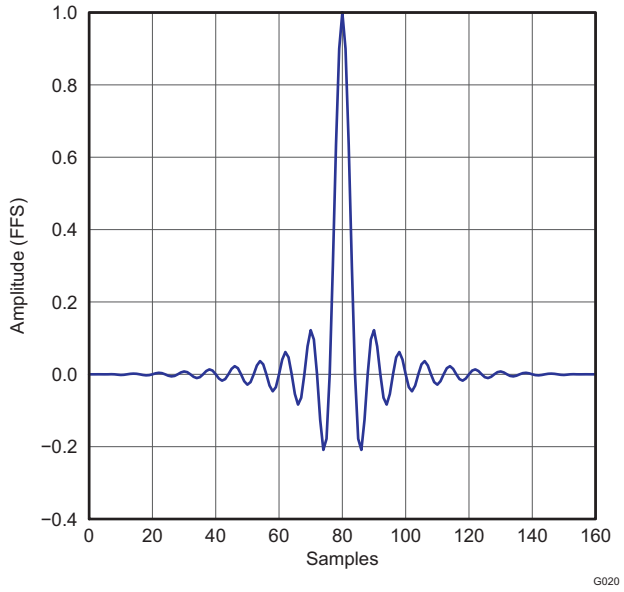


Figure 28. Normal x4 Interpolation Filter Impulse Response

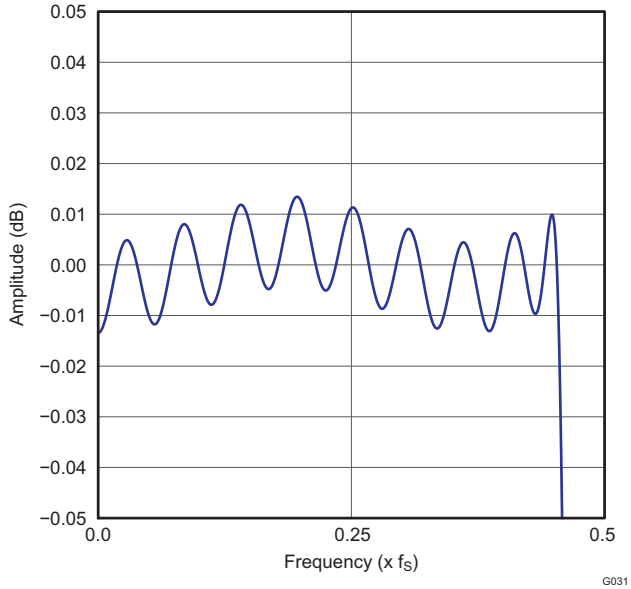


Figure 29. Normal x4 Interpolation Filter Passband Ripple

Table 11. Normal x2 Interpolation Filter, Quad Rate

Parameter	Condition	Value (Typical)	Value (Max)	Units
Filter Gain Pass Band	0 ……. $0.45f_S$		±0.01	dB
Filter Gain Stop Band	$0.55f_S$ ….. $1.455f_S$	–60		dB
Filter Group Delay		$20t_S$		S

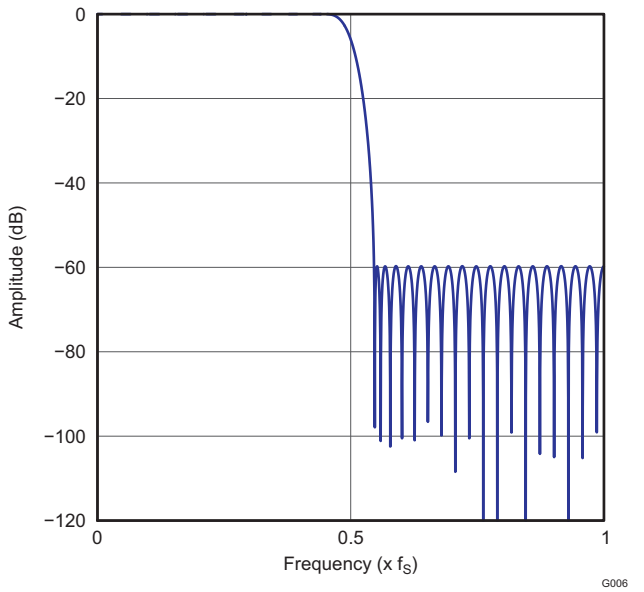


Figure 30. Normal x2 Interpolation Filter Frequency Response

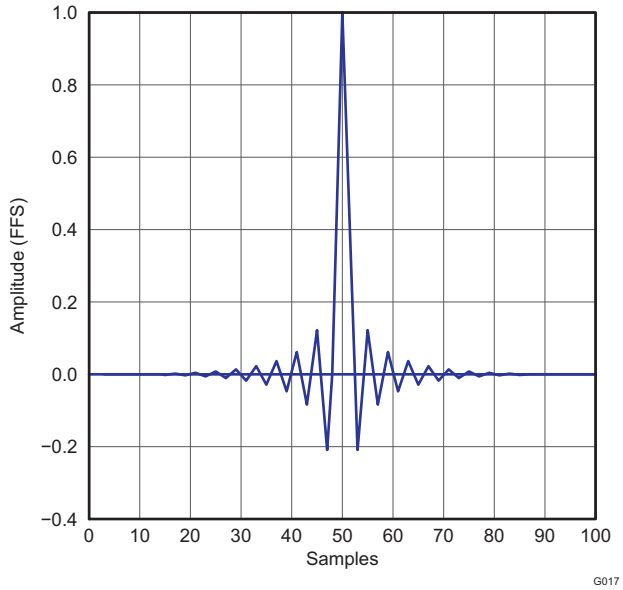


Figure 31. Normal x2 Interpolation Filter Impulse Response

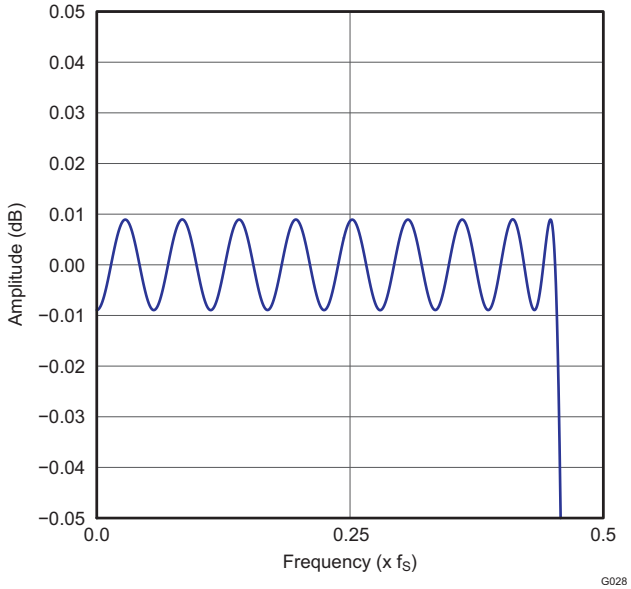


Figure 32. Normal x2 Interpolation Filter Passband Ripple

Table 12. Low latency x8 Interpolation Filter, Single Rate

Parameter	Condition	Value (Typical)	Value (Max)	Units
Filter Gain Pass Band	0 ……. $0.45f_S$		±0.001	dB
Filter Gain Stop Band	$0.55f_S$ ….. $7.455f_S$	–52		dB
Filter Group Delay		$3.5t_S$		S

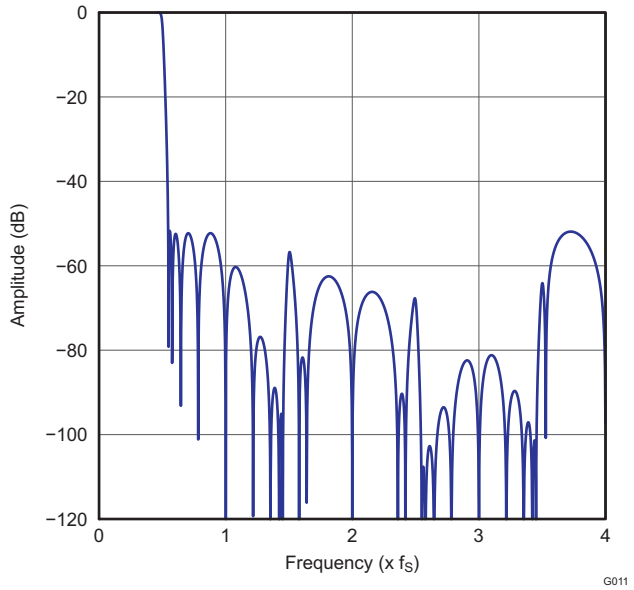


Figure 33. Low latency x8 Interpolation Filter Frequency Response

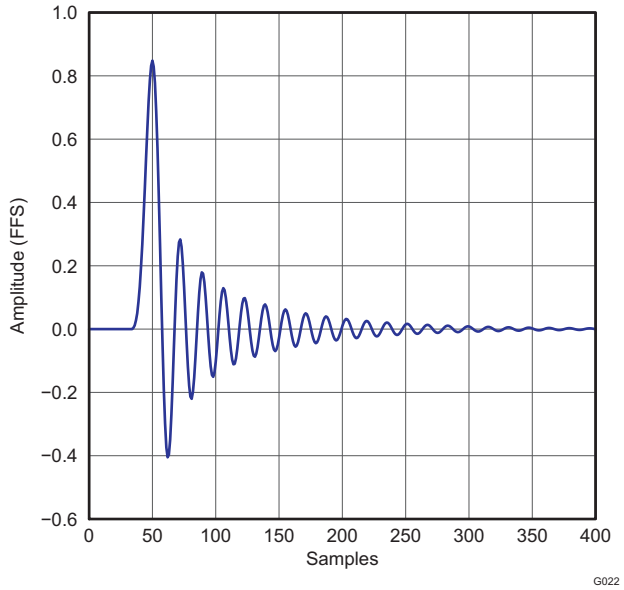


Figure 34. Low latency x8 Interpolation Filter Impulse Response

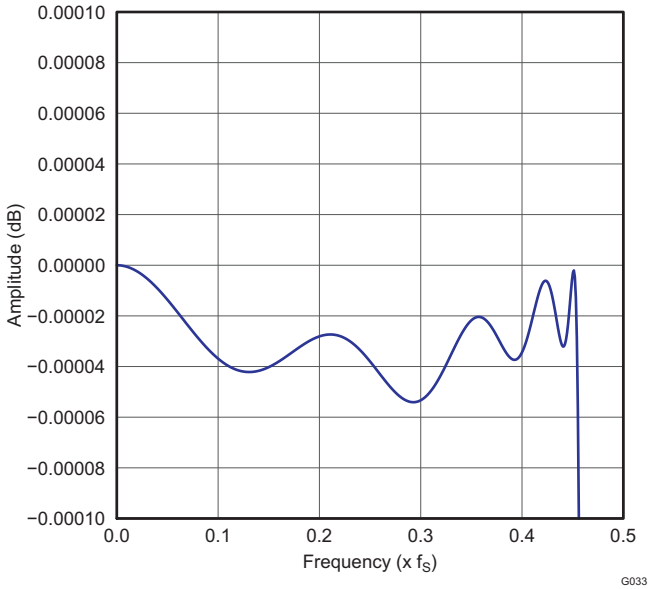


Figure 35. Low latency x8 Interpolation Filter Passband Ripple

Table 13. Low latency x4 Interpolation Filter, Dual Rate

Parameter	Condition	Value (Typical)	Value (Max)	Units
Filter Gain Pass Band	0 ……. $0.45f_S$		±0.001	dB
Filter Gain Stop Band	$0.55f_S$ ….. $3.455f_S$	–52		dB
Filter Group Delay		$3.5t_S$		S

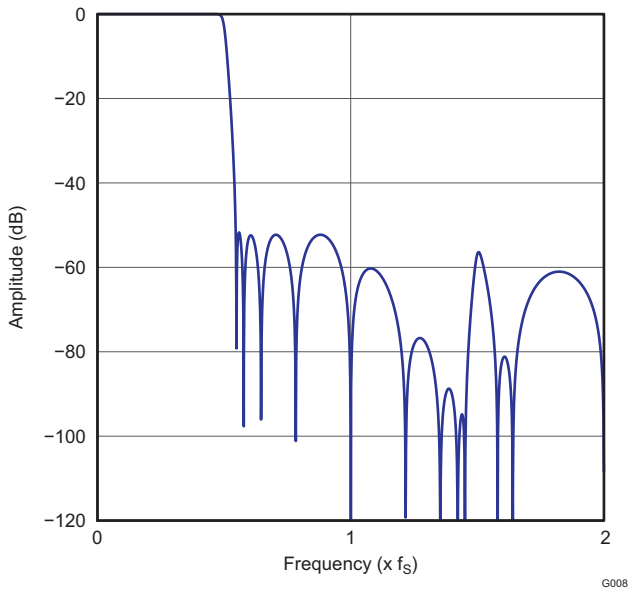


Figure 36. Low latency x4 Interpolation Filter Frequency Response

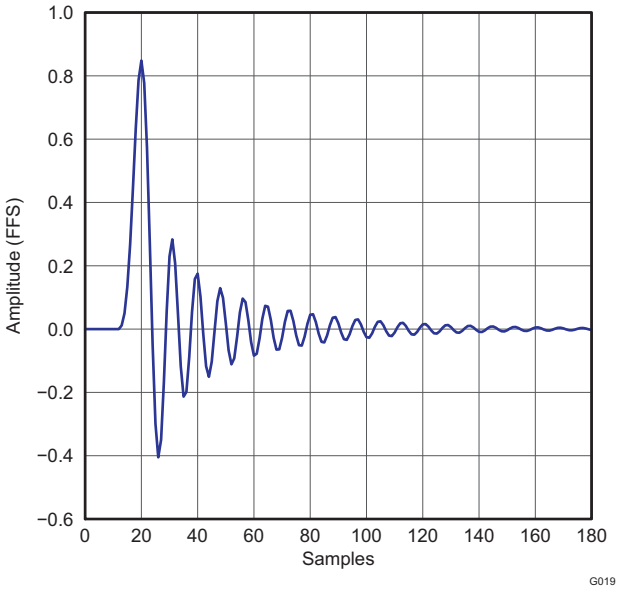


Figure 37. Low latency x4 Interpolation Filter Impulse Response

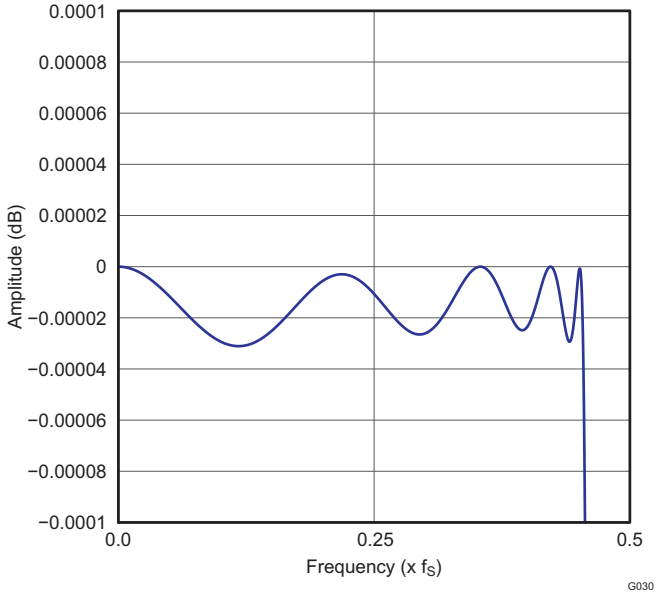


Figure 38. Low latency x4 Interpolation Filter Passband Ripple

Table 14. Low latency ×2 Interpolation Filter, Quad Rate

Parameter	Condition	Value (Typical)	Value (Max)	Units
Filter Gain Pass Band	0 ……. $0.45f_S$		±0.001	dB
Filter Gain Stop Band	$0.55f_S$ ….. $1.455f_S$	–52		dB
Filter Group Delay		$3.5t_S$		S

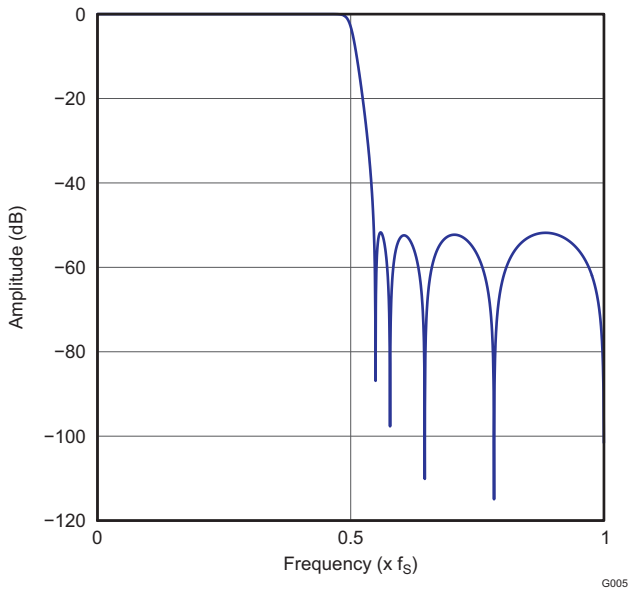


Figure 39. Low latency x2 Interpolation Filter Frequency Response

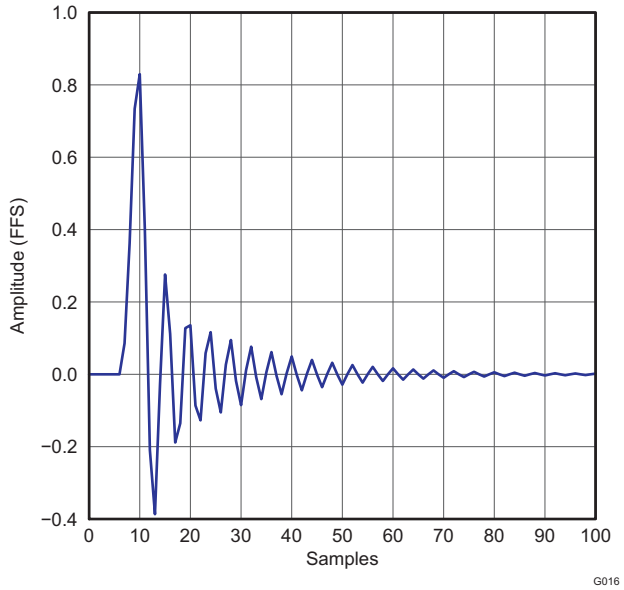


Figure 40. Low latency x2 Interpolation Filter Impulse Response

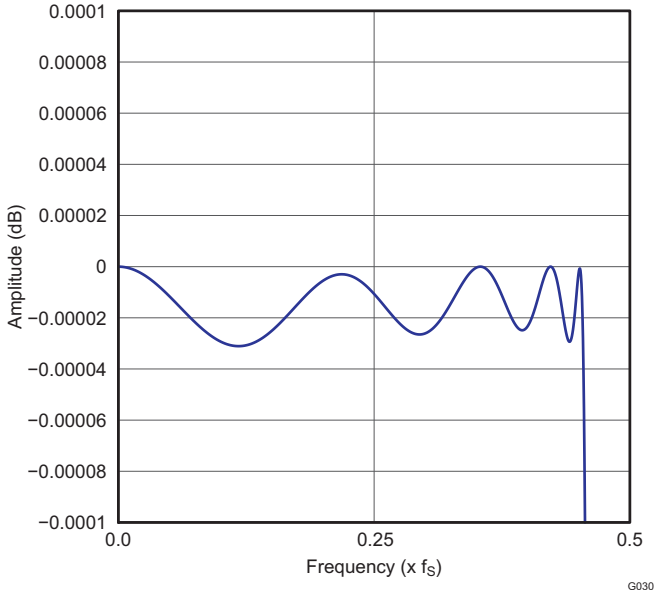


Figure 41. Low latency x2 Interpolation Filter Passband Ripple

Table 15. Asymmetric FIR x8 Interpolation Filter, Single Rate

Parameter	Condition	Value (Typical)	Value (Max)	Units
Filter Gain Pass Band	0 ……. $0.40f_S$		±0.05	dB
Filter Gain Stop Band	$0.72f_S$ ….. $7.28f_S$	–50		dB
Filter Group Delay		$1.2t_S$		S

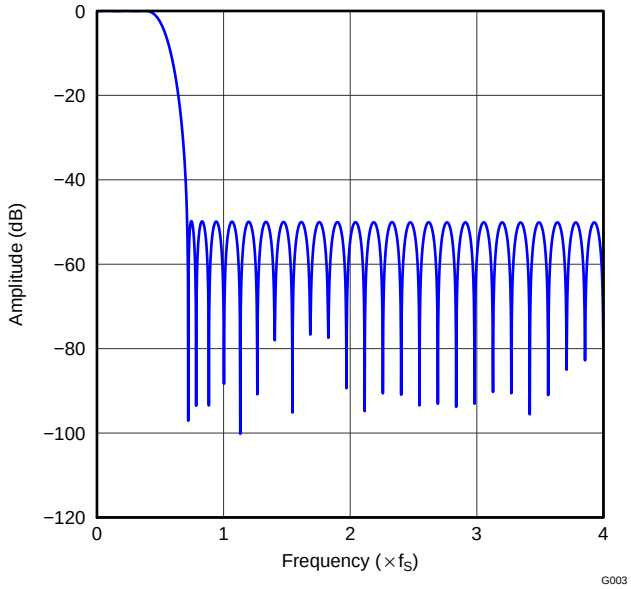


Figure 42. Asymmetric FIR x8 Interpolation Filter Frequency Response, Single Rate

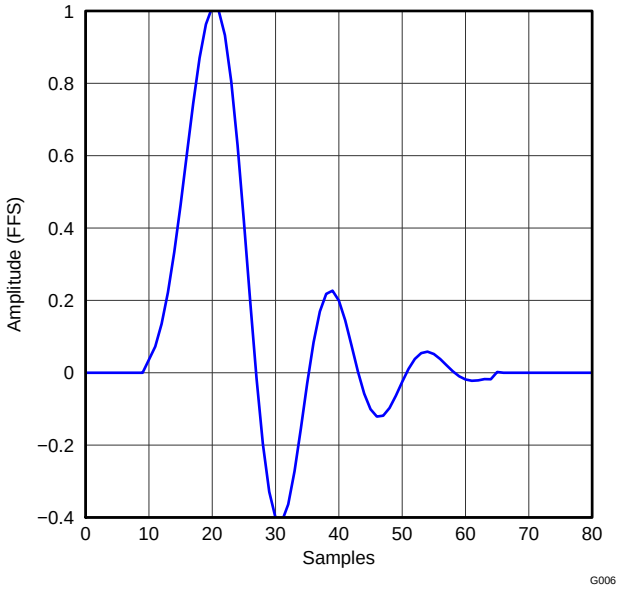


Figure 43. Asymmetric FIR x8 Interpolation Filter Impulse Response, Single Rate

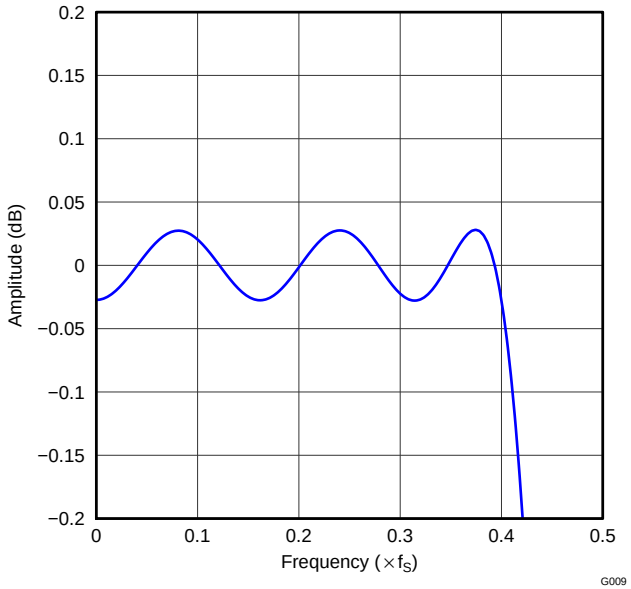


Figure 44. Asymmetric FIR x8 Interpolation Filter Passband Ripple, Single Rate

Table 16. Asymmetric FIR x4 Interpolation Filter, Dual Rate

Parameter	Condition	Value (Typical)	Value (Max)	Units
Filter Gain Pass Band	0 ……. $0.40f_S$		±0.05	dB
Filter Gain Stop Band	$0.72f_S$ ….. $3.28f_S$	–50		dB
Filter Group Delay		$1.2t_S$		S

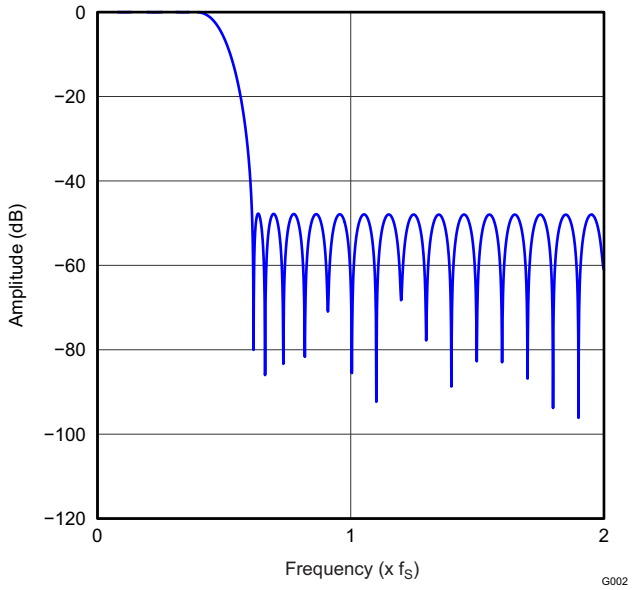


Figure 45. Asymmetric FIR x4 Interpolation Filter Frequency Response, Dual Rate

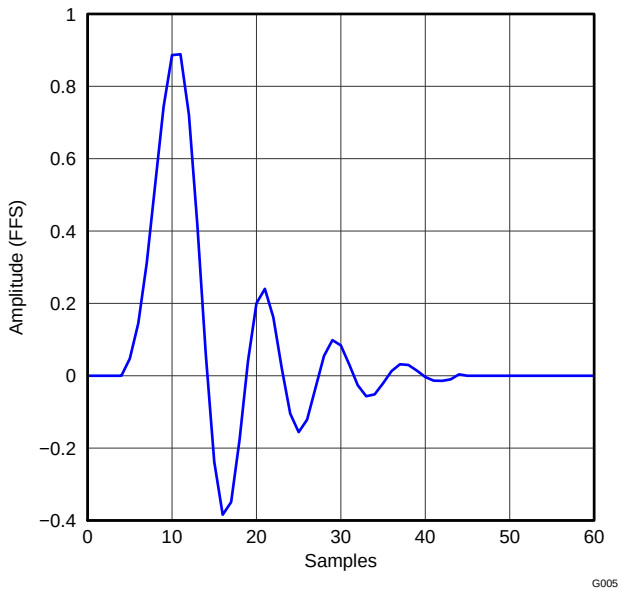


Figure 46. Asymmetric FIR x4 Interpolation Filter Impulse Response, Dual Rate

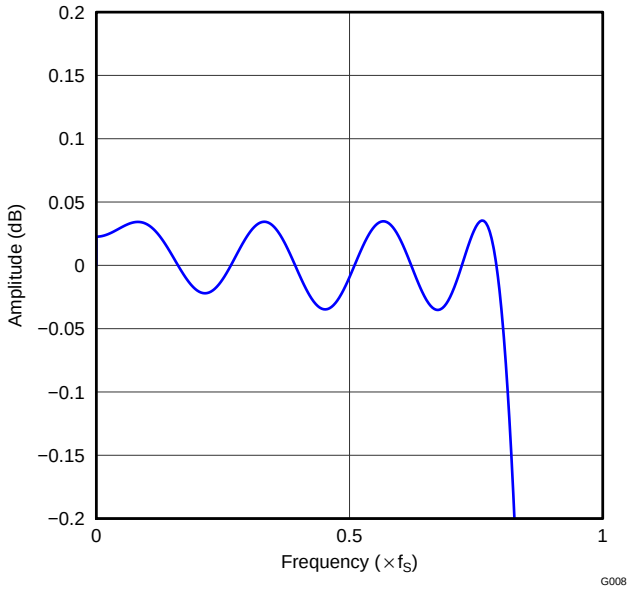


Figure 47. Asymmetric x4 Interpolation Filter Passband Ripple, Dual Rate

Table 17. Asymmetric FIR x2 Interpolation Filter, Quad Rate

Parameter	Condition	Value (Typical)	Value (Max)	Units
Filter Gain Pass Band	0 ……. $0.40f_S$		±0.05	dB
Filter Gain Stop Band	$0.72f_S$ ….. $1.28f_S$	–50		dB
Filter Group Delay		$1.2t_S$		S

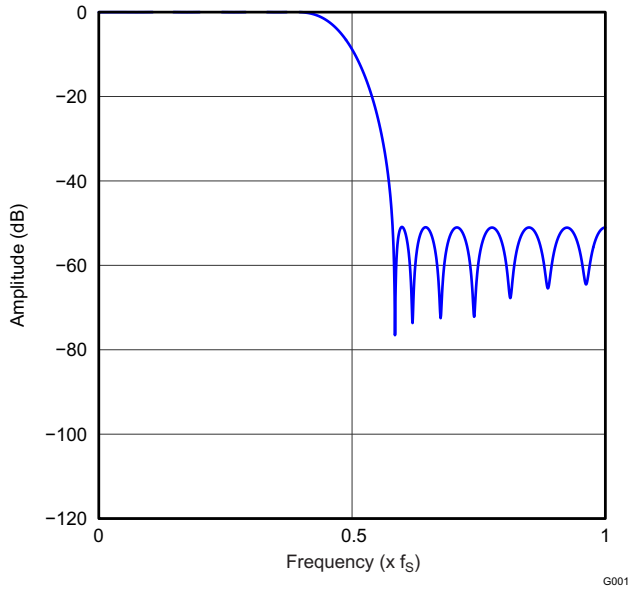


Figure 48. Asymmetric FIR x2 Interpolation Filter Frequency Response, Quad Rate

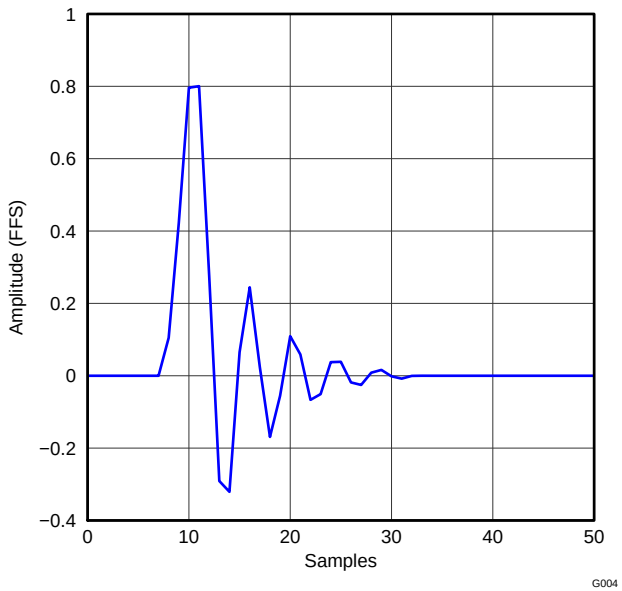


Figure 49. Asymmetric FIR x2 Interpolation Filter Impulse Response, Quad Rate

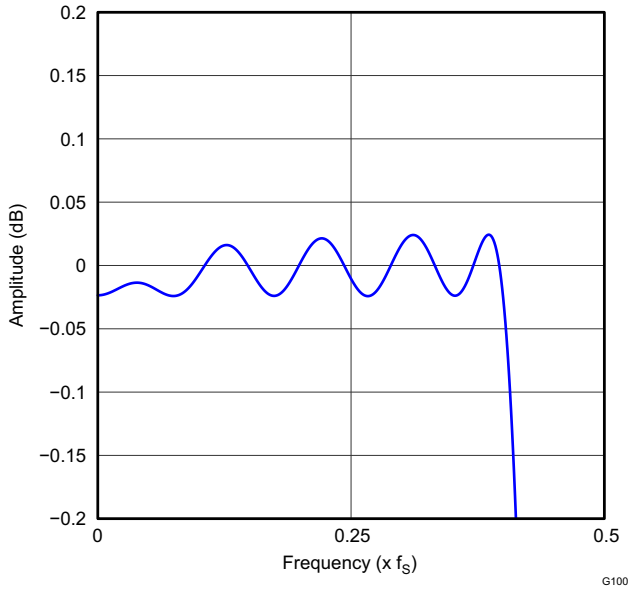


Figure 50. Asymmetric x2 Interpolation Filter Passband Ripple, Quad Rate

Table 18. High-Attentuation x8 Interpolation Filter, Single Rate

Parameter	Condition	Value (Typical)	Value (Max)	Units
Filter Gain Pass Band	0 ……. $0.45f_S$		±0.0005	dB
Filter Gain Stop Band	$0.55f_S$ ….. $7.455f_S$	–100		dB
Filter Group Delay		$33.7t_S$		S

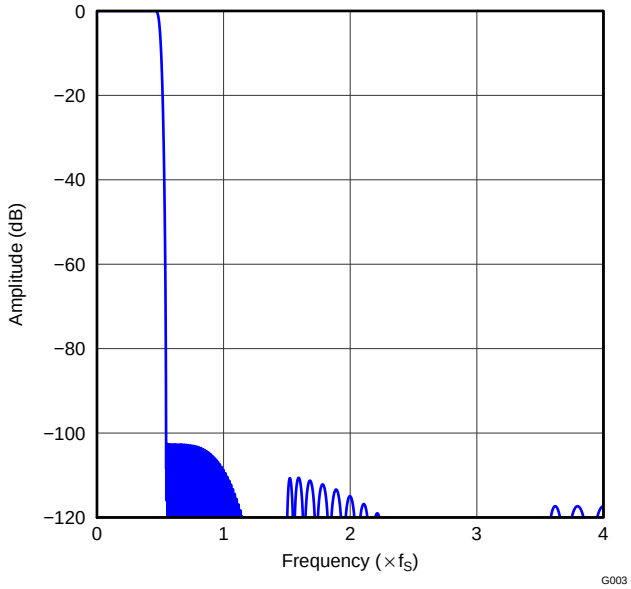


Figure 51. High-Attentuation x8 Interpolation Filter Frequency Response, Single Rate

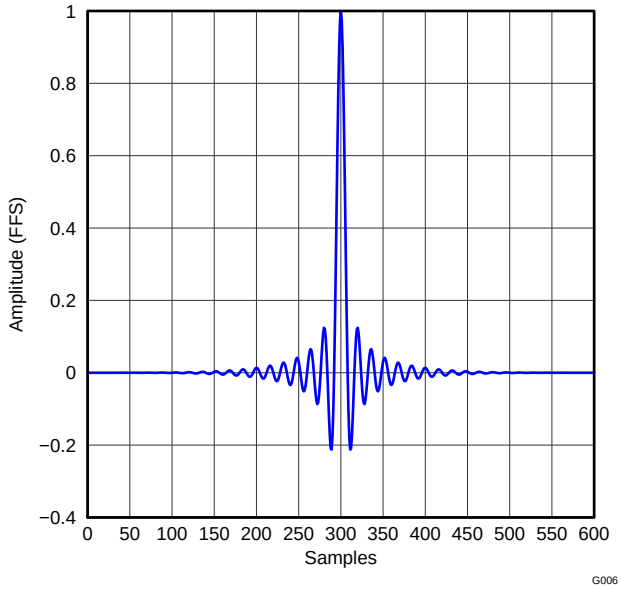


Figure 52. High-Attentuation x8 Interpolation Filter Impulse Response, Single Rate

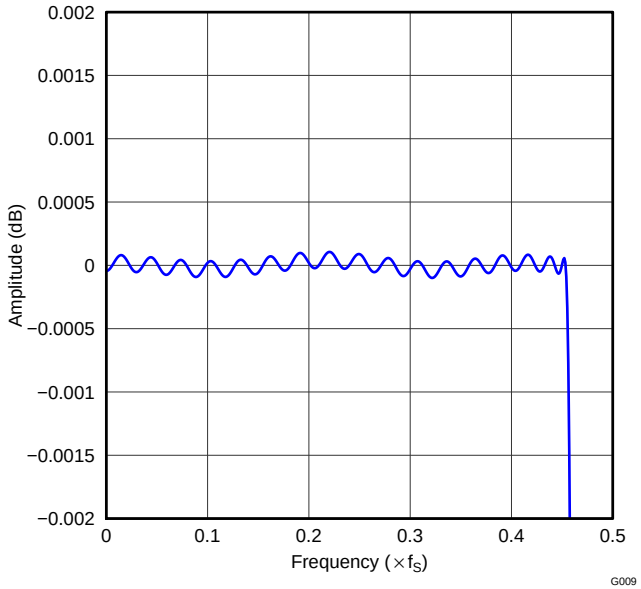


Figure 53. High-Attentuation x8 Interpolation Filter Passband Ripple, Single Rate

Table 19. High-Attentuation x4 Interpolation Filter, Dual Rate

Parameter	Condition	Value (Typical)	Value (Max)	Units
Filter Gain Pass Band	0 ……. $0.45f_S$		±0.0005	dB
Filter Gain Stop Band	$0.55f_S$ ….. $3.455f_S$	–100		dB
Filter Group Delay		$33.7t_S$		S

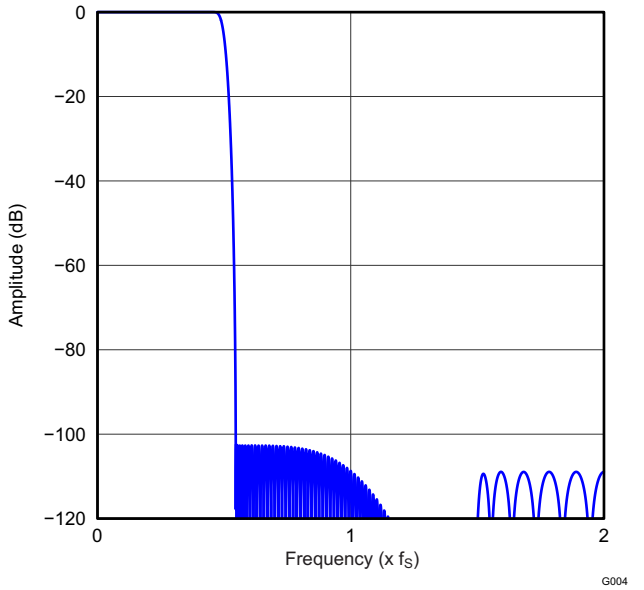


Figure 54. High-Attentuation x4 Interpolation Filter Frequency Response, Dual Rate

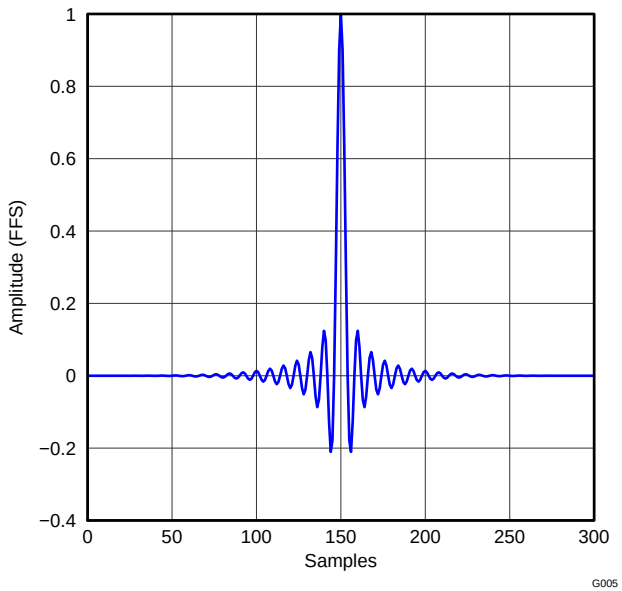


Figure 55. High-Attentuation x4 Interpolation Filter Impulse Response, Dual Rate

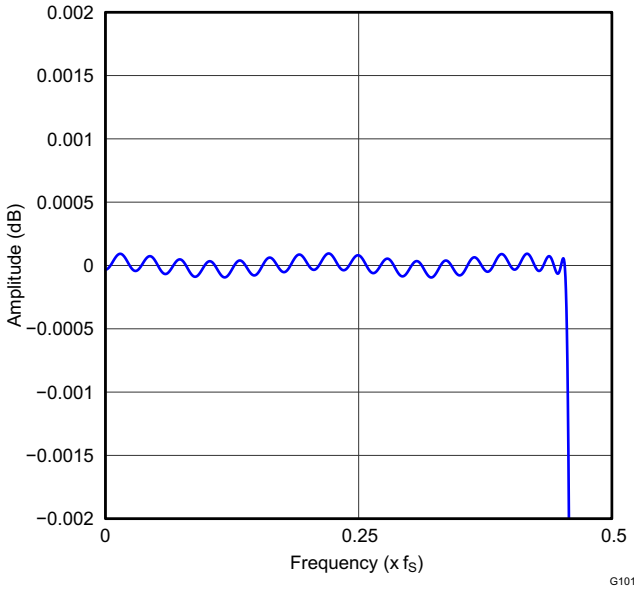


Figure 56. High-Attentuation x4 Interpolation Filter Passband Ripple, Dual Rate

Table 20. High-Attentuation x2 Interpolation Filter, Quad Rate

Parameter	Condition	Value (Typical)	Value (Max)	Units
Filter Gain Pass Band	0 ……. $0.45f_S$		±0.0005	dB
Filter Gain Stop Band	$0.55f_S$ ….. $1.455f_S$	–100		dB
Filter Group Delay		$33.7t_S$		S

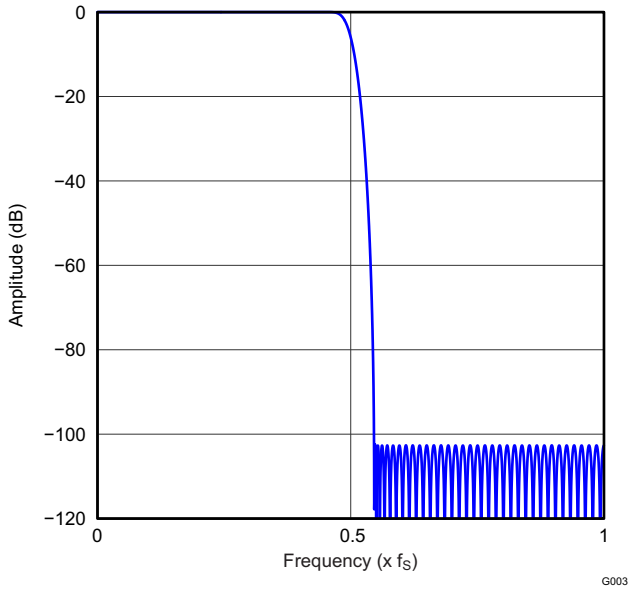


Figure 57. High-Attentuation x2 Interpolation Filter Frequency Response, Quad Rate

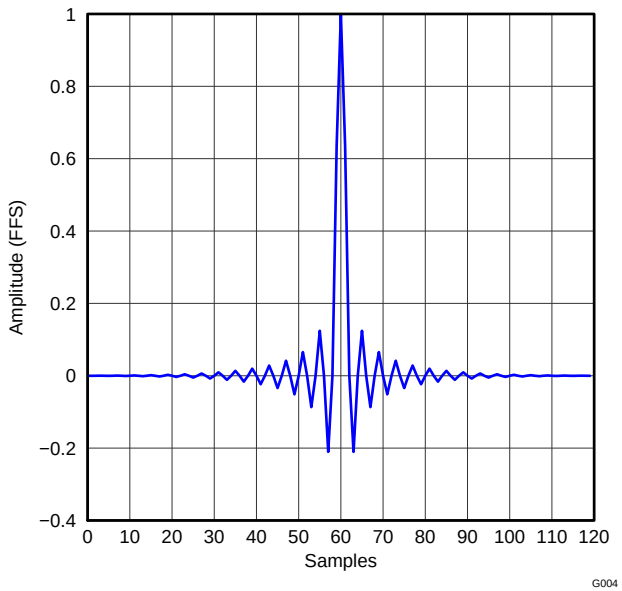


Figure 58. High-Attentuation x2 Interpolation Filter Impulse Response, Quad Rate

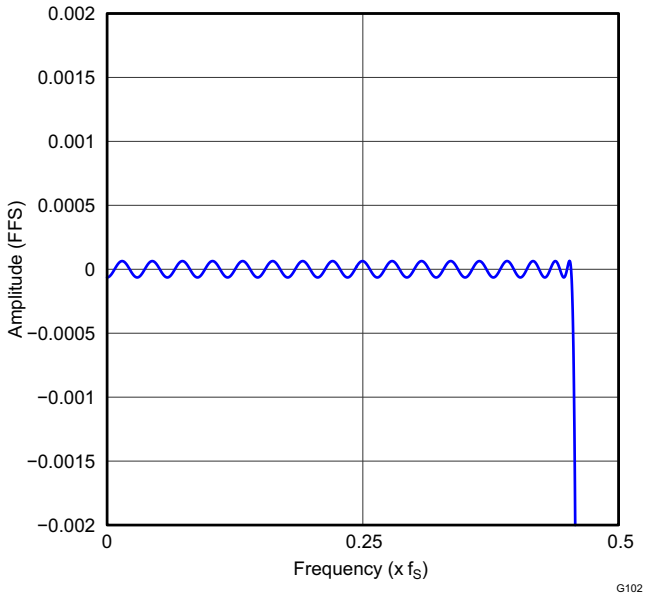


Figure 59. High-Attentuation x2 Interpolation Filter Passband Ripple, Quad Rate

8.6.3 Fixed Audio Processing Flow (Program 5)

The PCM5242 implements signal processing capabilities and interpolation filtering via processing blocks. These fixed processing blocks give users the choice of how much and what type of signal processing they may use and which interpolation filter is applied.

The signal processing blocks available are:

- Biquad filters
- Multiband DRC
- Mono mixer
- Stereo mixer
- Master volume

The addresses of the coefficients are fixed when selecting the fixed processing flow, however, if these components are used in the RAM source mode (Program 31) the registers for coefficients will change. Users can find more details in Purepath Studio.

NOTE

This process flow requires 1024 instruction cycles. Therefore, it will only function at sampling frequencies up to 48kHz.

8.6.3.1 Processing Blocks – Detailed Descriptions

Figure 60 shows the fixed processing flow.

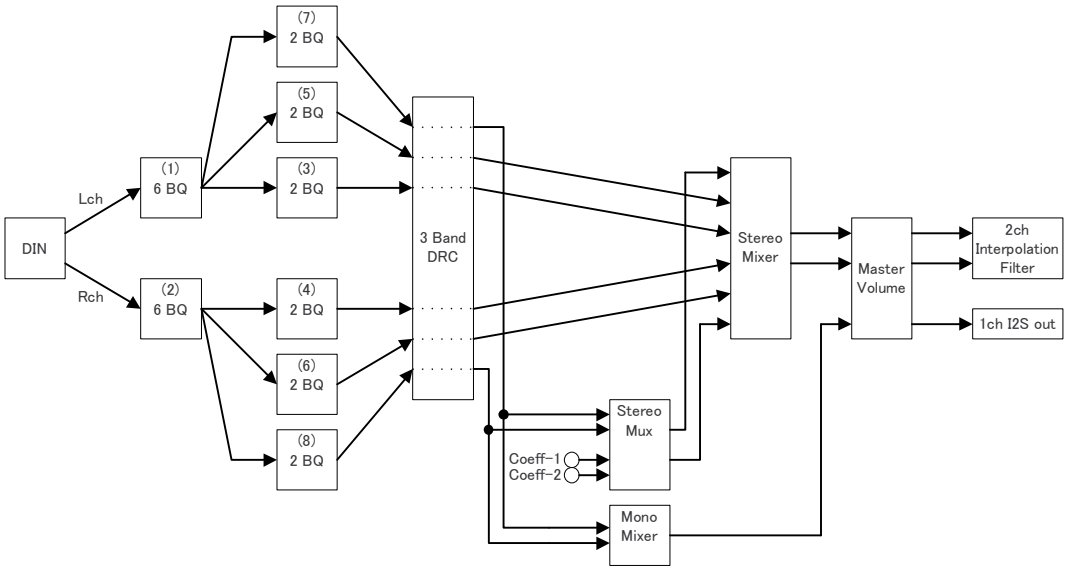


Figure 60. Preset Process Flow

Figure 61 shows a screen capture of PurePath Studio.

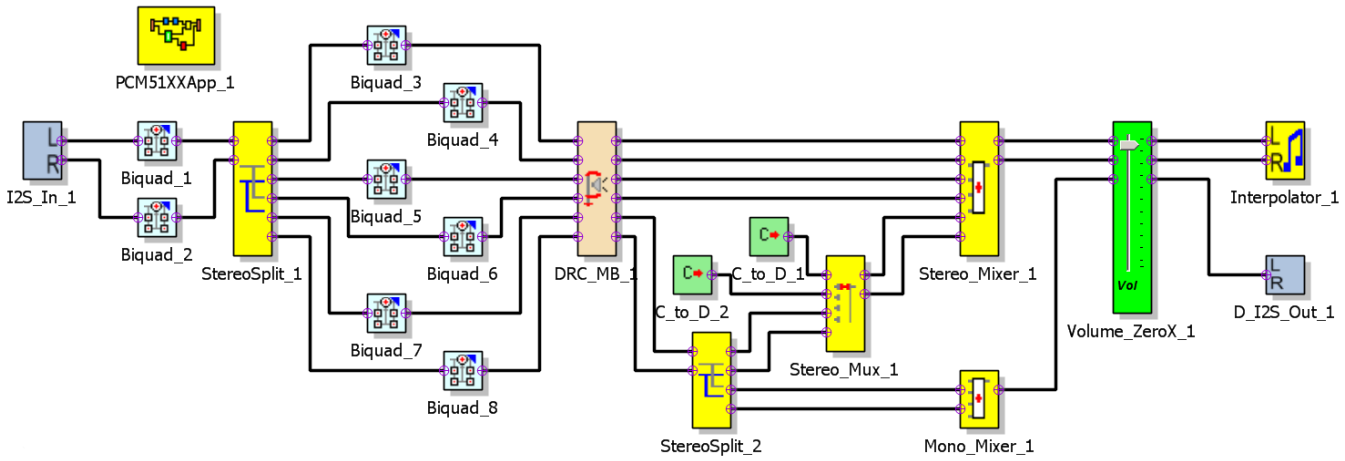


Figure 61. PurePath Studio Screen Capture

8.6.3.2 Biquad Section

The transfer function of each of the biquad filters is given by

$$H(z) = \frac{N_0 + 2N_1 z^{-1} + N_2 z^{-2}}{2^{23} - 2D_1 z^{-1} - D_2 z^{-2}} \quad (1)$$

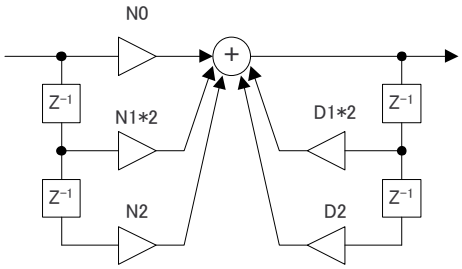


Figure 62. Biquad Block

Table 21. Biquad Filter Coefficients

Filter	Channel	Coefficient	Register
BIQUAD (1) - 1 BIQUAD (2) - 1	Lch, Rch	N0	C10 (Pg 44, Reg 48,49,50,51)
		N1	C11 (Pg 44, Reg 52,53,54,55)
		N2	C12 (Pg 44, Reg 56,57,58,59)
		D1	C13 (Pg 44, Reg 60,61,62,63)
		D2	C14 (Pg 44, Reg 64,65,66,67)
BIQUAD (1) - 2 BIQUAD (2) - 2	Lch, Rch	N0	C15 (Pg 44, Reg 68,69,70,71)
		N1	C16 (Pg 44, Reg 72,73,74,75)
		N2	C17 (Pg 44, Reg 76,77,78,79)
		D1	C18 (Pg 44, Reg 80,81,82,83)
		D2	C19 (Pg 44, Reg 84,85,86,87)

Table 21. Biquad Filter Coefficients (continued)

Filter	Channel	Coefficient	Register
BIQUAD (1) - 3 BIQUAD (2) - 3	Lch, Rch	N0	C20 (Pg 44, Reg 88,89,90,91)
		N1	C21 (Pg 44, Reg 92,93,94,95)
		N2	C22 (Pg 44, Reg 96,97,98,99)
		D1	C23 (Pg 44, Reg 100,101, 102, 103)
		D2	C24 (Pg 44, Reg 104, 105, 106, 107)
BIQUAD (1) - 4 BIQUAD (2) - 4	Lch, Rch	N0	C25 (Pg 44, Reg 108, 109, 110, 111)
		N1	C26 (Pg 44, Reg 112, 113, 114, 115)
		N2	C27 (Pg 44, Reg 116, 117, 118, 119)
		D1	C28 (Pg 44, Reg 120, 121, 122, 123)
		D2	C29 (Pg 44, Reg 124, 125, 126, 127)
BIQUAD (1) - 5 BIQUAD (2) - 5	Lch, Rch	N0	C30 (Pg 45, Reg 8, 9, 10, 11)
		N1	C31 (Pg 45, Reg 12, 13, 14, 15)
		N2	C32 (Pg 45, Reg 16, 17, 18, 19)
		D1	C33 (Pg 45, Reg 20, 21, 22, 23)
		D2	C34 (Pg 45, Reg 24, 25, 26, 27)
BIQUAD (1) - 6 BIQUAD (2) - 6	Lch, Rch	N0	C35 (Pg 45, Reg 28, 29, 30, 31)
		N1	C36 (Pg 45, Reg 32, 33, 34, 35)
		N2	C37 (Pg 45, Reg 36, 37, 38, 39)
		D1	C38 (Pg 45, Reg 40, 41, 42, 43)
		D2	C39 (Pg 45, Reg 44, 45, 46, 47)
BIQUAD (3) - 1 BIQUAD (4) - 1	Lch, Rch	N0	C40 (Pg 45, Reg 48, 49, 50, 51)
		N1	C41 (Pg 45, Reg 52, 53, 54, 55)
		N2	C42 (Pg 45, Reg 56, 57, 58, 59)
		D1	C43 (Pg 45, Reg 60, 61, 62, 63)
		D2	C44 (Pg 45, Reg 64, 65, 66, 67)
BIQUAD (3) - 2 BIQUAD (4) - 2	Lch, Rch	N0	C45 (Pg 45, Reg 68, 69, 70, 71)
		N1	C46 (Pg 45, Reg 72, 73, 74, 75)
		N2	C47 (Pg 45, Reg 76, 77, 78, 79)
		D1	C48 (Pg 45, Reg 80, 81, 82, 83)
		D2	C49 (Pg 45, Reg 84, 85, 86, 87)
BIQUAD (5) - 1 BIQUAD (6) - 1	Lch, Rch	N0	C50 (Pg 45, Reg 88, 89, 90, 91)
		N1	C51 (Pg 45, Reg 92, 93, 94, 95)
		N2	C52 (Pg 45, Reg 96, 97, 98, 99)
		D1	C53 (Pg 45, Reg 100, 101, 102, 103)
		D2	C54 (Pg 45, Reg 104, 105, 106, 107)
BIQUAD (5) - 2 BIQUAD (6) - 2	Lch, Rch	N0	C55 (Pg 45, Reg 108, 109, 110, 111)
		N1	C56 (Pg 45, Reg 112, 113, 114, 115)
		N2	C57 (Pg 45, Reg 116, 117, 118, 119)
		D1	C58 (Pg 45, Reg 120, 121, 122, 123)
		D2	C59 (Pg 45, Reg 124, 125, 126, 127)
BIQUAD (7) - 1 BIQUAD (8) - 1	Lch, Rch	N0	C60 (Pg 46, Reg 8, 9, 10, 11)
		N1	C61 (Pg 46, Reg 12, 13, 14, 15)
		N2	C62 (Pg 46, Reg 16, 17, 18, 19)
		D1	C63 (Pg 46, Reg 20, 21, 22, 23)
		D2	C64 (Pg 46, Reg 24, 25, 26, 27)

Table 21. Biquad Filter Coefficients (continued)

Filter	Channel	Coefficient	Register
BIQUAD (7) - 2 BIQUAD (8) - 2	Lch, Rch	N0	C65 (Pg 46, Reg 28, 29, 30, 31)
		N1	C66 (Pg 46, Reg 32, 33, 34, 35)
		N2	C67 (Pg 46, Reg 36, 37, 38, 39)
		D1	C68 (Pg 46, Reg 40, 41, 42, 43)
		D2	C69 (Pg 46, Reg 44, 45, 46, 47)

8.6.3.3 Dynamic Range Compression

Dynamic range compression (DRC) improves the overall listening experience. Typical music signals are characterized by crest factors (the ratio of peak signal power to average signal power) of 12dB or more. To avoid audible distortion due to clipping of peak signals, the gain of the DAC channel must be adjusted so as not to cause hard clipping. As a result, the low applied gain during nominal periods causes the perception that the signal is not loud enough. To overcome this problem, the DRC in the PCM5242 continuously monitors the output of the DAC Digital Volume control to detect its power level with respect to 0dB full-scale. When the power level is low, the DRC increases the input signal gain to make it sound louder, and reduces the gain during peaks to avoid hard clipping. The DRC enables louder audio during nominal periods with a clearer, more pleasant listening experience.

The 3-band DRC function applies DRC to 3 different mono/stereo signals with 3 different time constants. The same DRC curve is applied on all the signals, enabling a multi-band DRC solution. The underlying DRC algorithm is the same as that available with the DRC component in PurePath Studio. In this instance, the DRC gain acts on each signal in time-multiplexed order, for example, 1-2-3, 1-2-3, 1-2-3.

Table 22. DRC Coefficients

Coefficient	Register	Description
DRC_MB_1_DRC_1_DRCAE	C70 (Pg 46, Reg 48, 49, 50, 51)	
DRC_MB_1_DRC_1_DRC1AE	C71 (Pg 46, Reg 52, 53, 54, 55)	
DRC_MB_1_DRC_1_DRCAA	C72 (Pg 46, Reg 56, 57, 58, 59)	
DRC_MB_1_DRC_1_DRC1AA	C73 (Pg 46, Reg 60, 61, 62, 63)	
DRC_MB_1_DRC_1_DRCAD	C74 (Pg 46, Reg 64, 65, 66, 67)	
DRC_MB_1_DRC_1_DRC1AD	C75 (Pg 46, Reg 68, 69, 70, 71)	
DRC_MB_1_DRC_2_DRCAE	C76 (Pg 46, Reg 72, 73, 74, 75)	
DRC_MB_1_DRC_2_DRC1AE	C77 (Pg 46, Reg 76, 77, 78, 79)	
DRC_MB_1_DRC_2_DRCAA	C78 (Pg 46, Reg 80, 81, 82, 83)	
DRC_MB_1_DRC_2_DRC1AA	C79 (Pg 46, Reg 84, 85, 86, 87)	
DRC_MB_1_DRC_2_DRCAD	C80 (Pg 46, Reg 88, 89, 90, 91)	
DRC_MB_1_DRC_2_DRC1AD	C81 (Pg 46, Reg 92, 93, 94, 95)	
DRC_MB_1_DRC_3_DRCAE	C82 (Pg 46, Reg 96, 97, 98, 99)	
DRC_MB_1_DRC_3_DRC1AE	C83 (Pg 46, Reg 100, 101, 102, 103)	
DRC_MB_1_DRC_3_DRCAA	C84 (Pg 46, Reg 104, 105, 106, 107)	
DRC_MB_1_DRC_3_DRC1AA	C85 (Pg 46, Reg 108, 109, 119, 111)	
DRC_MB_1_DRC_3_DRCAD	C86 (Pg 46, Reg 112, 113, 114, 115)	
DRC_MB_1_DRC_3_DRC1AD	C87 (Pg 46, Reg 116, 117, 118, 119)	
DRC_MB_1_DRC_DRCK0	C88 (Pg 46, Reg 120, 121, 122, 123)	
DRC_MB_1_DRC_DRCK1	C89 (Pg 46, Reg 124, 125, 126, 127)	
DRC_MB_1_DRC_DRCK2	C90 (Pg 47, Reg 8, 9, 10, 11)	
DRC_MB_1_DRC_DRCMT1	C91 (Pg 47, Reg 12, 13, 14, 15)	
DRC_MB_1_DRC_DRCMT2	C92 (Pg 47, Reg 16, 17, 18, 19)	
DRC_MB_1_DRC_DRCOFF1	C93 (Pg 47, Reg 20, 21, 22, 23)	
DRC_MB_1_DRC_DRCOFF2	C94 (Pg 47, Reg 24, 25, 26, 27)	
DRC_MB_1_MinusOne_Q22	C95 (Pg 47, Reg 28, 29, 30, 31)	

Table 22. DRC Coefficients (continued)

Coefficient	Register	Description
DRC_MB_1_MinusTwo_Q22	C96 (Pg 47, Reg 32, 33, 34, 35)	
DRC_MB_1_One_M2	C97 (Pg 47, Reg 36, 37, 38, 39)	
DRC_MB_1_Zero	C98 (Pg 47, Reg 40, 41, 42, 43)	
DRC_MB_1_En_dB	C99 (Pg 47, Reg 44, 45, 46, 47)	
DRC_MB_1_Minus__Zero_dB	C100 (Pg 47, Reg 48, 49, 50, 51)	
DRC_MB_1_60_dB	C101 (Pg 47, Reg 52, 53, 54, 55)	
DRC_MB_1_Minus_60_dB	C102 (Pg 47, Reg 56, 57, 58, 59)	
DRC_MB_1_12_dB	C103 (Pg 47, Reg 60, 61, 62, 63)	
DRC_MB_1_Offset	C104 (Pg 47, Reg 64, 65, 66, 67)	
DRC_MB_1_K	C105 (Pg 47, Reg 68, 69, 70, 71)	
DRC_MB_1_x / DRC_MB_1_DRC	C106 (Pg 47, Reg 72, 73, 74, 75)	
DRC_MB_1_48_dB	C107 (Pg 47, Reg 76, 77, 78, 79)	
DRC_MB_1_Minus_48_dB	C108 (Pg 47, Reg 80, 81, 82, 83)	
DRC_MB_1_c1_3	C109 (Pg 47, Reg 84, 85, 86, 87)	
DRC_MB_1_c1_2	C110 (Pg 47, Reg 88, 89, 90, 91)	
DRC_MB_1_c1_1	C111 (Pg 47, Reg 92, 93, 94, 95)	
DRC_MB_1_c1_0	C112 (Pg 47, Reg 96, 97, 98, 99)	
DRC_MB_1_O1_1	C113 (Pg 47, Reg 100, 101, 102, 103)	
DRC_MB_1_S1_1	C114 (Pg 47, Reg 104, 105, 106, 107)	
DRC_MB_1_O1_2	C115 (Pg 47, Reg 108, 109, 119, 111)	
DRC_MB_1_S1_2	C116 (Pg 47, Reg 112, 113, 114, 115)	
DRC_MB_1_O1_3	C117 (Pg 47, Reg 116, 117, 118, 119)	
DRC_MB_1_S1_3	C118 (Pg 47, Reg 120, 121, 122, 123)	
DRC_MB_1_One_1_Q17	C119 (Pg 47, Reg 124, 125, 126, 127)	
DRC_MB_1_Scale1	C120 (Pg 48, Reg 8, 9, 10, 11)	
DRC_MB_1_x1Coeff	C121 (Pg 48, Reg 12, 13, 14, 15)	
DRC_MB_1_c2_3	C122 (Pg 48, Reg 16, 17, 18, 19)	
DRC_MB_1_c2_2	C123 (Pg 48, Reg 20, 21, 22, 23)	
DRC_MB_1_c2_1	C124 (Pg 48, Reg 24, 25, 26, 27)	
DRC_MB_1_c2_0	C125 (Pg 48, Reg 28, 29, 30, 31)	
DRC_MB_1_O2_1	C126 (Pg 48, Reg 32, 33, 34, 35)	
DRC_MB_1_S2_1	C127 (Pg 48, Reg 36, 37, 38, 39)	
DRC_MB_1_O2_2	C128 (Pg 48, Reg 40, 41, 42, 43)	
DRC_MB_1_S2_2	C129 (Pg 48, Reg 44, 45, 46, 47)	
DRC_MB_1_O2_3	C130 (Pg 48, Reg 48, 49, 50, 51)	
DRC_MB_1_S2_3	C131 (Pg 48, Reg 52, 53, 54, 55)	
DRC_MB_1_One_2_Q17	C132 (Pg 48, Reg 56, 57, 58, 59)	
DRC_MB_1_Scale2	C133 (Pg 48, Reg 60, 61, 62, 63)	
DRC_MB_1_x2Coeff	C134 (Pg 48, Reg 64, 65, 66, 67)	
DRC_MB_1_R1_1	C135 (Pg 48, Reg 68, 69, 70, 71)	
DRC_MB_1_R1_2	C136 (Pg 48, Reg 72, 73, 74, 75)	
DRC_MB_1_R2_1	C137 (Pg 48, Reg 76, 77, 78, 79)	
DRC_MB_1_R2_2	C138 (Pg 48, Reg 80, 81, 82, 83)	
DRC_MB_1_Band1_GainC	C139 (Pg 48, Reg 84, 85, 86, 87)	
DRC_MB_1_Band2_GainC	C140 (Pg 48, Reg 88, 89, 90, 91)	
DRC_MB_1_Band3_GainC	C141 (Pg 48, Reg 92, 93, 94, 95)	
DRC_MB_1_MinusOne_M1	C142 (Pg 48, Reg 96, 97, 98, 99)	

Table 22. DRC Coefficients (continued)

Coefficient	Register	Description
DRC_MB_1_One_M1	C143 (Pg 48, Reg 100, 101, 102, 103)	
DRC_MB_1_Band1_GainE	C144 (Pg 48, Reg 104, 105, 106, 107)	
DRC_MB_1_Band2_GainE	C145 (Pg 48, Reg 108, 109, 110, 111)	
DRC_MB_1_Band3_GainE	C146 (Pg 48, Reg 112, 113, 114, 115)	
DRC_MB_1_minus_One_M2	C147 (Pg 48, Reg 116, 117, 118, 119)	

8.6.3.4 Stereo Mixer

Three stereo inputs are mixed into one stereo output with input signal gain given by Equation 2.

$$Out\_L(n) = \sum (Input\_L(i,n) \bullet Gain(i)) \quad (2)$$

where

- i=1:2,3

Figure 63 and Table 23 show the strereo mixer operation.

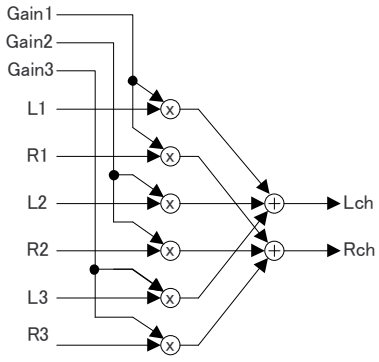


Figure 63. Stereo Mixer Block

Table 23. Stereo Mixer Coefficients

Coefficient	Register	Description
Stereo_Mixer_1_MixGain1	C148 (Pg 48, Reg 120, 121, 122, 123)	
Stereo_Mixer_1_MixGain2	C149 (Pg 48, Reg 124, 125, 126, 127)	
Stereo_Mixer_1_MixGain3	C150 (Pg 49, Reg 8, 9, 10, 11)	

8.6.3.5 Stereo Multiplexer

The Stereo Multiplexer selects one or 2 from 4 stereo input channels.

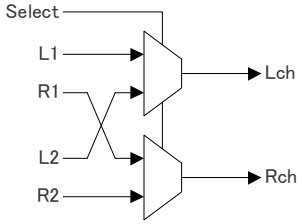


Figure 64. Stereo Multiplexer Block

Table 24. Stereo Multiplexer Select Coefficient

Coefficient	Register	Description
Stereo_Mux_1_MuxSelect	C152 (Pg 49, Reg 16, 17, 18, 19)	

Table 25. Stereo Multiplexer Input Coefficient

Coefficient	Register	Description
C_to_D_1_Coefval C_to_D_2_Coefval	C153 (Pg 49, Reg 20, 21, 22, 23)	

8.6.3.6 Mono Mixer

The Mono Mixer computes a weighted sum of 2 input channels and produces an output.

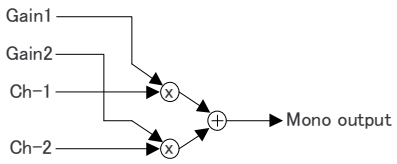


Figure 65. Mono Mixer Block

Table 26. Mono Mixer Coefficients

Coefficient	Register	Description
Mono_Mixer_1_MixGain1	C154 (Pg 49, Reg 24, 25, 26, 27)	
Mono_Mixer_1_MixGain2	C155 (Pg 49, Reg 28, 29, 30, 31)	

8.6.3.7 Master Volume Control

The Master Volume controls the volume using a linear ramp and zero crossing detection for transitions.

Table 27. Mono Mixer Coefficients

Coefficient	Register	Description
Volume_ZeroX_1_volcmd	C158 (Pg 49, Reg 40, 41, 42, 43)	
Volume_ZeroX_1_volout	C159 (Pg 49, Reg 44, 45, 46, 47)	
Volume_ZeroX_1_volout_loudness	C160 (Pg 49, Reg 48, 49, 50, 51)	
Volume_ZeroX_1_MinusOne_M2	C161 (Pg 49, Reg 52, 53, 54, 55)	
Volume_ZeroX_1_workingval_1_pre_CRAM	C162 (Pg 49, Reg 56, 57, 58, 59)	
Volume_ZeroX_1_volout_pre1	C163 (Pg 49, Reg 60, 61, 62, 63)	
Volume_ZeroX_1_workingval_2_pre_CRAM	C164 (Pg 49, Reg 64, 65, 66, 67)	
Volume_ZeroX_1_volout_pre2	C165 (Pg 49, Reg 68, 69, 70, 71)	
Volume_ZeroX_1_workingval_3_pre_CRAM	C166 (Pg 49, Reg 72, 73, 74, 75)	
Volume_ZeroX_1_volout_pre3	C167 (Pg 49, Reg 76, 77, 78, 79)	
Volume_ZeroX_1_One_M2	C168 (Pg 49, Reg 80, 81, 82, 83)	
Volume_ZeroX_1_Zero	C169 (Pg 49, Reg 84, 85, 86, 87)	
MinusOne_Int	C170 (Pg 49, Reg 88, 89, 90, 91)	
MinusOne_M1	C171 (Pg 49, Reg 92, 93, 94, 95)	
One_M2	C172 (Pg 49, Reg 96, 97, 98, 99)	
One_M1	C173 (Pg 49, Reg 100, 101, 102, 103)	
Zero	C174 (Pg 49, Reg 104, 105, 106, 107)	

8.6.3.8 Miscellaneous Coefficients

Table 28. Miscellaneous Coefficients

Coefficient	Register	Description
DRC_MB_1_DataBlock	C175 (Pg 49, Reg 108, 109, 110, 111)	
DRC_MB_1_CoeffBlock	C176 (Pg 49, Reg 112, 113, 114, 115)	
Volume_ZeroX_1_DataBlock	C177 (Pg 49, Reg 116, 117, 118, 119)	
Volume_ZeroX_1_CoeffBlock	C178 (Pg 49, Reg 120, 121, 122, 123)	
plus_one	C179 (Pg 49, Reg 124, 125, 126, 127)	
ADD_OF_filter_in_L	C180 (Pg 50, Reg 8, 9, 10, 11)	
ADD_OF_filter_in_R	C181 (Pg 50, Reg 12, 13, 14, 15)	

8.7 DAC and Differential Analog Outputs

8.7.1 Analog Outputs

The PCM5242 devices include a two-channel DAC, with differential outputs. Each pin has a full-scale output voltage is $2.1V_{rms}$ with ground center output. This equates to a $4.2V_{rms}$ differential output. A dc-coupled load is supported in addition to an ac-coupled load, if the load resistance conforms to the specification. The PCM5242 DAC outputs on the OUTLP, OUTLN, OUTRP, and OUTRN terminals have market-leading low out-of-band noise, which offer up to 20dB lower out-of-band noise compared with existing DAC technology.

Many applications require an external low-pass RC filter (470Ω + 1.2nF) to provide sufficient out-of-band noise rejection. This RC filter provides the added advantage of improved protection against ESD damage.

The PCM5242 can also support single ended outputs, using OUTLP and OUTRP respectively. A single 470Ω and 2.2nF capacitor can be used on each pin in single ended mode.

The choice between VREF and VCOM modes affects the maximum output level. This is explained in Voltage Reference and Output Levels.

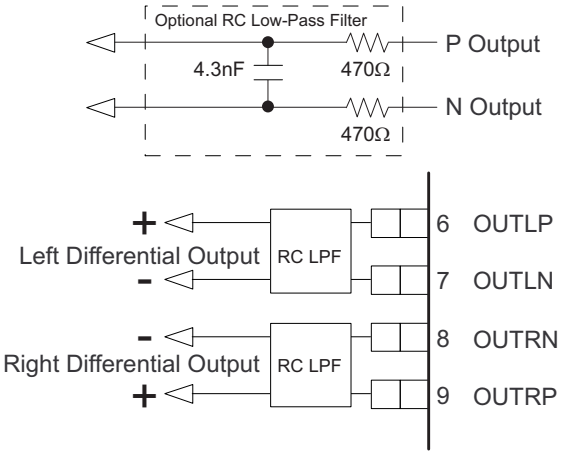


Figure 66. Optional Low Pass Filters

8.7.2 Choosing Between VREF and VCOM Modes

VREF mode is the default configuration. This mode allows full $2.1V_{rms}$ signal output. As shown in Recommended Operating Conditions, the minimum AVDD to avoid clipping is 3.2V.

VCOM mode allows setting a custom common-mode voltage when required by the application. This somewhat limits the output signal swing before clipping.

8.7.2.1 Voltage Reference and Output Levels

The PCM5242 has an internal, fixed band-gap reference voltage, with default operation in VREF mode. No external decoupling capacitor is required for this mode.

The PCM5242 can be operated with a common-mode voltage output (VCOM mode) at the VCOM pin by setting Page 1, Register 1, D(0) to 1. In this mode, an external decoupling capacitor is required.

When using this DAC in VREF mode, the output-signal voltage is independent of the power-supply voltage: The D/A conversion gain in VREF mode yields a $2.1V_{rms}$ output voltage with a digital full-scale input. However, in VREF mode, an output waveform may clip due to the limitations that may be present in the analog power supply voltage. On the other hand, the full-scale output voltage in VCOM mode is proportional to the analog power supply AVDD. Example, (2.1 × AVDD / 3.3) V_{rms}.

8.7.2.2 Mode Switching Sequence, From VREF Mode to VCOM Mode

Following register setting sequence is recommended for changing VREF mode to VCOM mode.

1. Page 0 / Register 2 RQST = 1: Standby mode

DAC and Differential Analog Outputs (continued)

2.	Page 1 / Register 8	RCMF = 1: Fast ramp up → on
3.	Page 1 / Register 9	VCPD = 0: VCOM is power on
4.		Wait 3ms with external capacitor = 1µF
5.	Page 1 / Register 8	RCMF = 0: Fast ramp up → off
6.	Page 1 / Register 1	OSEL = 1: VCOM mode
7.	Page 0 / Register 2	RQST = 0: Normal mode

8.7.3 Digital Volume Control

A basic digital volume control with range from 24 dB to -103 dB and mute is available on each channels by Page 0, Resister 61, D(7:0) for L-ch and Register 62, D(7:0) for R-ch. These volume controls all have 0.5 dB step programmability over most gain and attenuation ranges. Table 29 lists the detailed gain versus programmed setting for this basic volume control. Volume can be changed for both L-ch and R-ch at the same time or independently by Page 0, Register 60, D(1:0). When D(1:0) set 00 (default), independent control is selected. When D(1:0) set 01, R-ch accords with L-ch volume. When D(1:0) set 10, L-ch accords with R-ch volume. To set D(1:0) to 11 is prohibited.

NOTE

This volume control is done externally to the miniDSP and only influences the analog DAC output. Any changes to the SDOUT data should be done in the miniDSP process flow

Table 29. Digital Volume Control Settings

Gain Setting	Binary Data	Gain (dB)	Comments
0	0000-0000	24.0	Positive maximum
1	0000-0001	23.5	
:	:	:	
46	0010-1110	1.0	
47	0010-1111	0.5	
48	0011-0000	0.0	No attenuation (default)
49	0011-0001	- 0.5	
50	0011-0010	- 1.0	
51	0011-0011	- 1.5	
:	:	:	
253	1111-1101	- 102.5	
254	1111-1110	- 103	Negative maximum
255	1111-1111	- ∞	Negative infinite (Mute)

Ramp-up frequency and ramp-down frequency can be controlled by Page 0, Register 63, D(7:6) and D(3:2) as shown in Table 30. Also Ramp-up step and ramp-down step can be controlled by Page 0, Register 63 D(5:4) and D(1:0) as shown in Table 31.

Table 30. Ramp Up or Down Frequency

Ramp up speed	Every N f_S	Comments	Ramp down frequency	Every N f_S	Comments
00	1	Default	00	1	Default
01	2		01	2	
10	4		10	4	
11	Direct change		11	Direct change	

Table 31. Ramp Up or Down Step

Ramp up step	Step dB	Comments	Ramp down step	Step dB	Comments
00	4.0		00	-4.0	
01	2.0		01	-2.0	
10	1.0	Default	10	-1.0	Default
11	0.5		11	-0.5	

8.7.3.1 Emergency Ramp Down

Digital volume emergency ramp down by is provided for situations such as I^2S clock error and power supply failure. Ramp-down speed is controlled by Page 0, Register 64, D(7:6). Ramp-down step can be controlled by Page 0 Register 64, D(5:4). Default is ramp-down by every f_S cycle with -4dB step.

8.7.4 Analog Gain Control

Analog gain control can be selected between $2V_{rms}$ FS (0dB) or $1V_{rms}$ FS (-6dB). Gain is controlled via hardware by the AGNS pin, and via software (SPI/I^2C), Page 1, Register 2, D4(L-ch) / D0(R-ch).

8.8 Reset and System Clock Functions

8.8.1 Clocking Overview

The PCM5242 devices have flexible systems for clocking. Internally, the device requires a number of clocks, mostly at related clock rates to function correctly. All of these clocks can be derived from the Serial Audio Interface in one form or another.

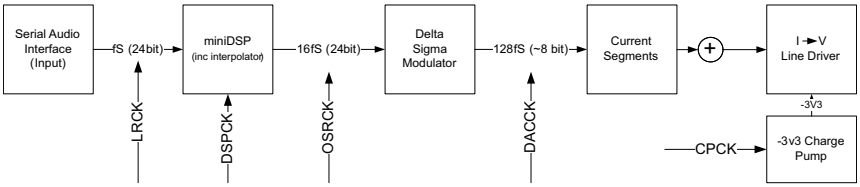


Figure 67. Audio flow with respective clocks

As shown in Figure 67 the basic data flow at basic sample rate (f_S). Once the data is brought into the serial audio interface, it gets processed, interpolated and modulated all the way to 128 × f_S before arriving at the current segments for the final digital to analog conversion.

The clock tree is shown in Figure 68.

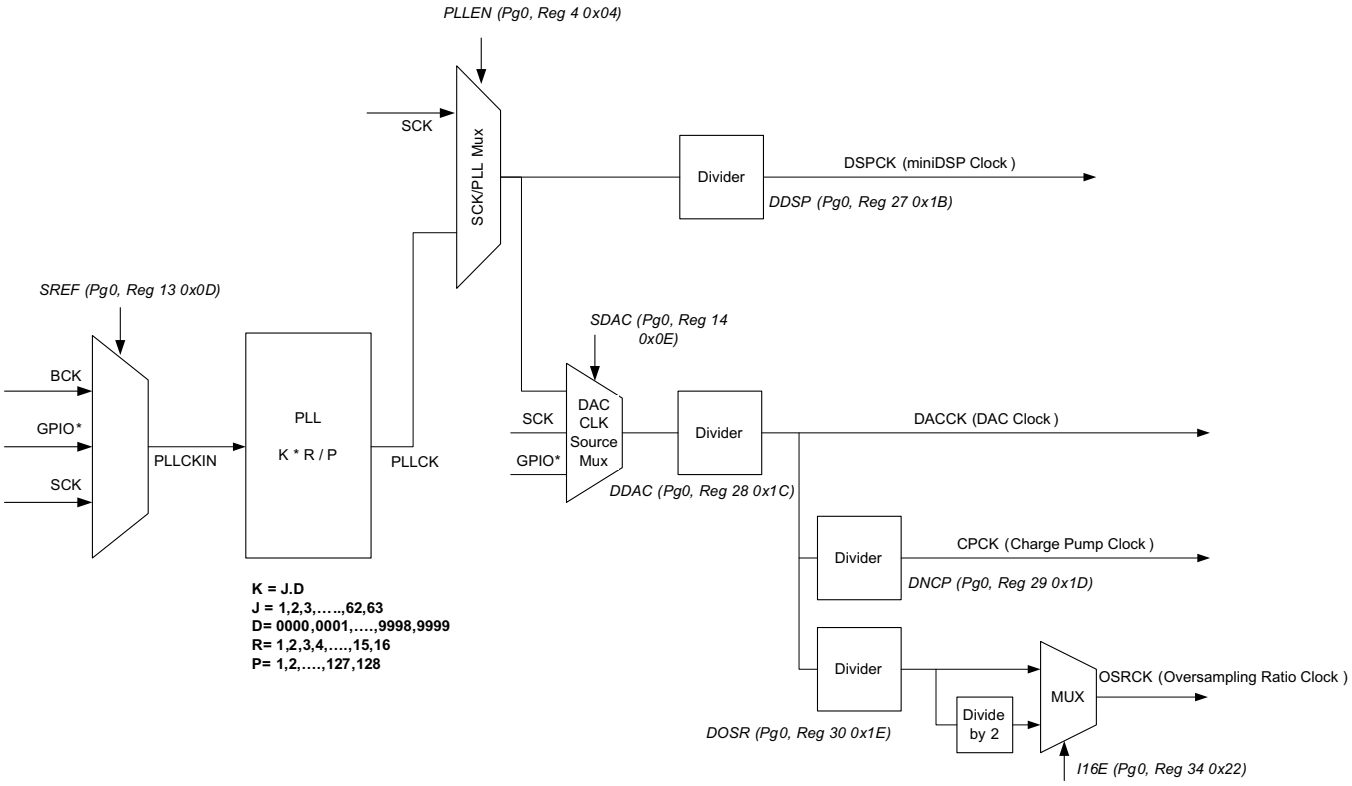


Figure 68. PCM5242 Clock Distribution Tree

The Serial Audio Interface typically has 4 connections SCK (System Master Clock), BCK (Bit Clock), LRCK (Left Right Word Clock) and Data. The device has an internal PLL that is used to take either SCK or BCK and create the higher rate clocks required by the miniDSP and the DAC clock.

In situations where the highest audio performance is required, it's suggested that the SCK is brought to the device, along with BCK and LRCK. The device should be configured so that the PLL is only providing a clock source to the miniDSP. By ensuring that the DACCK (DAC Clock) is being driven by the external SCK source, jitter evident in the PLL (in all PLL's) is kept out of the DAC, Charge Pump and Oversampling system.

Reset and System Clock Functions (continued)

Everything else should be a division of the incoming SCK. This is done by setting DAC CLK Source Mux (SDAC in the diagram above) to use SCK as a source, rather than the output of the SCK/PLL Mux. Code Examples for this are available in SLAC622

When the Auto Clock Configuration bit is set (Page0/ Register 0x25), no additional clocks configuration is required. However, when setting custom PLL values etc, the target output rates should match those shown in the recommended PLL values of Table 50.

8.8.2 Clock Slave Mode With Master Clock (SCK) Input (4 Wire I²S)

The PCM5242 requires a system clock to operate the digital interpolation filters and advanced segment DAC modulators. The system clock is applied at the SCK input and supports up to 50MHz. The PCM5242 system-clock detection circuit automatically senses the system-clock frequency. Common audio sampling frequencies in the bands of 8kHz, 16kHz, (32kHz - 44.1kHz - 48kHz), (88.2kHz - 96kHz), (176.4kHz -192kHz), and 384kHz with ±4% tolerance are supported. **Values in the parenthises are "grouped" when detected, e.g. 88.2kHZ and 96kHz are detected as "double rate", 32kHz, 44.1kHz and 48kHz will be detected as "single rate".**

In the presence of a valid bit SCK, BCK and LRCK in software mode, the device will autoconfigure the clock tree and PLL to drive the miniDSP as required.

The sampling frequency detector sets the clock for the digital filter, Delta Sigma Modulator (DSM) and the Negative Charge Pump (NCP) automatically. Table 32 shows examples of system clock frequencies for common audio sampling rates.

SCK rates that are not common to standard audio clocks, between 1MHz and 50MHz, are only supported in software mode by configuring various PLL and clock-divider registers. This programmability allows the device to become a clock master and drive the host serial port with LRCK and BCK, from a non-audio related clock (for example, using 12MHz to generate 44.1kHz (LRCK) and 2.8224MHz (BCK)).

Table 32. System Master Clock Inputs for Audio Related Clocks

Sampling Frequency	System Clock Frequency (f_{SCK}) (MHz)											
	64 f_S	128 f_S	192 f_S	256 f_S	384 f_S	512 f_S	768 f_S	1024 f_S	1152 f_S	1536 f_S	2048 f_S	3072 f_S
8 kHz	–(1)	1.0240(2)	1.5360(2)	2.0480	3.0720	4.0960	6.1440	8.1920	9.2160	12.2880	16.3840	24.5760
16 kHz	–(1)	2.0480(2)	3.0720(2)	4.0960	6.1440	8.1920	12.2880	16.3840	18.4320	24.5760	36.8640	49.1520
32 kHz	–(1)	4.0960(2)	6.1440(2)	8.1920	12.2880	16.3840	24.5760	32.7680	36.8640	49.1520	–(1)	–(1)
44.1 kHz	–(1)	5.6488(2)	8.4672(2)	11.2896	16.9344	22.5792	33.8688	45.1584	–(1)	–(1)	–(1)	–(1)
48 kHz	–(1)	6.1440(2)	9.2160(2)	12.2880	18.4320	24.5760	36.8640	49.1520	–(1)	–(1)	–(1)	–(1)
88.2 kHz	–(1)	11.2896(2)	16.9344	22.5792	33.8688	45.1584	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)
96 kHz	–(1)	12.2880(2)	18.4320	24.5760	36.8640	49.1520	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)
176.4 kHz	–(1)	22.5792	33.8688	45.1584	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)
192 kHz	–(1)	24.5760	36.8640	49.1520	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)
384 kHz	24.5760	49.1520	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)

(1) This system clock rate is not supported for the given sampling frequency.
(2) This system clock rate is supported by PLL mode.

See Timing Requirements: PCM Audio Data for clock timing requirements.

8.8.3 Clock Slave Mode with BCK PLL to Generate Internal Clocks (3-Wire PCM)

The system clock PLL mode allows designers to use a simple 3-wire I²S audio source. The 3-wire source reduces the need for a high frequency SCK, making PCB layout easier, and reduces high frequency electromagnetic interference.

In hardwired mode, the internal PLL is disabled as soon as an external SCK is supplied.

In hardwired mode, the device starts up expecting an external SCK input, but if BCK and LRCK start correctly while SCK remains at ground level for 16 successive LRCK periods, then the internal PLL starts, automatically generating an internal SCK from the BCK reference. Specific BCK rates are required to generate an appropriate master clock. Table 33 describes the minimum and maximum BCK per LRCK for the integrated PLL to automatically generate an internal SCK.

In software mode, the user must set all the PLL registers and clock divider registers for referencing BCK. See Clock Generation Using The PLL for more information. Recommended values can be found in Table 50.

Table 33. BCK Rates (MHz) by LRCK Sample Rate for PCM5242 PLL Operation

Sample f (kHz)	BCK (f_S)	
	32	64
8	-	-
16	-	1.024
32	1.024	2.048
44.1	1.4112	2.8224
48	1.536	3.072
96	3.072	6.144
192	6.144	12.288
384	12.288	24.576

8.8.4 Clock Generation Using The PLL

The PCM5242 supports a wide range of options to generate the required clocks for the DAC section as well as interface and other control blocks as shown in Figure 68.

The clocks for the PLL require a source reference clock. This clock is sourced as the incoming BCK or SCK. In software mode, a GPIO can also be used.

The source reference clock for the PLL reference clock is selected by programming the SRCREF value on Page 0, Register 13, D(6:4). The PCM5242 provides several programmable clock dividers to achieve a variety of sampling rates for the DAC and clocks for the NCP, OSR, and the miniDSP. OSRCK for OSR must be set at $16f_S$ frequency by DOSR on Page0, Register 30, D(6:0). See Figure 68.

If PLL functionality is not required, set the PLLEN value on Page 0, Register 4, D(0) to 0. In this situation, an external SCK is required.

Table 34. PLL Configuration Registers

Clock multiplexer	Function	Bits
SREF	PLL Reference	Page 0, Register 13, D(6:4)
Divider	**Function**	**Bits**
DDSP	miniDSP clock divider	Page 0, Register 27, D(6:0)
DACCK	DAC clock divider	Page 0, Register 28, D(6:0)
CPCK	NCP clock divider	Page 0, Register 29, D(6:0)
OSRCK	OSR clock divider	Page 0, Register 30, D(6:0)
DBCK	External BCK Div	Page 0, Register 32, D(6:0)
DLRK	External LRCK Div	Page 0, Register 33, D(7:0)

8.8.5 PLL Calculation

The PCM5242 has an on-chip PLL with fractional multiplication to generate the clock frequency needed by the audio DAC, Negative Charge Pump, Modulator and Digital Signal Processing blocks. The programmability of the PLL allows operation from a wide variety of clocks that may be available in the system. The PLL input (PLLCKIN) supports clock frequencies from 1MHz to 50MHz and is register programmable to enable generation of required sampling rates with fine precision.

The PLL is enabled by default. The PLL can be turned on by writing to Page 0, Register 4, D(0). When the PLL is enabled, the PLL output clock PLLCK is given by Equation 3:

$$PLLCK = \frac{PLLCKIN \times R \times J.D}{P} \quad \text{or} \quad PLLCK = \frac{PLLCKIN \times R \times K}{P} \tag{3}$$

R = 1, 2, 3,4, ... , 15, 16

J = 4,5,6, . . . 63, and D = 0000, 0001, 0002, . . . 9999

K = [J value].[D value]

P = 1, 2, 3, ... 15

R, J, D, and P are programmable. J is the integer portion of K (the numbers to the left of the decimal point), while D is the fractional portion of K (the numbers to the right of the decimal point, assuming four digits of precision).

8.8.5.1 Examples:

- If K = 8.5, then J = 8, D = 5000
- If K = 7.12, then J = 7, D = 1200
- If K = 14.03, then J = 14, D = 0300
- If K = 6.0004, then J = 6, D = 0004

When the PLL is enabled and D = 0000, **the following conditions must be satisfied:**

- 1MHz ≤ (PLLCKIN / P) ≤ 20MHz
- 64MHz ≤ (PLLCKIN x K x R / P) ≤ 100MHz (in VREF mode)
- 72MHz ≤ (PLLCKIN x K x R / P) ≤ 86MHz (in VCOM mode)
- 1 ≤ J ≤ 63

When the PLL is enabled and D ≠ 0000, **the following conditions must be satisfied:**

- 6.667MHz ≤ PLLCLKIN / P ≤ 20MHz
- 64MHz ≤ (PLLCKIN x K x R / P) ≤ 100MHz (in VREF mode)
- 72MHz ≤ (PLLCK IN x K x R / P) ≤ 86MHz (in VCOM mode)
- 4 ≤ J ≤ 11
- R = 1

When the PLL is enabled,

- f_S = (PLLCLKIN × K × R) / (2048 × P)
- The value of N is selected so that f_S × N = PLLCLKIN x K x R / P is in the allowable range.

Example: MCLK = 12MHz and f_S = 44.1kHz, (N=2048)

Select P = 1, R = 1, K = 7.5264, which results in J = 7, D = 5264

Example: MCLK = 12MHz and f_S = 48.0kHz, (N=2048)

Select P = 1, R = 1, K = 8.192, which results in J = 8, D = 1920

Values are written to the registers in Table 35.

8.8.5.1.1 Recommended PLL settings

Recommended values for the PLL can be found after the register descriptions in this datasheet. Different values are defined based on the device configuration for VREF or VCOM mode.

Other configurations are possible, at your own risk.

Below are details of the register locations, as well as the nomenclature for the table of registers found at the end of this document.

Table 35. PLL Registers

Divider	Function	Bits
PLLE	PLL enable	Page 0, Register 4, D(0)
PPDV	PLL P	Page 0, Register 20, D(3:0)
PJDV	PLL J	Page 0, Register 21, D(5:0)
PDDV	PLL D	Page 0, Register 22, D(5:0)
		Page 0, Register 23, D(7:0)
PRDV	PLL R	Page 0, Register 24, D(3:0)

Table 36. PLL Configuration Recommendations

Column	Description
f_S (kHz)	Sampling frequency
RSCK	Ratio between sampling frequency and SCK frequency (SCK frequency = RSCK x sampling frequency)
SCK (MHz)	System master clock frequency at SCK input (pin 20)
PLL VCO (MHz)	PLL VCO frequency as PLLCK in Figure 68
P	One of the PLL coefficients in Equation 3
PLL REF (MHz)	Internal reference clock frequency which is produced by SCK / P
M = K * R	The final PLL multiplication factor computed from K and R as described in Equation 3
K = J.D	One of the PLL coefficients in Equation 3
R	One of the PLL coefficients in Equation 3
PLL f_S	Ratio between f_S and PLL VCO frequency (PLL VCO / f_S)
DSP f_S	Ratio between miniDSP operating clock rate and f_S (PLL f_S / NMAC)
NMAC	The miniDSP clock divider value in Table 34
DSP CLK (MHz)	The miniDSP operating frequency as DSPCK in Figure 68
MOD f_S	Ratio between DAC operating clock frequency and f_S (PLL f_S / NDAC)
MOD f (kHz)	DAC operating frequency as DACCK in
NDAC	DAC clock divider value in Table 34
DOSR	OSR clock divider value in Table 34 for generating OSRCK in Figure 68. DOSR must be chosen so that MOD f_S / DOSR = 16 for correct operation.
NCP	NCP (negative charge pump) clock divider value in Table 34
CP f	Negative charge pump clock frequency (f_S * MOD f_S / NCP)
% Error	Percentage of error between PLL VCO / PLL f_S and f_S (mismatch error). • This number is typically zero but can be non-zero especially when K is not an integer (D is not zero). • This number may be non-zero only when the PCM5242 acts as a master.

8.8.6 Clock Master Mode from Audio Rate Master Clock

In Master Mode, the device generates bit clock (BCK) and left-right clock (LRCK) and outputs them on the appropriate pins. To configure the device in this mode, first put the device into reset, then use registers BCKO and LRKO (Pg 0, Reg 9 0x09). Then reset the LRCK and BCK divider counters using bits RBCK and RLRK (Pg 0, Reg 12 0x0C). Finally exit reset.

An example of this is given in *Register Programming Examples* SLAC622.

Figure 69 shows a simplified serial port clock tree for the device in master mode.

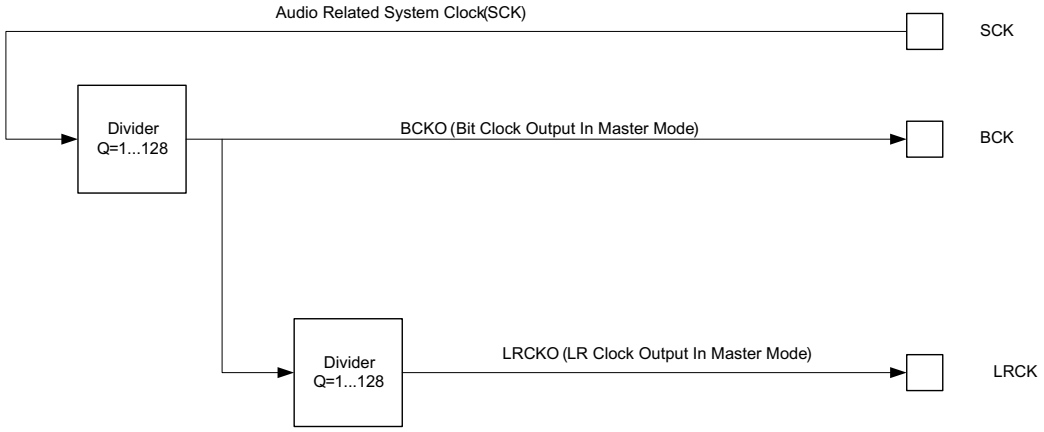


Figure 69. Simplified clock tree for SCK sourced master mode

In master mode, SCK is an input and BCK/LRCK are outputs. BCK and LRCK are integer divisions of SCK. Master mode with a non-audio rate master clock source will require external GPIO's to use the PLL in standalone mode.

The PLL will also need to be configured to ensure that the onchip miniDSP processor can be driven at its maximum clock rate.

Register changes that need to be done include switching the device into master mode, and setting the divider ratio.

Here is an example of using 24.576MCLK as a master clock source and driving the BCK and LRCK with integer dividers to create 48kHz.

In this mode, the DAC section of the device is also running from the PLL output. While the PLL inside the PCM5242 is one that has been spec'd well enough to achieve the stated performance, using the SCK CMOS Oscillator source will have less jitter.

To switch the DAC clocks (SDAC in the Figure 68) the following registers should be modified

- Clock Tree Flex Mode (Page 253, Registers 0x3F and 0x40)
- DAC & OSR Source Clock Register (Page 0, Reg 14) – set to 0x30 (SCK input, and OSR is set to whatever the DAC source is)
- The DAC clock divider should be 16FS.
  - 16*48kHz = 768kHz
  - 24.576MHz (SCK in) / 768kHz = 32
  - Therefor, divide ratio for register DDAC (Page 0, Reg 28 0x1C) should be set to 32. The may the register is mapped gives 0x00 = 1, so 32 must be converter to 0x1F (31dec).

An example configuration can be found in SLAC622

8.8.7 Clock Master from a Non-Audio Rate Master Clock

The classic example here is running 12MHz Master clock for a 48kHz sampling system. Given the clock tree for the device (shown in Figure 68), a non-audio clock rate cannot be brought into the SCK to the PLL in master mode. Therefore, the PLL source must be configured to be a GPIO pin, and the output brought back into another GPIO pin.

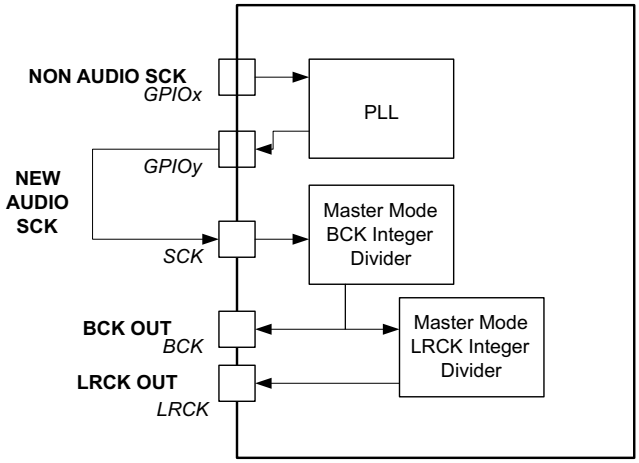


Figure 70. Application diagram for using non-audio clock sources to generate audio clocks

The clock flow through the system is shown above. The newly generated SCK must be brought out of the device on a GPIO pin, then brought into the SCK pin for integer division to create BCK and LRCK outputs.

NOTE

Pull up resistors should be used on BCK and LRCK in this mode to ensure the device doesn't go into sleep mode.

A code example for configuring this mode is provided in SLAC622

8.9 Device Functional Modes

8.9.1 Choosing A Control Mode

SPI Mode is selected by connecting MODE1 to DVDD. SPI mode uses four signal lines and allows higher-speed full-duplex communication between the host and the PCM5242.

I^2C Mode is selected by connecting MODE1 to DGND and Mode2 to DVDD. I^2C uses two signal lines for half-duplex communication, and is widely used in a variety of devices.

Hardware Control Mode is selected by connecting both MODE1 and MODE2 pins to DGND. Hardware control is useful in applications that do not require on-the-fly device-reconfiguration changes in operating features such as gain or filter latency selection.

See Pin Assignments for a comparison of pin assignments for the 32-terminal QFN.

8.9.1.1 Software Control

8.9.1.1.1 SPI Interface

The SPI interface is a 4-wire synchronous serial port which operates asynchronously to the serial audio interface and the system clock (SCK). The serial control interface is used to program and read the on-chip mode registers.

The control interface includes MISO (pin 24), MOSI (pin 11), MC (pin 12), and MS (pin 18). MISO (Master In Slave Out) is the serial data output, used to read back the values of the mode registers; MOSI (Master Out Slave In) is the serial data input, used to program the mode registers.

MC is the serial bit clock, used to shift data in and out of the control port by falling edge of MC, and MS is the mode control enable with LOW active, used to enable the internal mode register access. If feedback from the device is not required, the MISO pin can be assigned to GPIO1 by register control.

8.9.1.1.1.1 Register Read/Write Operation

All read/write operations for the serial control port use 16-bit data words. Figure 71 shows the control data word format. The most significant bit is the read/write bit. For write operations, the bit must be set to 0. For read operations, the bit must be set to 1. There are seven bits, labeled IDX[6:0], that hold the register index (or address) for the read and write operations. The least significant eight bits, D[7:0], contain the data to be written to, or the data that was read from, the register specified by IDX[6:0].

Figure 71 and Figure 72 show the functional timing diagram to write or read through the serial control port. MS is held at a logic-1 state until a register access. To start the register write or read cycle, set MS to logic 0. Sixteen clocks are then provided on MC, corresponding to the 16 bits of the control data word on MOSI and read-back data on MISO. After the eighth clock cycle has completed, the data from the indexed-mode control register appears on MISO during the read operation. After the sixteenth clock cycle has completed, the data is latched into the indexed-mode control register during the write operation. To write or read subsequent data, MS is set to logic 1 once (See t_{MHH} in Figure 76).

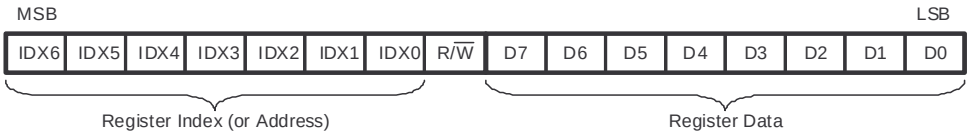


Figure 71. Control Data Word Format; MDI

NOTE

B8 is used for selection of “Write” or “Read”. Setting = 0 indicates a “Write”, while = 1 indicates a ”Read”. Bits 15–9 are used for register address. Bits 7–0 are used for register data. Multiple-byte write or read (up to 8 bytes) is supported while MS is kept low. The address field becomes the initial address, automatically incrementing for each byte.

Device Functional Modes (continued)

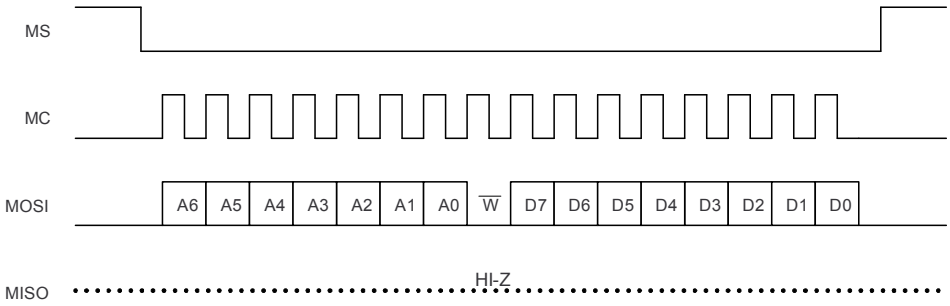


Figure 72. Serial Control Format; Write, Single Byte

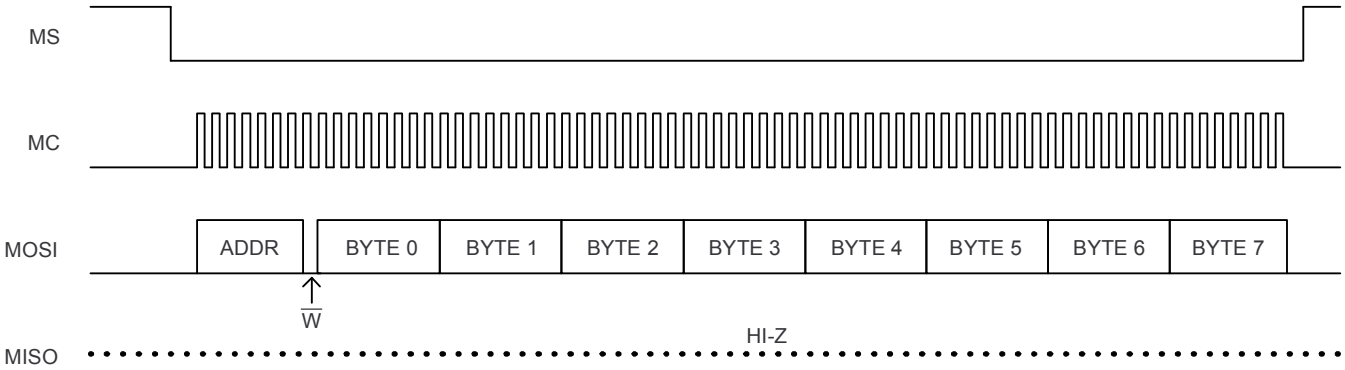


Figure 73. Serial Control Format; Write, Multiple Byte

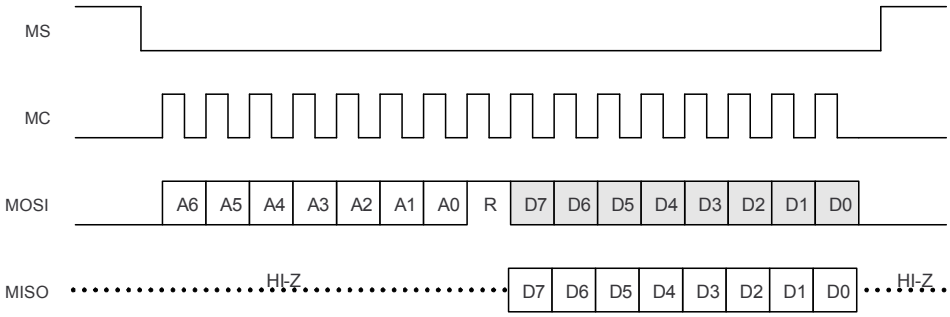


Figure 74. Serial Control Format; Read

Device Functional Modes (continued)

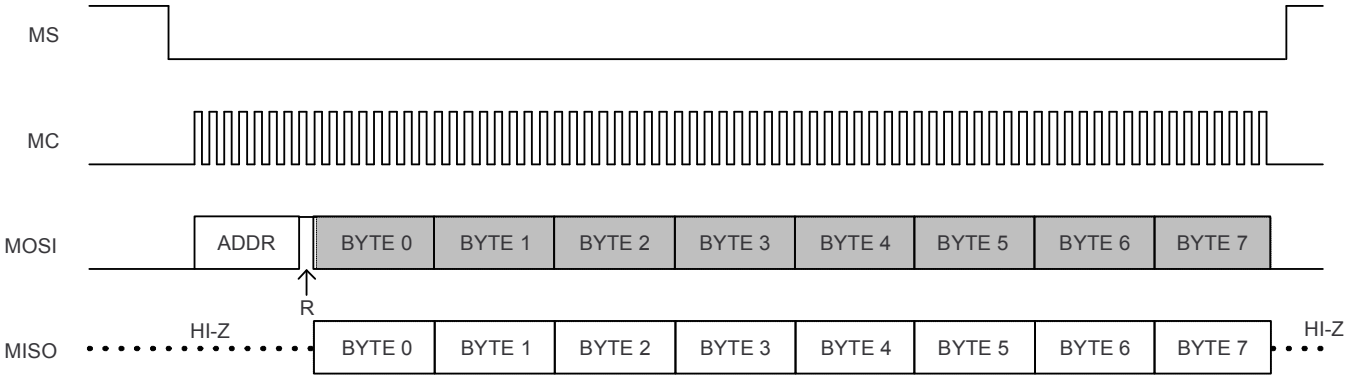


Figure 75. Serial Control Format; Read, Multiple Byte

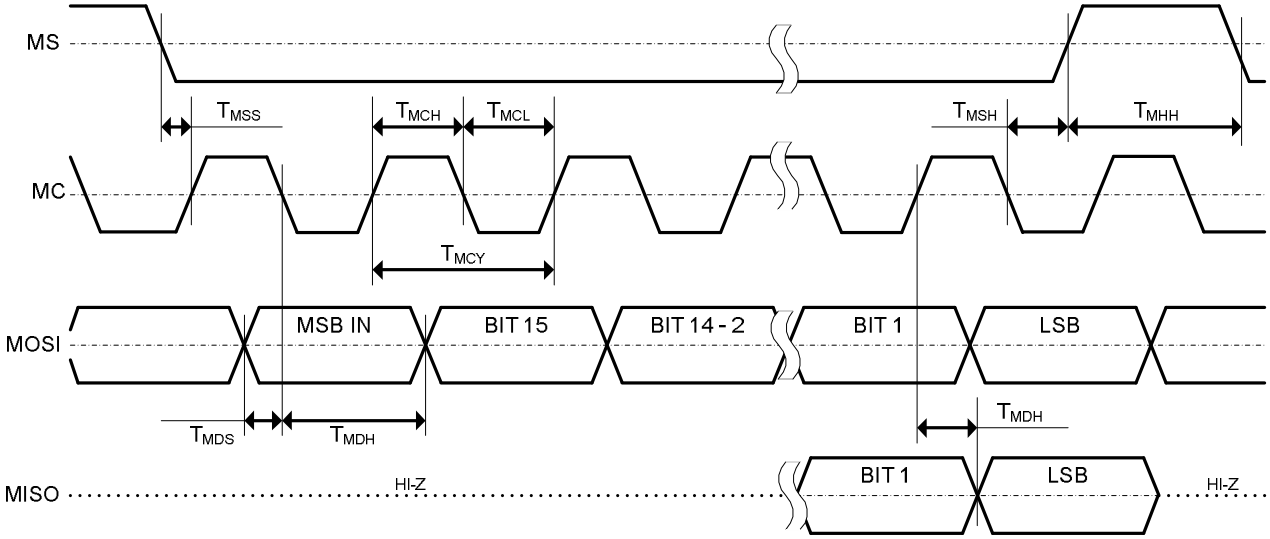


Figure 76. Control Interface Timing

Table 37. Control Interface Timing

	Parameters	Min	Max	Units
t_{MCY}	MC Pulse Cycle Time	100		ns
t_{MCL}	MC Low Level Time	40		
t_{MCH}	MC High Level Time	40		
t_{MHH}	$\overline{MS}$ High Level Time	20		
t_{MSS}	$\overline{MS}$ ↓ Edge to MC ↑ Edge	30		
t_{MSH}	$\overline{MS}$ Hold Time (1)	30		
t_{MDH}	MDI Hold Time	15		
t_{MDS}	MDI Set-up Time	15		
t_{MOS}	MC Rise Edge to MDO Stable		20	

(1) MC falling edge for LSB to MS rising edge.

8.9.1.1.2 I²C Interface

The PCM5242 supports the I²C serial bus and the data transmission protocol for standard and fast mode as a slave device.

In I²C mode, the control terminals are changed as follows.

Table 38. I²C Pins and Functions

Signal	Pin	I/O	Description
SDA	11	I/O	I²C data
SCL	12	I	I²C clock
ADR2	16	I	I²C address 2
ADR1	24	I	I²C address 1

8.9.1.1.2.1 Slave Address

Table 39. I²C Slave Address

MSB							LSB
1	0	0	1	1	ADR2	ADR1	R/ $\overline{W}$

The PCM5242 has 7 bits for its own slave address. The first five bits (MSBs) of the slave address are factory preset to 10011 (0x9x). The next two bits of the address byte are the device select bits which can be user-defined by the ADR1 and ADR0 terminals. A maximum of four devices can be connected on the same bus at one time. This gives a range of 0x98, 0x9A, 0x9C and 0x9E. Each PCM5242 responds when it receives its own slave address.

8.9.1.1.2.2 Register Address Auto-Increment Mode

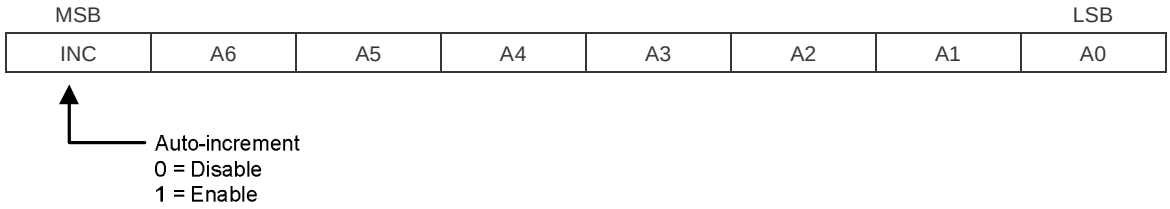


Figure 77. Auto Increment Mode

Auto-increment mode allows multiple sequential register locations to be written to or read back in a single operation, and is especially useful for block write and read operations.

8.9.1.1.2.3 Packet Protocol

A master device must control packet protocol, which consists of start condition, slave address, read/write bit, data if write or acknowledge if read, and stop condition. The PCM5242 supports only slave receivers and slave transmitters.

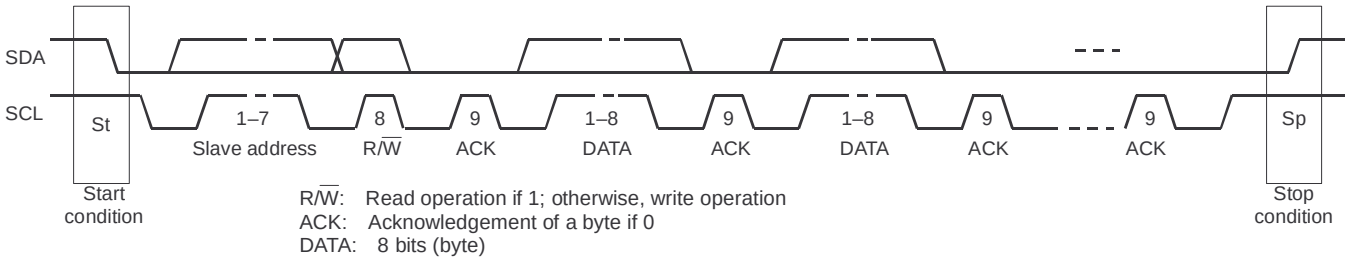


Figure 78. Packet Protocol

Table 40. Write Operation - Basic I²C Framework

Transmitter	*M*	*M*	*M*	*S*	*M*	*S*	*M*	*S*		*S*	*M*
Data Type	St	slave address	R/	ACK	DATA	ACK	DATA	ACK		ACK	Sp

Table 41. Read Operation - Basic I²C Framework

Transmitter	*M*	*M*	*M*	*S*	*S*	*M*	*S*	*M*		*M*	*M*
Data Type	St	slave address	R/	ACK	DATA	ACK	DATA	ACK		NACK	Sp

M = Master Device; S = Slave Device; St = Start Condition Sp = Stop Condition

8.9.1.1.2.4 Write Register

A master can write to any PCM5242 registers using single or multiple accesses. The master sends a PCM5242 slave address with a write bit, a register address with auto-increment bit, and the data. If auto-increment is enabled, the address is that of the starting register, followed by the data to be transferred. When the data is received properly, the index register is incremented by 1 automatically. When the index register reaches 0x7F, the next value is 0x0. Table 42 shows the write operation.

Table 42. Write Operation

Transmitter	*M*	*M*	*M*	*S*	*M*		*S*	*M*	*S*	*M*	*S*		*S*	*M*
Data Type	St	slave addr	W	ACK	inc	reg addr	ACK	write data 1	ACK	write data 2	ACK		ACK	Sp

M = Master Device; S = Slave Device; St = Start Condition Sp = Stop Condition; W = Write; ACK = Acknowledge

8.9.1.1.2.5 Read Register

A master can read the PCM5242 register. The value of the register address is stored in an indirect index register in advance. The master sends a PCM5242 slave address with a read bit after storing the register address. Then the PCM5242 transfers the data which the index register points to. When auto-increment is enabled, the index register is incremented by 1 automatically. When the index register reaches 0x7F, the next value is 0x0. Table 43 shows the read operation.

Table 43. Read Operation

Transmitter	*M*	*M*	*M*	*S*	*M*		*S*	*M*	*M*	*M*	*S*	*S*	*M*		*M*	*M*
Data Type	St	slave addr	W	ACK	inc	reg addr	ACK	Sr	slave addr	R	ACK	data	ACK		NACK	Sp

M = Master Device; S = Slave Device; St = Start Condition; Sr = Repeated start condition; Sp = Stop Condition; W = Write; R = Read; NACK = Not acknowledge

8.9.1.1.2.6 Timing Characteristics

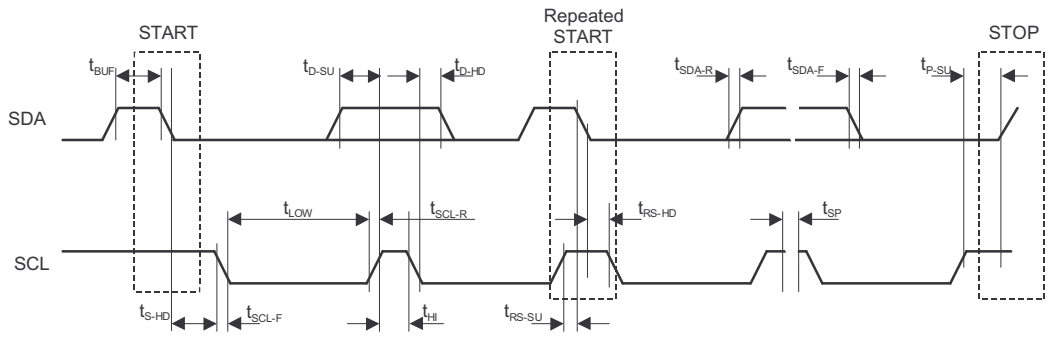


Figure 79. Register Access Timing

Table 44. I²C Bus Timing

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
f_{SCL}	SCL clock frequency	Standard		100	kHz
		Fast		400	kHz
t_{BUF}	Bus free time between a STOP and START condition	Standard	4.7		µs
		Fast	1.3		
t_{LOW}	Low period of the SCL clock	Standard	4.7		µs
		Fast	1.3		
t_{HI}	High period of the SCL clock	Standard	4.0		µs
		Fast	600		ns
t_{RS-SU}	Setup time for (repeated)START condition	Standard	4.7		µs
		Fast	600		ns
t_{S-HD}	Hold time for (repeated)START condition	Standard	4.0		µs
t_{RS-HD}		Fast	600		ns
t_{D-SU}	Data setup time	Standard	250		ns
		Fast	100		
t_{D-HD}	Data hold time	Standard	0	900	ns
		Fast	0	900	
t_{SCL-R}	Rise time of SCL signal	Standard	$20 + 0.1C_B$	1000	ns
		Fast	$20 + 0.1C_B$	300	
t_{SCL-R1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	Standard	$20 + 0.1C_B$	1000	ns
		Fast	$20 + 0.1C_B$	300	
t_{SCL-F}	Fall time of SCL signal	Standard	$20 + 0.1C_B$	1000	ns
		Fast	$20 + 0.1C_B$	300	
t_{SDA-R}	Rise time of SDA signal	Standard	$20 + 0.1C_B$	1000	ns
		Fast	$20 + 0.1C_B$	300	
t_{SDA-F}	Fall time of SDA signal	Standard	$20 + 0.1C_B$	1000	ns
		Fast	$20 + 0.1C_B$	300	
t_{P-SU}	Setup time for STOP condition	Standard	4.0		µs
		Fast	600		ns
C_B	Capacitive load for SDA and SCL line			400	pF
t_{SP}	Pulse width of spike suppressed	Fast		50	ns
V_{NH}	Noise margin at High level for each connected device (including hysteresis)		$0.2V_{DD}$		V

8.9.2 Choosing Between VREF and VCOM Modes

See Choosing Between VREF and VCOM Modes for information on configuring these modes.

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.2 Typical Application

Differential outputs DAC's are regularly used where higher performance is required from them compared to single ended output DACs. They offer twice as much output voltage for the same power supply, along with noise cancelling effect of differential signaling. The PCM5242 makes an ideal front end for both analog input speaker amplifiers and headphone amplifiers with its higher voltage differential output and low noise floor.

9.2.1 High Fidelity Smartphone Application

A new trend in portable applications are termed "Hifi Smartphones". In these systems, a standard portable audio codec continues to be used for telephony, while a separate, higher performance DAC and Headphone Amplifier is used for music playback.

Figure 80 shows a complete circuit schematic for such a system. The digital audio is fed into a high performance DAC. The PCM5242 is a 32-bit, stereo DAC.

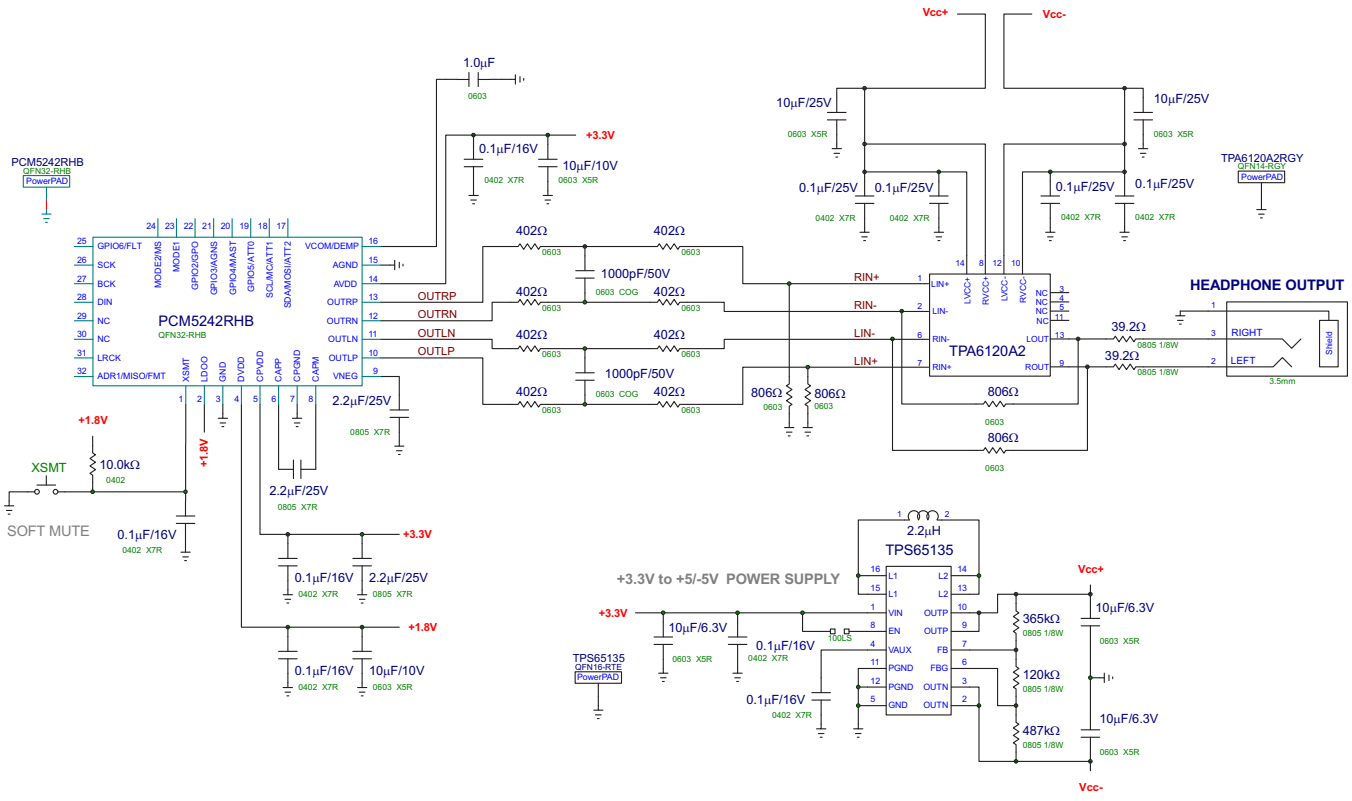


Figure 80. High Fidelity Smartphone Application

Typical Application (continued)

9.2.1.1 Design Requirements

- Directpath output to headphone amplifier
- 1VRMS output, as 2VRMS may cause hearing damage into low impedance headphones
- Stereo differential inputs (DAC is differential)
- Be transparent to the user. (DAC SNR and THD+N performance all the way to the headphone)
- Automatic f_S switching up to 384kHz
- 3-wire I^2S source

9.2.1.2 Detailed Design Procedure

For optimal performance, the TPA6120A2 is configured for use with differential inputs, stereo use, and a gain of 1V/V.

The TPA6120A2 requires a bipolar power supply to drive a ground centered output. The application employs a TPS65135 DC-DC converter that generates ±5V from a single 3.3V supply.

The PCM5242 DAC is configured for a 1VRMS output so that clipping is avoided should the 3.3V power supply sag. The PCM5242 offers a ground centered output, so that no DC blocking capacitors are required between it and the TPA6120A2. (Page 1, Register 2)

9.2.1.2.1 Initialization Script

w 98 00 01 # PCM5242 to Page 1

w 98 02 11 # PCM5242 output to 1 Vrms

w 98 00 00 # PCM5242 back to page 0

w 98 3B 66 # set auto mute time to six seconds of audio zero.

w 98 3C 01 # Left Vol register controls both

w 98 3D 4F # Change left channel volume, right will follow.

w 98 3F BB # set vol changes for every 4 samples, 0.5 sample steps.

9.2.1.3 Application Performance Plot

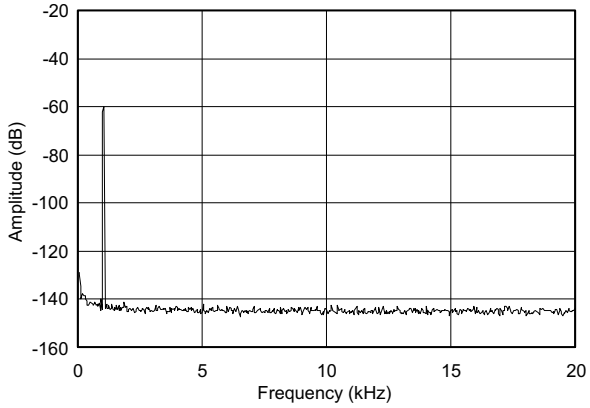


Figure 81. 2 FFT Plot At -60db Input

In this particular application, the TPA6120A2's performance is transparent and the performance of the system is dictated by the PCM5242 DAC, even into a 32-Ω headphone load.

10 Power Supply Recommendations

10.1 Power Supply Distribution and Requirements

The PCM5242 is powered through the following pins:

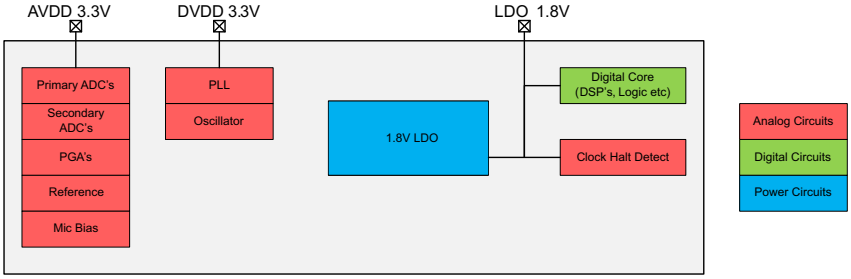


Figure 82. Power Distribution Tree within PCM5242

Table 45. Power Supply Pin Descriptions

NAME	USAGE / DESCRIPTION
AVDD	Analog Voltage Supply - should be 3.3V. Powers the ADC, PGA, Reference, and Secondary ADC
DVDD	Digital Voltage Supply - This is used as the I/O voltage control and the input to the onchip LDO.
CPVDD	Charge Pump Voltage Supply - should be 3.3V
LDOO	Output from the Onchip LDO. Should be used with a 0.1uF decoupling cap. Can be driven (used as power input) with a 1.8V supply to bypass the onchip LDO for lower power consumption.
AGND	Analog Ground
DGND	Digital Ground

10.2 Recommended Powerdown Sequence

Under certain conditions, the PCM5242 can exhibit some pop on power down. Pops are caused by the device not having enough time to detect power loss and start the muting process.

The PCM5242 has two auto-mute functions to mute the device upon power loss (intentional or unintentional).

XSMT = 0

When the XSMT pin is pulled low, the incoming PCM data is attenuated to 0, closely followed by a hard analog mute. This process takes 150 sample times (t_s) + 0.2mS.

Because this mute time is mainly dominated by the sampling frequency, systems sampling at 192kHz will mute much faster than a 48kHz system.

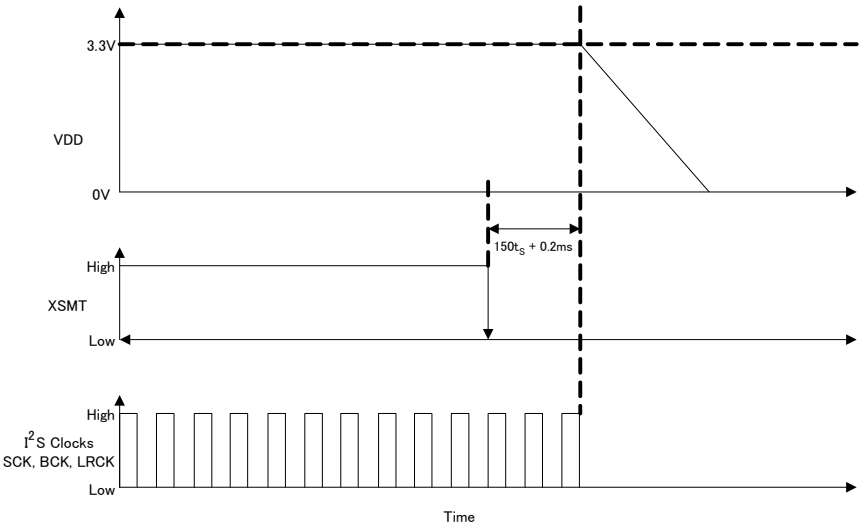
Clock Error Detect

When clock error is detected on the incoming data clock, the PCM5242 switches to an internal oscillator, and continues to the drive the output, while attenuating the data from the last known value. Once this process is complete, the PCM5242 outputs are hard muted to ground.

10.2.1 Planned Shutdown

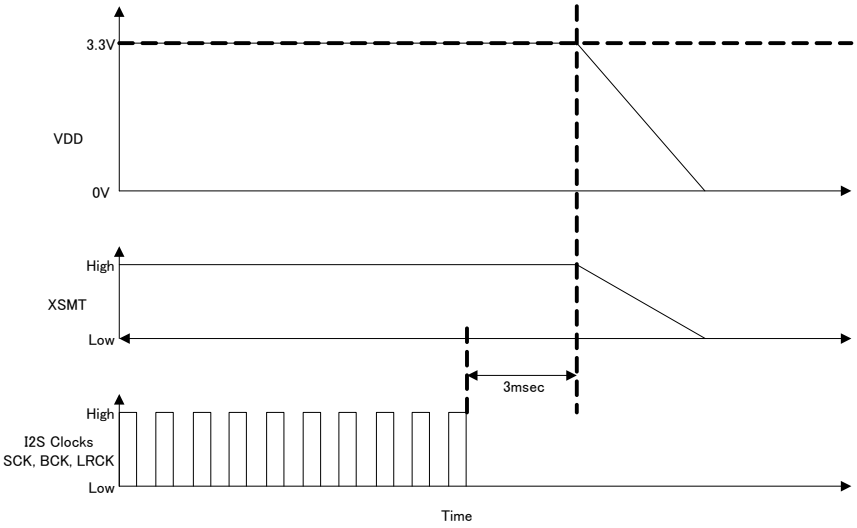
These auto-muting processes can be manipulated by system designs to mute before power loss in the following ways:

1. Assert XSMT low $150t_S$ + 0.2mS before power is removed.



Recommended Powerdown Sequence (continued)

2. Stop I^2S clocks (SCK, BCK, LRCK) 3ms before powerdown as shown below:



10.2.2 Unplanned Shutdown

Many systems use a low-noise regulator to provide an AVDD 3.3V supply for the DAC. The XSMT Pin can take advantage of such a feature to measure the pre-regulated output from the system SMPS to mute the output before the entire SMPS discharges. Figure 83 shows how to configure such a system to use the XSMT pin. The XSMT pin can also be used in parallel with a GPIO pin from the system microcontroller/DSP or Power Supply.

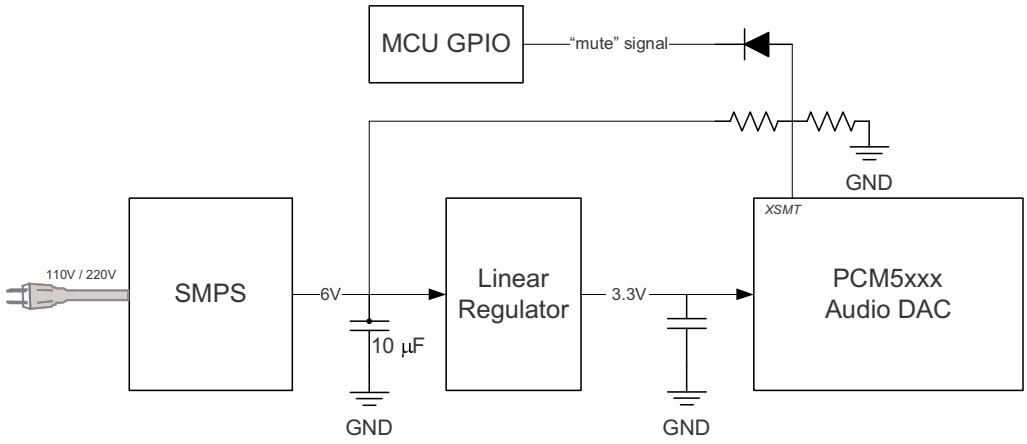


Figure 83. Using the XSMT Pin

10.3 External Power Sense Undervoltage Protection mode (supported only when DVDD = 3.3V)

The XSMT pin can also be used to monitor a system voltage, such as the 24VDC LCD TV backlight, or 12VDC system supply using a voltage divider created with two resistors. (See Figure 84)

- If the XSMT pin makes a transition from “1” to “0” over 6ms or more, the device switches into external under-voltage protection mode. This mode uses two trigger levels.
- When the XSMT pin level reaches 2V, soft mute process begins.
- When the XSMT pin level reaches 1.2V, analog mute engages, regardless of digital audio level, and analog shutdown begins. (DAC and related circuitry powers down).

A timing diagram to show this is shown in Figure 85.

NOTE

The XSMT input pin voltage range is from -0.3V to DVDD + 0.3V.The ratio of external resistors must produce a voltage within this input range. Any increase in power supply (such as power supply positive noise or ripple) can pull the XSMT pin higher than DVDD+0.3V.

For example, if the PCM5242 is monitoring a 12V input, and dividing the voltage by 4, then the voltage at XSMT during ideal power supply conditions is 3V. A voltage spike higher than 14.4V causes a voltage greater than 3.6V (DVDD+0.3) on the XSMT pin, potentially damaging the device.

Providing the divider is set appropriately, any DC voltage can be monitored.

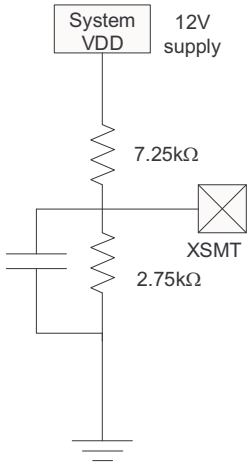


Figure 84. XSMT in External UVP Mode

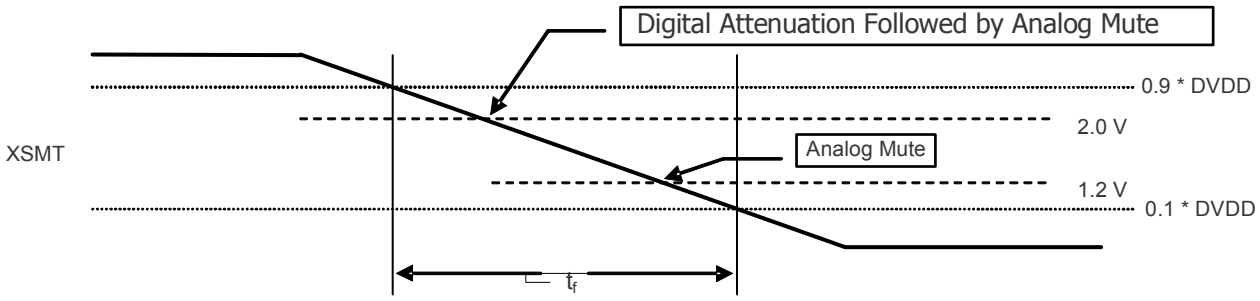


Figure 85. XSMT Timing for Undervoltage Protection

10.4 Power-On Reset Function

Power-On Reset, DVDD 3.3V Supply

The PCM5242 includes a power-on reset function shown in Figure 86. With V_{DD} > 2.8V, the power-on reset function is enabled. After the initialization period, the PCM5242 is set to its default reset state.

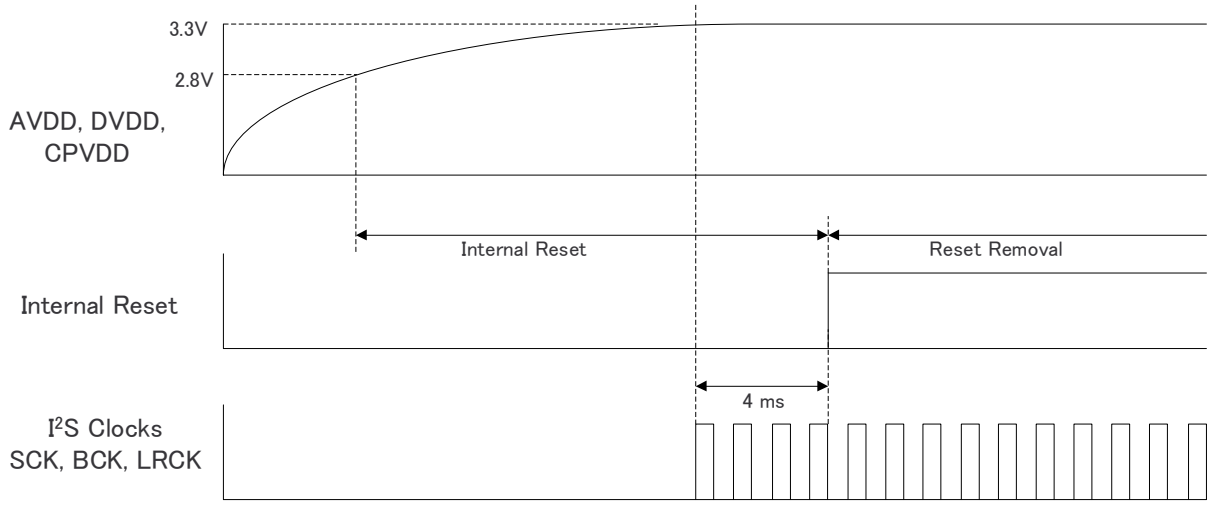


Figure 86. Power-On Reset Timing, DVDD = 3.3V

Power-On Reset Function (continued)

Power-On Reset, DVDD 1.8V Supply

The PCM5242 includes a power-on reset function shown in Figure 87 operating at DVDD=1.8V. With AVDD greater than approximately 2.8V, CPVDD greater than approximately 2.8V, and DVDD greater than approximately 1.5V, the power-on reset function is enabled. After the initialization period, the PCM5242 is set to its default reset state.

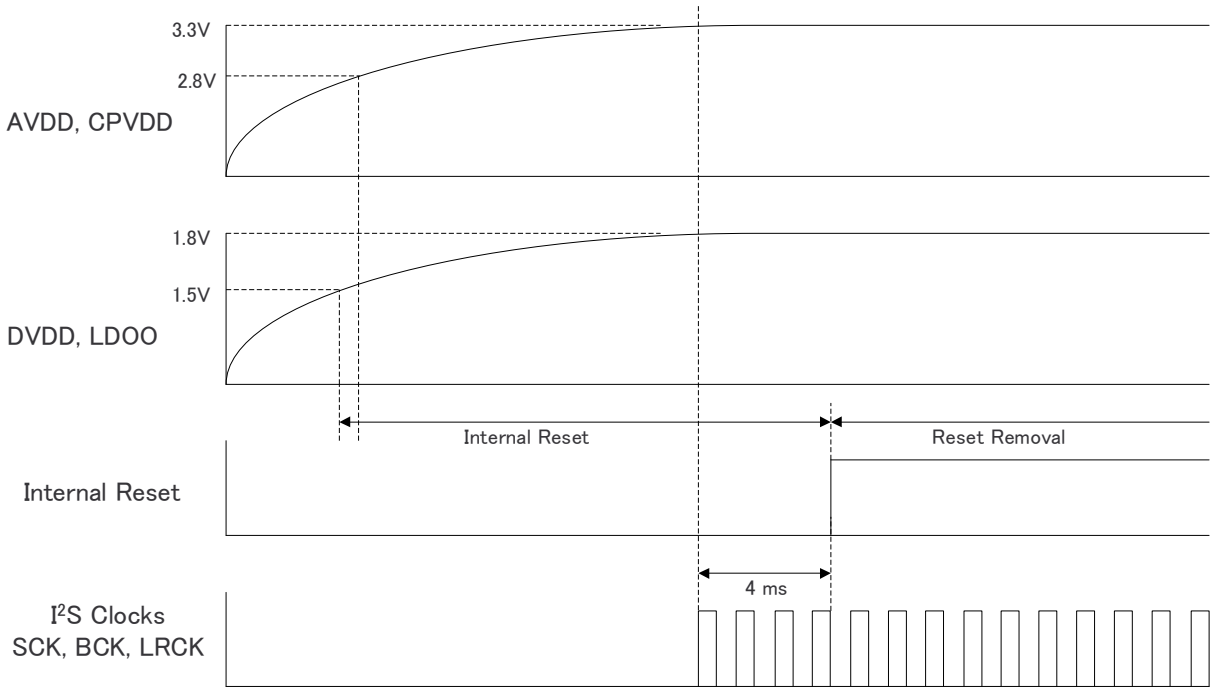


Figure 87. Power-On Reset Timing, DVDD = 1.8V

10.5 PCM5242 Power Modes

10.5.1 Setting Digital Power Supplies and I/O Voltage Rails

The internal digital core of the PCM5242 runs from a 1.8V supply. This can be generated by the internal LDO, or by an external 1.8V supply.

DVDD is used to set the I/O voltage, and to be used as the input to the onchip LDO that creates the 1.8V required by the digital core.

For systems that require 3.3V IO support, but lower power consumption, DVDD should be connected to 3.3V and LDOO can be connected to an external 1.8V source. Doing so will disable the onchip LDO.

When setting IO voltage to be 1.8V, both DVDD and LDOO must be provided with an external 1.8V supply.

PCM5242 Power Modes (continued)

10.5.2 Power Save Modes

The PCM5242 offers two power-save modes; standby and power-down.

When a clock error (SCK, BCK, and LRCK) or clock halt is detected, the PCM5242 automatically enters standby mode. The DAC and line driver are also powered down. The device can also be placed in standby mode via software command.

When BCK and LRCK remain at a low level for more than 1 second, the PCM5242 automatically enters power-down mode. Power-down mode disables the negative charge pump and bias/reference circuit, in addition to those disabled in standby mode. The device can also be placed in power-down mode via software command.

The detection time of BCK and LRCK halt can be controlled by Page 0, Register 44, D(2:0).

When expected Audio clocks (SCK, BCK, LRCK) are applied to the PCM5242, the device starts its powerup sequence automatically. The detection time for BCK and LRCK halt is programmable.

PCM5242 Power Modes (continued)

10.5.3 Power Save Parameter Programming

Register	Description
Page 0, Register 2, D(4)	Software standby mode command
Page 0, Register 2, D(0)	Software power-down command
Page 0, Register 2, D(4) and D(0)	Software power-up sequence command (required after software standby or power-down)
Page 0, Register 44, D(2:0)	Detection time of BCK and LRCK halt

11 Layout

11.1 Layout Guidelines

- The PCM5242 is a simple device to layout. Most engineers use a shared common ground for the entire device. GND can be consider AGND and DGND connected.
- Good system partitioning should keep digital clock and interface traces away from the differential analog outputs for highest analog performance. This reduces any high speed clock return currents influencing the analog outputs.
- Power supply and charge pump decoupling capacitors should be placed as close as possible to the device.
- The thermal pad on the underside of the package should be connected to GND.
- The top layer should be used for routing signals, whilst the bottom layer can be used for GND.

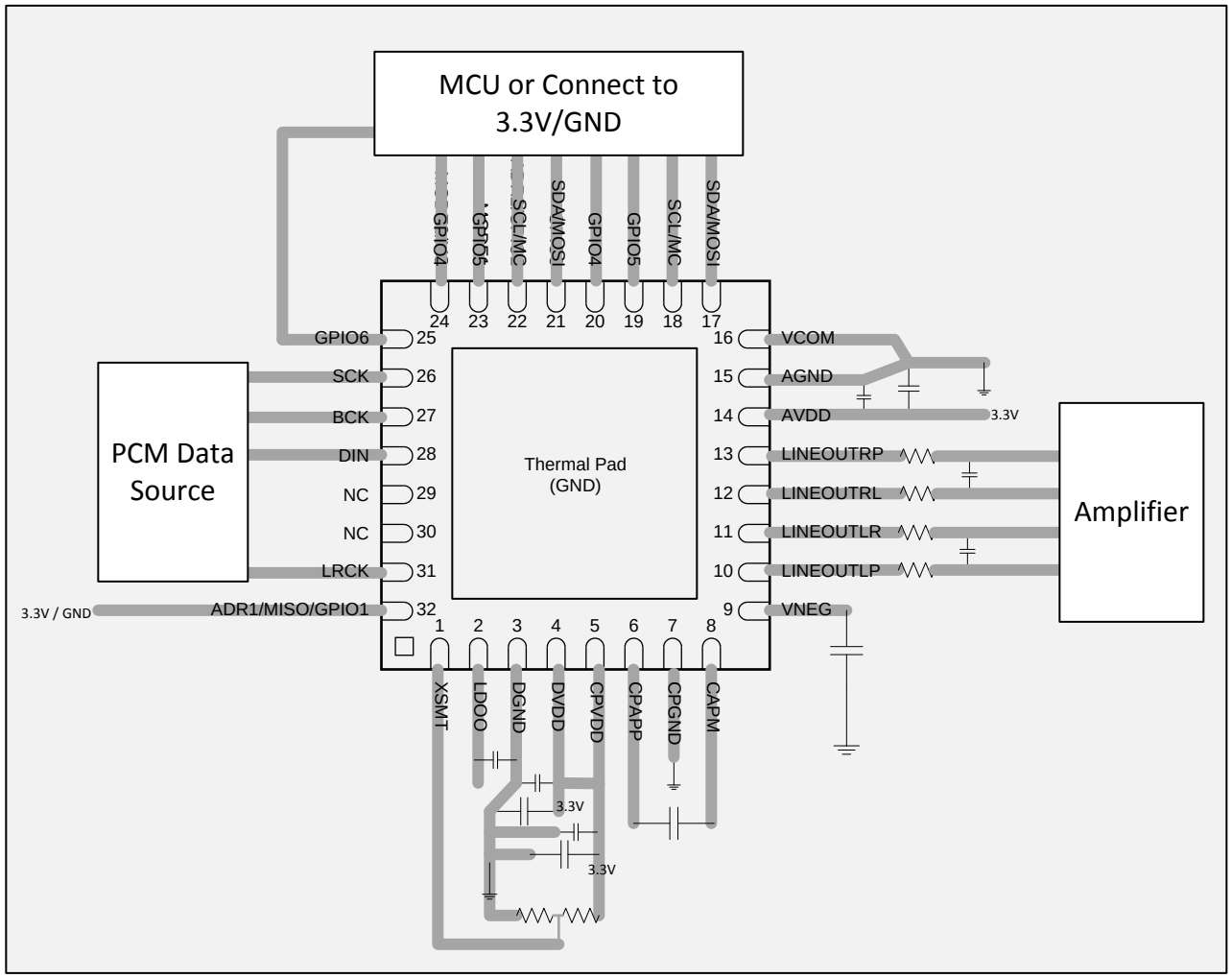


Figure 88. PCM5252 Layout Example

12 Programming and Registers Reference

12.1 Coefficient Data Formats

All mixer gain coefficients are 24-bit coefficients using a 4.20 number format. Numbers formatted as 4.20 numbers have 4 bits to the left of the binary point and 20 bits to the right of the binary point. If the most significant bit is logic 0, the number is a positive number. If the most significant bit is a logic 1, then the number is a negative number. In this case, every bit must be inverted, a 1 added to the result.

12.2 Power Down and Reset Behavior

Register values including those in the Coefficient Memory and Instruction Memory should remain when the device is put into power down mode. (PG0 Reg 0x02).

Register values in the device are reset to defaults when bit 0 or 4 of (Pg0, Reg 0x01) is set to 1. Please see the register description for more information.

12.3 PCM5242 Register Map

In any page, register 0 is the Page Select Register. The register value selects the Register Page from 0 to 255 for next read or write command.

Table 46. Register Map Overview

Register Number	Description
Page 0	
0	Page select register
1	Analog control register
2	Standby, Powerdown requests
3	Mute
4	PLL Lock Flag, PLL enable
5	Reserved
6	SPI MISO function select
7	De-emphasis enable, SDOUT select
8	GPIO enables
9	BCK, LRCLK configuration
10	DSP GPIO Input
11	Reserved
12	Master mode BCK, LRCLK reset
13	PLL clock source select
14 - 19	Reserved
20 - 24	PLL dividers
25, 26	Reserved
27	DSP clock divider
28	DAC clock divider
29	NCP clock divider
30	OSR clock divider
31	Reserved
32, 33	Master mode dividers
34	f_S speed mode
35, 36	IDAC (number of DSP clock cycles available in one audio frame)
37	Ignore various errors
38,39	Reserved
40, 41	I^2S configuration
42	DAC data path
43	DSP program selection
44	Clock missing detection period

Table 46. Register Map Overview (continued)

59	Auto mute time
60 - 64	Digital volume
65	Auto mute
75 - 79	Reserved
80 - 85	GPIOn output selection
86, 87	GPIO control
88, 89	Reserved
90	DSP overflow
91 - 94	Sample rate status
95 - 107	Reserved
108	Analog mute monitor
109 - 118	Reserved
119	GPIO input
120	Auto Mute flags
121	Reserved
Page 1	
1	Output amplitude type
2	Analog gain control
3, 4	Reserved
5	Undervoltage protection
6	Analog mute control
7	Analog gain boost
8, 9	VCOM configuration
Page 44	
1	Coefficient memory (CRAM) control
Pages 44 - 52	Coefficient buffer - A (256 coeffs x 24 bits) : See Table 47
Pages 62 - 70	Coefficient buffer - B (256 coeffs x 24 bits) : See Table 48
Pages 152 - 186	Instruction buffer (1024 instruction x 25 bits), I512 - I1023 are reserved.: See Table 49
Pages 187 - 252	Reserved
Page 253	
63, 64	Clock Flex Mode
Pages 254 - 255	Reserved

The PCM5242 has a register map split into multiple pages. Pages 0 and 1 control of the DAC and other on-chip peripherals. Pages 44 through 52 are used for Coefficient A memory, while Pages 62-70 are coefficient B memory. Pages 152-186 contain the miniDSP instruction memory. Page 253 is where the Clock Flex Mode register is located.

PCM5242 Register Page Structure

Page:	0	1	2-43	44-52	53-61	62-70	71-151	152-186	187-252	253	254-255
Func:	Control	Analog Control	Reserved	Coeffient A	Reserved	Coeffient B	Reserved	Instruction	Reserved	Clock Flex	Reserved
Desc:	General Control and Configuration	Analog Control		256 24-bit coefficients, 30 coefficients per page, 4 registers per coefficient		256 24-bit coefficients, 30 coefficients per page, 4 registers per coefficient		1024 24-bit instructions, 30 instructions per page, 4 registers per instruction		Clock Flex Mode	

Table 47. Coefficient Buffer-A Map

Coeff NO	Page NO	Base Register	Base Register+0	Base Register+1	Base Register+2	Base Register+3
C0	44	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C1	44	12	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..	..	..	..	..	..	..
C29	44	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C30	45	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..	..	..	..	..	..	..
C59	45	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C60	46	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..	..	..	..	..	..	..
C89	46	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C90	47	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..	..	..	..	..	..	..
C119	47	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C120	48	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..	..	..	..	..	..	..
C149	48	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C150	49	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..	..	..	..	..	..	..
C179	49	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C180	50	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..	..	..	..	..	..	..
C209	50	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C210	51	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..	..	..	..	..	..	..
C239	51	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C240	52	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..	..	..	..	..	..	..
C255	52	68	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

Table 48. Coefficient Buffer-B Map

Coeff NO	Page NO	Base Register	Base Register+0	Base Register+1	Base Register+2	Base Register+3
C0	62	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C1	62	12	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..	..	..	..	..	..	..
C29	62	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C30	63	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..	..	..	..	..	..	..
C59	63	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C60	64	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..	..	..	..	..	..	..
C89	64	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C90	65	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..	..	..	..	..	..	..
C119	65	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C120	66	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..	..	..	..	..	..	..
C149	66	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C150	67	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..	..	..	..	..	..	..
C179	67	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C180	68	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..	..	..	..	..	..	..
C209	68	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C210	69	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..	..	..	..	..	..	..
C239	69	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C240	70	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..	..	..	..	..	..	..
C255	70	68	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

minidsp

Table 49. miniDSP Instruction Map

Coeff NO	Page NO	Base Register	Base Register+0	Base Register+1	Base Register+2	Base Register+3
I0	152	8	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
I1	152	12	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
..	..	..	..	..	..	..
I29	152	124	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
I30	153	8	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
..	..	..	..	..	..	..
I59	153	124	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
I60	154	8	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
..	..	..	..	..	..	..
I89	154	124	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
I90	155	8	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
..	..	..	..	..	..	..
I119	155	124	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
I120	156	8	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
..	..	..	..	..	..	..

Table 49. miniDSP Instruction Map (continued)

I149	156	124	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
I150	157	8	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
..	..	..	..	..	..	..
I179	157	124	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
I180	158	8	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
..	..	..	..	..	..	..
I209	158	124	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
I210	159	8	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
..	..	..	..	..	..	..
I239	159	124	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
I240	160	8	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
..	..	..	..	..	..	..
I269	160	124	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
I270	161	8	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
..	..	..	..	..	..	..
I299	161	124	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
I300	162	8	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
..	..	..	..	..	..	..
I329	162	124	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
I330	163	8	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
..	..	..	..	..	..	..
I359	163	124	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
I360	164	8	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
..	..	..	..	..	..	..
I389	164	124	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
I390	165	8	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
..	..	..	..	..	..	..
I419	165	124	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
I420	166	8	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
..	..	..	..	..	..	..
I449	166	124	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
I450	167	8	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
..	..	..	..	..	..	..
I479	167	124	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
I480	168	8	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
..	..	..	..	..	..	..
I509	168	124	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
I510	169	8	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
I511	169	12	Instr(31:24)	Instr(23:16)	Instr(15:8)	Instr(7:0)
..	..	..	..	..	..	..
I539	169	124	Reserved.	Reserved.	Reserved.	Reserved.
I540	170	8	Reserved.	Reserved.	Reserved.	Reserved.
..	..	..	..	..	..	..
I569	170	124	Reserved.	Reserved.	Reserved.	Reserved.
I570	171	8	Reserved.	Reserved.	Reserved.	Reserved.
..	..	..	..	..	..	..
I599	171	124	Reserved.	Reserved.	Reserved.	Reserved.
I600	172	8	Reserved.	Reserved.	Reserved.	Reserved.

Table 49. miniDSP Instruction Map (continued)

..	..	..	..	..	..	..
I629	172	124	Reserved.	Reserved.	Reserved.	Reserved.
I630	173	8	Reserved.	Reserved.	Reserved.	Reserved.
..	..	..	..	..	..	..
I659	173	124	Reserved.	Reserved.	Reserved.	Reserved.
I660	174	8	Reserved.	Reserved.	Reserved.	Reserved.
..	..	..	..	..	..	..
I689	174	124	Reserved.	Reserved.	Reserved.	Reserved.
I690	175	8	Reserved.	Reserved.	Reserved.	Reserved.
..	..	..	..	..	..	..
I719	175	124	Reserved.	Reserved.	Reserved.	Reserved.
I720	176	8	Reserved.	Reserved.	Reserved.	Reserved.
..	..	..	..	..	..	..
I749	176	124	Reserved.	Reserved.	Reserved.	Reserved.
I750	177	8	Reserved.	Reserved.	Reserved.	Reserved.
..	..	..	..	..	..	..
I779	177	124	Reserved.	Reserved.	Reserved.	Reserved.
I780	178	8	Reserved.	Reserved.	Reserved.	Reserved.
..	..	..	..	..	..	..
I809	178	124	Reserved.	Reserved.	Reserved.	Reserved.
I810	179	8	Reserved.	Reserved.	Reserved.	Reserved.
..	..	..	..	..	..	..
I839	179	124	Reserved.	Reserved.	Reserved.	Reserved.
I840	180	8	Reserved.	Reserved.	Reserved.	Reserved.
..	..	..	..	..	..	..
I869	180	124	Reserved.	Reserved.	Reserved.	Reserved.
I870	181	8	Reserved.	Reserved.	Reserved.	Reserved.
..	..	..	..	..	..	..
I899	181	124	Reserved.	Reserved.	Reserved.	Reserved.
I900	182	8	Reserved.	Reserved.	Reserved.	Reserved.
..	..	..	..	..	..	..
I929	182	124	Reserved.	Reserved.	Reserved.	Reserved.
I930	183	8	Reserved.	Reserved.	Reserved.	Reserved.
..	..	..	..	..	..	..
I959	183	124	Reserved.	Reserved.	Reserved.	Reserved.
I960	184	8	Reserved.	Reserved.	Reserved.	Reserved.
..	..	..	..	..	..	..
I989	184	124	Reserved.	Reserved.	Reserved.	Reserved.
I990	185	8	Reserved.	Reserved.	Reserved.	Reserved.
..	..	..	..	..	..	..
I1019	185	124	Reserved.	Reserved.	Reserved.	Reserved.
I1020	186	8	Reserved.	Reserved.	Reserved.	Reserved.
..	..	..	..	..	..	..
I1023	186	20	Reserved.	Reserved.	Reserved.	Reserved.

12.3.1 Detailed Register Descriptions

12.3.1.1 Register Map Summary

Register Map Summary

Page 0									
Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
1	01	RSV	RSV	RSV	RSTM	RSV	RSV	RSV	RSTR
2	02	RSV	RSV	RSV	RQST	RSV	RSV	RSV	RQPD
3	03	RSV	RSV	RSV	RQML	RSV	RSV	RSV	RQMR
4	04	RSV	RSV	RSV	PLCK	RSV	RSV	RSV	PLLE
6	06	RSV	RSV	RSV	RSV	RSV	RSV	FSMI1	FSMI0
7	07	RSV	RSV	RSV	DEMP	RSV	RSV	RSV	SDSL
8	08	RSV	RSV	G6OE	G5OE	G4OE	G3OE	G2OE	G1OE
9	09	RSV	RSV	BCKP	BCKO	RSV	RSV	RSV	LRKO
10	0A	DSPG7	DSPG6	DSPG5	DSPG4	DSPG3	DSPG2	DSPG1	DSPG0
12	0C	RSV	RSV	RSV	RSV	RSV	RSV	RBCK	RLRK
13	0D	RSV	SREF2	SREF1	SREF0	RSV	RSV	RSV	RSV
14	0E	RSV	SDAC2	SDAC1	SDAC0	RSV	RSV	RSV	RSV
18	12	RSV	RSV	RSV	RSV	RSV	GREF2	GREF1	GREF0
19	13	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RQSY
20	14	RSV	RSV	RSV	RSV	PPDV3	PPDV2	PPDV1	PPDV0
21	15	RSV	RSV	PJDV5	PJDV4	PJDV3	PJDV2	PJDV1	PJDV0
22	16	RSV	RSV	PDDV13	PDDV12	PDDV11	PDDV10	PDDV9	PDDV8
23	17	PDDV7	PDDV6	PDDV5	PDDV4	PDDV3	PDDV2	PDDV1	PDDV0
24	18	RSV	RSV	RSV	RSV	PRDV3	PRDV2	PRDV1	PRDV0
27	1B	RSV	DDSP6	DDSP5	DDSP4	DDSP3	DDSP2	DDSP1	DDSP0
28	1C	RSV	DDAC6	DDAC5	DDAC4	DDAC3	DDAC2	DDAC1	DDAC0
29	1D	RSV	DNCP6	DNCP5	DNCP4	DNCP3	DNCP2	DNCP1	DNCP0
30	1E	RSV	DOSR6	DOSR5	DOSR4	DOSR3	DOSR2	DOSR1	DOSR0
32	20	RSV	DBCK6	DBCK5	DBCK4	DBCK3	DBCK2	DBCK1	DBCK0
33	21	DLRK7	DLRK6	DLRK5	DLRK4	DLRK3	DLRK2	DLRK1	DLRK0
34	22	RSV	RSV	RSV	I16E	RSV	RSV	FSSP1	FSSP0
35	23	IDAC15	IDAC14	IDAC13	IDAC12	IDAC11	IDAC10	IDAC9	IDAC8
36	24	IDAC7	IDAC6	IDAC5	IDAC4	IDAC3	IDAC2	IDAC1	IDAC0
37	25	RSV	IDFS	IDBK	IDSK	IDCH	IDCM	DCAS	IPLK
40	28	RSV	RSV	AFMT1	AFMT0	RSV	RSV	ALEN1	ALEN0
41	29	AOFS7	AOFS6	AOFS5	AOFS4	AOFS3	AOFS2	AOFS1	AOFS0
42	2A	RSV	RSV	AUPL1	AUPL0	RSV	RSV	AUPR1	AUPR0
43	2B	RSV	RSV	RSV	PSEL4	PSEL3	PSEL2	PSEL1	PSEL0
44	2C	RSV	RSV	RSV	RSV	RSV	CMDP2	CMDP1	CMDP0
59	3B	RSV	AMTL2	AMTL1	AMTL0	RSV	AMTR2	AMTR1	AMTR0
60	3C	RSV	RSV	RSV	RSV	RSV	RSV	PCTL1	PCTL0
61	3D	VOLL7	VOLL6	VOLL5	VOLL4	VOLL3	VOLL2	VOLL1	VOLL0
62	3E	VOLR7	VOLR6	VOLR5	VOLR4	VOLR3	VOLR2	VOLR1	VOLR0
63	3F	VNDF1	VNDF0	VNDS1	VNDS0	VNUF1	VNUF0	VNUS1	VNUS0
64	40	VEDF1	VEDF0	VEDS1	VEDS0	RSV	RSV	RSV	RSV
65	41	RSV	RSV	RSV	RSV	RSV	ACTL2	AMLE1	AMRE0
80	50	RSV	RSV	RSV	G1SL4	G1SL3	G1SL2	G1SL1	G1SL0
81	51	RSV	RSV	RSV	G2SL4	G2SL3	G2SL2	G2SL1	G2SL0

Register Map Summary (continued)

82	52	RSV	RSV	RSV	G3SL4	G3SL3	G3SL2	G3SL1	G3SL0
83	53	RSV	RSV	RSV	G4SL4	G4SL3	G4SL2	G4SL1	G4SL0
84	54	RSV	RSV	RSV	G5SL4	G5SL3	G5SL2	G5SL1	G5SL0
85	55	RSV	RSV	RSV	G6SL4	G6SL3	G6SL2	G6SL1	G6SL0
86	56	RSV	RSV	GOUT5	GOUT4	GOUT3	GOUT2	GOUT1	GOUT0
87	57	RSV	RSV	GINV5	GINV4	GINV3	GINV2	GINV1	GINV0
90	5A	RSV	RSV	RSV	L1OV	R1OV	L2OV	R2OV	SFOV
91	5B	RSV	DTFS2	DTFS1	DTFS0	DTSR3	DTSR2	DTSR1	DTSR0
92	5C	RSV	RSV	RSV	RSV	RSV	RSV	RSV	DTBR8
93	5D	DTBR7	DTBR6	DTBR5	DTBR4	DTBR3	DTBR2	DTBR1	DTBR0
94	5E	RSV	CDST	PLL-L	LrckBck	fS-SCKr	SCKval	BCKval	fSval
95	5F	RSV	RSV	RSV	LTSH	RSV	CKMF	CSRF	CERF
108	6C	RSV	RSV	RSV	RSV	RSV	RSV	AMLM	AMRM
109	6D	RSV	RSV	RSV	SDTM	RSV	RSV	RSV	SHTM
114	72	RSV	RSV	RSV	RSV	RSV	RSV	MTST1	MTST0
115	73	RSV	RSV	RSV	RSV	RSV	RSV	FSMM1	FSMM0
118	76	BOTM	RSV	RSV	RSV	PSTM3	PSTM2	PSTM1	PSTM0
119	77	RSV	RSV	GPIN5	GPIN4	GPIN3	GPIN2	GPIN1	RSV
120	78	RSV	RSV	RSV	AMFL	RSV	RSV	RSV	AMFR
121	79	RSV	RSV	RSV	RSV	RSV	RSV	RSV	DAMD
122	7A	RSV	RSV	RSV	RSV	RSV	RSV	RSV	EIFM
123	7B	RSV	G1MC2	G1MC1	G1MC0	RSV	G2MC2	G2MC1	G2MC0
124	7C	RSV	G3MC2	G3MC1	G3MC0	RSV	G4MC2	G4MC1	G4MC0
125	7D	RSV	G5MC2	G5MC1	G5MC0	RSV	G6MC2	G6MC1	G6MC0
Page 1									
Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
1	01	RSV	RSV	RSV	RSV	RSV	RSV	RSV	OSEL
2	02	RSV	RSV	RSV	LAGN	RSV	RSV	RSV	RAGN
5	05	RSV	RSV	RSV	RSV	RSV	RSV	UEPD	UIPD
6	06	RSV	RSV	RSV	RSV	RSV	RSV	RSV	AMCT
7	07	RSV	RSV	RSV	AGBL	RSV	RSV	RSV	AGBR
8	08	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RCMF
9	09	RSV	RSV	RSV	RSV	RSV	RSV	RSV	VCPD
Page 44									
Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
1	01	RSV	RSV	RSV	RSV	ACRM	AMDC	ACRS	ACSW
Page 253									
Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
63	3F	PLLFLEX17	PLLFLEX16	PLLFLEX15	PLLFLEX14	PLLFLEX13	PLLFLEX12	PLLFLEX11	PLLFLEX10
64	40	PLLFLEX27	PLLFLEX26	PLLFLEX25	PLLFLEX24	PLLFLEX23	PLLFLEX22	PLLFLEX21	PLLFLEX20

12.3.1.2 Page 0 Registers

Page 0 / Register 1

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
1	01	RSV	RSV	RSV	RSTM	RSV	RSV	RSV	RSTR
Reset Value					0				0

RSV	**Reserved** Reserved. Do not access.
RSTM	**Reset Modules** This bit resets the interpolation filter and the DAC modules. Since the DSP is also reset, the coeffient RAM content will also be cleared by the DSP. This bit is auto cleared and can be set only in standby mode. Default value: 0 0: Normal 1: Reset modules
RSTR	**Reset Registers** This bit resets the mode registers back to their initial values. The RAM content is not cleared, but the execution source will be back to ROM. This bit is auto cleared and must be set only when the DAC is in standby mode (resetting registers when the DAC is running is prohibited and not supported). Default value: 0 0: Normal 1: Reset mode registers

Page 0 / Register 2

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
2	02	RSV	RSV	RSV	RQST	RSV	RSV	RSV	RQPD
Reset Value					0				0

RSV	**Reserved** Reserved. Do not access.
RQST	**Standby Request** When this bit is set, the DAC will be forced into a system standby mode, which is also the mode the system enters in the case of clock errors. In this mode, most subsystems will be powered down but the charge pump and digital power supply. Default value: 0 0: Normal operation 1: Standby mode
RQPD	**Powerdown Request** When this bit is set, the DAC will be forced into powerdown mode, in which the power consumption would be minimum as the charge pump is also powered down. However, it will take longer to restart from this mode. This mode has higher precedence than the standby mode, i.e. setting this bit along with bit 4 for standby mode will result in the DAC going into powerdown mode. Default value: 0 0: Normal operation 1: Powerdown mode

Page 0 / Register 3

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
3	03	RSV	RSV	RSV	RQML	RSV	RSV	RSV	RQMR
Reset Value					0				0

RSV	**Reserved** Reserved. Do not access.
RQML	**Mute Left Channel** This bit issues soft mute request for the left channel. The volume will be smoothly ramped down/up to avoid pop/click noise. Default value: 0 0: Normal volume 1: Mute
RQMR	**Mute Right Channel**

	This bit issues soft mute request for the right channel. The volume will be smoothly ramped down/up to avoid pop/click noise. Default value: 0 0: Normal volume 1: Mute

Page 0 / Register 4

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
4	04	RSV	RSV	RSV	PLCK	RSV	RSV	RSV	PLLE
Reset Value									1

RSV	**Reserved** Reserved. Do not access.
PLCK	**PLL Lock Flag (Read Only)** This bit indicates whether the PLL is locked or not. When the PLL is disabled this bit always shows that the PLL is not locked. 0: The PLL is locked 1: The PLL is not locked
PLLE	**PLL Enable** This bit enables or disables the internal PLL. When PLL is disabled, the master clock will be switched to the SCK. Default value: 1 0: Disable PLL 1: Enable PLL

Page 0 / Register 6

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
6	06	RSV	RSV	RSV	RSV	RSV	RSV	FSMI1	FSMI0
Reset Value								0	0

RSV	**Reserved** Reserved. Do not access.
FSMI[1:0]	**SPI MISO function sel** These bits select the function of the SPI_MISO pin when in SPI mode. If the pin is set as GPIO, register readout via SPI is not possible. Default value: 00 00: SPI_MISO 01: GPIO1 Others: Reserved (Do not set)

Page 0 / Register 7

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
7	07	RSV	RSV	RSV	DEMP	RSV	RSV	RSV	SDSL
Reset Value					0				0

RSV	**Reserved** Reserved. Do not access.
DEMP	**De-Emphasis Enable** This bit enables or disables the de-emphasis filter. The default coefficients are for 44.1kHz sampling rate, but can be changed by reprogramming the appropriate coeffients in RAM. Default value: 0 0: De-emphasis filter is disabled

	1: De-emphasis filter is enabled
SDSL	**SDOUT Select** This bit selects what is being output as SDOUT via GPIO pins. Default value: 0 0: SDOUT is the DSP output (post-processing) 1: SDOUT is the DSP input (pre-processing)

Page 0 / Register 8

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
8	08	RSV	RSV	G6OE	G5OE	G4OE	G3OE	G2OE	G1OE
Reset Value				0	0	0	0	0	0

RSV	**Reserved** Reserved. Do not access.
G6OE	**GPIO6 Output Enable** This bit sets the direction of the GPIO6 pin Default value: 0 0: GPIO6 is input 1: GPIO6 is output
G5OE	**GPIO5 Output Enable** This bit sets the direction of the GPIO5 pin Default value: 0 0: GPIO5 is input 1: GPIO5 is output
G4OE	**GPIO4 Output Enable** This bit sets the direction of the GPIO4 pin Default value: 0 0: GPIO4 is input 1: GPIO4 is output
G3OE	**GPIO3 Output Enable** This bit sets the direction of the GPIO3 pin Default value: 0 0: GPIO3 is input 1: GPIO3 is output
G2OE	**GPIO2 Output Enable** This bit sets the direction of the GPIO2 pin Default value: 0 0: GPIO2 is input 1: GPIO2 is output
G1OE	**GPIO1 Output Enable** This bit sets the direction of the GPIO1 pin Default value: 0 0: GPIO1 is input 1: GPIO1 is output

Page 0 / Register 9

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
9	09	RSV	RSV	BCKP	BCKO	RSV	RSV	RSV	LRKO
Reset Value				0	0				0

RSV	**Reserved** Reserved. Do not access.
BCKP	**BCK Polarity** This bit sets the inverted BCK mode. In inverted BCK mode, the DAC assumes that the LRCK and DIN edges are aligned to the rising edge of the BCK. Normally they are assumed to be aligned to the falling edge of the BCK. Default value: 0 0: Normal BCK mode 1: Inverted BCK mode
BCKO	**BCK Output Enable** This bit sets the BCK pin direction to output for I2S master mode operation. In I2S master mode the PCM5xxx outputs the reference BCK and LRCK, and the external source device provides the DIN according to these clocks. Use Page 0 / Register 32 to program the division factor of the SCK to yield the desired BCK rate (normally 64FS) Default value: 0 0: BCK is input (I2S slave mode) 1: BCK is output (I2S master mode)
LRKO	**LRCLK Output Enable** This bit sets the LRCK pin direction to output for I2S master mode operation. In I2S master mode the PCM5xxx outputs the reference BCK and LRCK, and the external source device provides the DIN according to these clocks. Use Page 0 / Register 33 to program the division factor of the BCK to yield 1FS for LRCK. Default value: 0 0: LRCK is input (I2S slave mode) 1: LRCK is output (I2S master mode)

Page 0 / Register 10

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
10	0A	DSPG7	DSPG6	DSPG5	DSPG4	DSPG3	DSPG2	DSPG1	DSPG0
Reset Value		0	0	0	0	0	0	0	0

DSPG[7:0]	**DSP GPIO Input** The DSP accepts a 24-bit external control signals input. The value set in this register will go to bit 16:8 of this external input. Default value: 00000000

Page 0 / Register 12

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
12	0C	RSV	RSV	RSV	RSV	RSV	RSV	RBCK	RLRK
Reset Value								0	0

RSV	**Reserved** Reserved. Do not access.
RBCK	**Master Mode BCK Divider Reset** This bit, when set to 0, will reset the SCK divider to generate BCK clock for I2S master mode. To use I2S master mode, the divider must be enabled and programmed properly. Default value: 0 0: Master mode BCK clock divider is reset 1: Master mode BCK clock divider is functional
RLRK	**Master Mode LRCK Divider Reset** This bit, when set to 0, will reset the BCK divider to generate LRCK clock for I2S master mode. To use I2S master mode, the divider must be enabled and programmed properly. Default value: 0 0: Master mode LRCK clock divider is reset

	1: Master mode LRCK clock divider is functional

Page 0 / Register 13

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
13	0D	RSV	SREF2	SREF1	SREF0	RSV	RSV	RSV	RSV
Reset Value			0	0	0				

RSV	**Reserved** Reserved. Do not access.
SREF[2:0]	**PLL Reference** This bit select the source clock for internal PLL. This bit is ignored and overriden in clock auto set mode. Default value: 000 000: The PLL reference clock is SCK 001: The PLL reference clock is BCK 010: Reserved 011: The PLL reference clock is GPIO (selected using Page 0 / Register 18) others: Reserved (PLL reference is muted)
SREF	**PLL Reference** Default value: 0

Page 0 / Register 14

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
14	0E	RSV	SDAC2	SDAC1	SDAC0	RSV	RSV	RSV	RSV
Reset Value			0	0	0				

RSV	**Reserved** Reserved. Do not access.
SDAC[2:0]	**DAC clock source** These bits select the source clock for DAC clock divider. Default value: 000 This Register requires use of the Clock Flex Register 000: Master clock (PLL/SCK and OSC auto-select) 001: PLL clock 010: Reserved 011: SCK clock 100: BCK clock others: Reserved (muted)

Page 0 / Register 18

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
18	12	RSV	RSV	RSV	RSV	RSV	GREF2	GREF1	GREF0
Reset Value							0	0	0

RSV	**Reserved** Reserved. Do not access.
GREF[2:0]	**GPIO Source for PLL reference clk** These bits select the GPIO pins as clock input source when GPIO is selected as the PLL reference clock source. Default value: 000 This register requires use of the Clock Flex Register.000: GPIO1

	001: GPIO2 010: GPIO3 011: GPIO4 100: GPIO5 101: GPIO6 others: Reserved (muted)

Page 0 / Register 19

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
19	13	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RQSY
Reset Value									0

RSV	**Reserved** Reserved. Do not access.
RQSY	**Sync request** This bit, when set to 1 will issue the clock resynchronization by synchronously resets the DAC, CP and OSR clocks. The actual clock resynchronization takes place when this bit is set back to 0, where the DAC, CP and OSR clocks are resumed at the beginning of the audio frame. Default value: 0 0: Resume DAC, CP and OSR clocks synchronized to the beginning of audio frame 1: Halt DAC, CP and OSR clocks as the beginning of resynchronization process

Page 0 / Register 20

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
20	14	RSV	RSV	RSV	RSV	PPDV3	PPDV2	PPDV1	PPDV0
Reset Value						0	0	0	0

RSV	**Reserved** Reserved. Do not access.
PPDV[3:0]	**PLL P** These bits set the PLL divider P factor. These bits are ignored in clock auto set mode. Default value: 0000 0000: P=1 0001: P=2 ... 1110: P=15 1111: Prohibited (do not set this value)

Page 0 / Register 21

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
21	15	RSV	RSV	PJDV5	PJDV4	PJDV3	PJDV2	PJDV1	PJDV0
Reset Value				0	0	0	0	0	0

RSV	**Reserved** Reserved. Do not access.
PJDV[5:0]	**PLL J** These bits set the J part of the overall PLL multiplication factor J.D * R. These bits are ignored in clock auto set mode. Default value: 000000 000000: Prohibited (do not set this value) 000001: J=1

	000010: J=2 ... 111111: J=63

Page 0 / Register 22

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
22	16	RSV	RSV	PDDV13	PDDV12	PDDV11	PDDV10	PDDV9	PDDV8
Reset Value				0	0	0	0	0	0

Page 0 / Register 23

23	17	PDDV7	PDDV6	PDDV5	PDDV4	PDDV3	PDDV2	PDDV1	PDDV0
Reset Value		0	0	0	0	0	0	0	0

RSV	**Reserved** Reserved. Do not access.
PDDV[13:0]	**PLL D (MSB)** These bits set the D part of the overall PLL multiplication factor J.D * R. These bits are ignored in clock auto set mode. Default value: 00000000000000 0 (in decimal): D=0000 1 (in decimal): D=0001 ... 9999 (in decimal): D=9999 others: Prohibited (do not set)

Page 0 / Register 24

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
24	18	RSV	RSV	RSV	RSV	PRDV3	PRDV2	PRDV1	PRDV0
Reset Value						0	0	0	0

RSV	**Reserved** Reserved. Do not access.
PRDV[3:0]	**PLL R** These bits set the R part of the overall PLL multiplication factor J.D * R. These bits are ignored in clock auto set mode. Default value: 0000 0000: R=1 0001: R=2 ... 1111: R=16

Page 0 / Register 27

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
27	1B	RSV	DDSP6	DDSP5	DDSP4	DDSP3	DDSP2	DDSP1	DDSP0
Reset Value			0	0	0	0	0	0	0

RSV	**Reserved** Reserved. Do not access.
DDSP[6:0]	**DSP Clock Divider** These bits set the source clock divider value for the DSP clock. These bits are ignored in clock auto set mode.

	Default value: 0000000 0000000: Divide by 1 0000001: Divide by 2 ... 1111111: Divide by 128

Page 0 / Register 28

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
28	1C	RSV	DDAC6	DDAC5	DDAC4	DDAC3	DDAC2	DDAC1	DDAC0
Reset Value			0	0	0	0	0	0	0

RSV	**Reserved** Reserved. Do not access.
DDAC[6:0]	**DAC Clock Divider** These bits set the source clock divider value for the DAC clock. These bits are ignored in clock auto set mode. Default value: 0000000 0000000: Divide by 1 0000001: Divide by 2 ... 1111111: Divide by 128

Page 0 / Register 29

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
29	1D	RSV	DNCP6	DNCP5	DNCP4	DNCP3	DNCP2	DNCP1	DNCP0
Reset Value			0	0	0	0	0	0	0

RSV	**Reserved** Reserved. Do not access.
DNCP[6:0]	**NCP Clock Divider** These bits set the source clock divider value for the CP clock. These bits are ignored in clock auto set mode. Default value: 0000000 0000000: Divide by 1 0000001: Divide by 2 ... 1111111: Divide by 128

Page 0 / Register 30

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
30	1E	RSV	DOSR6	DOSR5	DOSR4	DOSR3	DOSR2	DOSR1	DOSR0
Reset Value			0	0	0	0	0	0	0

RSV	**Reserved** Reserved. Do not access.
DOSR[6:0]	**OSR Clock Divider** These bits set the source clock divider value for the OSR clock. These bits are ignored in clock auto set mode. Default value: 0000000 0000000: Divide by 1 0000001: Divide by 2 ... 1111111: Divide by 128

Page 0 / Register 32

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
32	20	RSV	DBCK6	DBCK5	DBCK4	DBCK3	DBCK2	DBCK1	DBCK0
Reset Value			0	0	0	0	0	0	0

RSV	**Reserved** Reserved. Do not access.
DBCK[6:0]	**Master Mode BCK Divider** These bits set the SCK divider value to generate I2S master BCK clock. Default value: 0000000 0000000: Divide by 1 0000001: Divide by 2 ... 1111111: Divide by 128

Page 0 / Register 33

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
33	21	DLRK7	DLRK6	DLRK5	DLRK4	DLRK3	DLRK2	DLRK1	DLRK0
Reset Value		0	0	0	0	0	0	0	0

DLRK[7:0]	**Master Mode LRCK Divider** These bits set the I2S master BCK clock divider value to generate I2S master LRCK clock. Default value: 00000000 00000000: Divide by 1 00000001: Divide by 2 ... 11111111: Divide by 256

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Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
34	22	RSV	RSV	RSV	I16E	RSV	RSV	FSSP1	FSSP0
Reset Value					0			0	0

RSV	**Reserved** Reserved. Do not access.
I16E	**16x Interpolation** This bit enables or disables the 16x interpolation mode Default value: 0 0: 8x interpolation 1: 16x interpolation
FSSP[1:0]	**FS Speed Mode** These bits select the FS operation mode, which must be set according to the current audio sampling rate. These bits are ignored in clock auto set mode. Default value: 00 00: Single speed (FS ≤ 48 kHz) 01: Double speed (48 kHz < FS ≤ 96 kHz) 10: Quad speed (96 kHz < FS ≤ 192 kHz) 11: Octal speed (192 kHz < FS ≤ 384 kHz)

Page 0 / Register 35

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
35	23	IDAC15	IDAC14	IDAC13	IDAC12	IDAC11	IDAC10	IDAC9	IDAC8
Reset Value		0	0	0	0	0	0	0	1

Page 0 / Register 36

36	24	IDAC7	IDAC6	IDAC5	IDAC4	IDAC3	IDAC2	IDAC1	IDAC0
Reset Value		0	0	0	0	0	0	0	0

IDAC[15:0]	**IDAC (MSB)** These bits specify the number of DSP clock cycles available in one audio frame. The value should match the DSP clock FS ratio. These bits are ignored in clock auto set mode. Default value: 0000000100000000

Page 0 / Register 37

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
37	25	RSV	IDFS	IDBK	IDSK	IDCH	IDCM	DCAS	IPLK
Reset Value			0	0	0	0	0	0	0

RSV	**Reserved** Reserved. Do not access.
IDFS	**Ignore FS Detection** This bit controls whether to ignore the FS detection. When ignored, FS error will not cause a clock error. Default value: 0 0: Regard FS detection 1: Ignore FS detection
IDBK	**Ignore BCK Detection** This bit controls whether to ignore the BCK detection against LRCK. The BCK must be stable between 32FS and 256FS inclusive or an error will be reported. When ignored, a BCK error will not cause a clock error. Default value: 0 0: Regard BCK detection 1: Ignore BCK detection
IDSK	**Ignore SCK Detection** This bit controls whether to ignore the SCK detection against LRCK. Only some certain SCK ratios within some error margin are allowed. When ignored, an SCK error will not cause a clock error. Default value: 0 0: Regard SCK detection 1: Ignore SCK detection
IDCH	**Ignore Clock Halt Detection** This bit controls whether to ignore the SCK halt (static or frequency is lower than acceptable) detection. When ignored an SCK halt will not cause a clock error. Default value: 0 0: Regard SCK halt detection 1: Ignore SCK halt detection
IDCM	**Ignore LRCK/BCK Missing Detection** This bit controls whether to ignore the LRCK/BCK missing detection. The LRCK/BCK need to be in low state (not only static) to be deemed missing. When ignored an LRCK/BCK missing will not cause the DAC go into powerdown mode. Default value: 0 0: Regard LRCK/BCK missing detection 1: Ignore LRCK/BCK missing detection

DCAS	**Disable Clock Divider Autoset** This bit enables or disables the clock auto set mode. When dealing with uncommon audio clock configuration, the auto set mode must be disabled and all clock dividers must be set manually. Addtionally, some clock detectors might also need to be disabled. The clock autoset feature will not work with PLL enabled in VCOM mode. In this case this feature has to be disabled and the clock dividers must be set manually. Default value: 0 0: Enable clock auto set 1: Disable clock auto set
IPLK	**Ignore PLL Lock Detection** This bit controls whether to ignore the PLL lock detection. When ignored, PLL unlocks will not cause a clock error. The PLL lock flag at Page 0 / Register 4, bit 4 is always correct regardless of this bit. Default value: 0 0: PLL unlocks raise clock error 1: PLL unlocks are ignored

Page 0 / Register 40

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
40	28	RSV	RSV	AFMT1	AFMT0	RSV	RSV	ALEN1	ALEN0
Reset Value				0	0			1	0

RSV	**Reserved** Reserved. Do not access.
AFMT[1:0]	**I2S Data Format** These bits control both input and output audio interface formats for DAC operation. Default value: 00 00: I2S 01: TDM/DSP 10: RTJ 11: LTJ
ALEN[1:0]	**I2S Word Length** These bits control both input and output audio interface sample word lengths for DAC operation. Default value: 10 00: 16 bits 01: 20 bits 10: 24 bits 11: 32 bits

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Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
41	29	AOFS7	AOFS6	AOFS5	AOFS4	AOFS3	AOFS2	AOFS1	AOFS0
Reset Value		0	0	0	0	0	0	0	0

AOFS[7:0]	**I2S Shift** These bits control the offset of audio data in the audio frame for both input and output. The offset is defined as the number of BCK from the starting (MSB) of audio frame to the starting of the desired audio sample. Default value: 00000000 00000000: offset = 0 BCK (no offset) 00000001: ofsset = 1 BCK 00000010: offset = 2 BCKs . . . 11111111: offset = 256 BCKs

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Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
42	2A	RSV	RSV	AUPL1	AUPL0	RSV	RSV	AUPR1	AUPR0
Reset Value				0	1			0	1

RSV	**Reserved** Reserved. Do not access.
AUPL[1:0]	**Left DAC Data Path** These bits control the left channel audio data path connection. Default value: 01 00: Zero data (mute) 01: Left channel data 10: Right channel data 11: Reserved (do not set)
AUPR[1:0]	**Right DAC Data Path** These bits control the right channel audio data path connection. Default value: 01 00: Zero data (mute) 01: Right channel data 10: Left channel data 11: Reserved (do not set)

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Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
43	2B	RSV	RSV	RSV	PSEL4	PSEL3	PSEL2	PSEL1	PSEL0
Reset Value					0	0	0	0	1

RSV	**Reserved** Reserved. Do not access.
PSEL[4:0]	**DSP Program Selection** These bits select the DSP program to use for audio processing. Default value: 00001 00000: Reserved (do not set) 00001: 8x/4x/2x FIR interpolation filter with de-emphasis 00010: 8x/4x/2x Low latency IIR interpolation filter with de-emphasis 00011: High attenuation x8/x4/x2 interpolation filter with de-emphasis 00100: Reserved 00101: Fixed process flow with configurable parameters 00110: Reserved (do not set) 00111: 8x Ringing-less low latency FIR interpolation filter without de-emphasis 11111: User program in RAM others: Reserved (do not set)

Page 0 / Register 44

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
44	2C	RSV	RSV	RSV	RSV	RSV	CMDP2	CMDP1	CMDP0
Reset Value							0	0	0

RSV	**Reserved** Reserved. Do not access.
CMDP[2:0]	**Clock Missing Detection Period** These bits set how long both BCK and LRCK keep low before the audio clocks deemed missing and the DAC transitions to powerdown mode. Default value: 000 000: about 1 second 001: about 2 seconds 010: about 3 seconds ... 111: about 8 seconds

Page 0 / Register 59

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
59	3B	RSV	AMTL2	AMTL1	AMTL0	RSV	AMTR2	AMTR1	AMTR0
Reset Value			0	0	0		0	0	0

RSV	**Reserved** Reserved. Do not access.
AMTL[2:0]	**Auto Mute Time for Left Channel** These bits specify the length of consecutive zero samples at left channel before the channel can be auto muted. The times shown are for 48 kHz sampling rate and will scale with other rates. Default value: 000 000: 21 ms 001: 106 ms 010: 213 ms 011: 533 ms 100: 1.07 sec 101: 2.13 sec 110: 5.33 sec 111: 10.66 sec
AMTR[2:0]	**Auto Mute Time for Right Channel** These bits specify the length of consecutive zero samples at right channel before the channel can be auto muted. The times shown are for 48 kHz sampling rate and will scale with other rates. Default value: 000 000: 21 ms 001: 106 ms 010: 213 ms 011: 533 ms 100: 1.07 sec 101: 2.13 sec 110: 5.33 sec 111: 10.66 sec

Page 0 / Register 60

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
60	3C	RSV	RSV	RSV	RSV	RSV	RSV	PCTL1	PCTL0
Reset Value								0	0

RSV	**Reserved** Reserved. Do not access.
PCTL[1:0]	**Digital Volume Control** These bits control the behavior of the digital volume. Default value: 00 00: The volume for Left and right channels are independent 01: Right channel volume follows left channel setting 10: Left channel volume follows right channel setting 11: Reserved (The volume for Left and right channels are independent)

Page 0 / Register 61

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
61	3D	VOLL7	VOLL6	VOLL5	VOLL4	VOLL3	VOLL2	VOLL1	VOLL0
Reset Value		0	0	1	1	0	0	0	0

VOLL[7:0]	**Left Digital Volume** These bits control the left channel digital volume. The digital volume is 24 dB to -103 dB in -0.5 dB step. Default value: 00110000 00000000: +24.0 dB 00000001: +23.5 dB . . . 00101111: +0.5 dB 00110000: 0.0 dB 00110001: -0.5 dB ... 11111110: -103 dB 11111111: Mute

Page 0 / Register 62

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
62	3E	VOLR7	VOLR6	VOLR5	VOLR4	VOLR3	VOLR2	VOLR1	VOLR0
Reset Value		0	0	1	1	0	0	0	0

VOLR[7:0]	**Right Digital Volume** These bits control the right channel digital volume. The digital volume is 24 dB to -103 dB in -0.5 dB step. Default value: 00110000 00000000: +24.0 dB 00000001: +23.5 dB . . . 00101111: +0.5 dB 00110000: 0.0 dB 00110001: -0.5 dB ... 11111110: -103 dB 11111111: Mute

Page 0 / Register 63

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
63	3F	VNDF1	VNDF0	VNDS1	VNDS0	VNUF1	VNUF0	VNUS1	VNUS0
Reset Value		0	0	1	0	0	0	1	0

VNDF[1:0]	**Digital Volume Normal Ramp Down Frequency** These bits control the frequency of the digital volume updates when the volume is ramping down. The setting here is applied to soft mute request, asserted by XSMUTE pin or Page 0 / Register 3. Default value: 00 00: Update every 1 FS period 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly set the volume to zero (Instant mute)
VNDS[1:0]	**Digital Volume Normal Ramp Down Step** These bits control the step of the digital volume updates when the volume is ramping down. The setting here is applied to soft mute request, asserted by XSMUTE pin or Page 0 / Register 3. Default value: 10 00: Decrement by 4 dB for each update 01: Decrement by 2 dB for each update 10: Decrement by 1 dB for each update 11: Decrement by 0.5 dB for each update
VNUF[1:0]	**Digital Volume Normal Ramp Up Frequency** These bits control the frequency of the digital volume updates when the volume is ramping up. The setting here is applied to soft unmute request, asserted by XSMUTE pin or Page 0 / Register 3. Default value: 00 00: Update every 1 FS period 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly restore the volume (Instant unmute)
VNUS[1:0]	**Digital Volume Normal Ramp Up Step** These bits control the step of the digital volume updates when the volume is ramping up. The setting here is applied to soft unmute request, asserted by XSMUTE pin or Page 0 / Register 3. Default value: 10 00: Increment by 4 dB for each update 01: Increment by 2 dB for each update 10: Increment by 1 dB for each update 11: Increment by 0.5 dB for each update

Page 0 / Register 64

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
64	40	VEDF1	VEDF0	VEDS1	VEDS0	RSV	RSV	RSV	RSV
Reset Value		0	0	0	0				

RSV	**Reserved** Reserved. Do not access.
VEDF[1:0]	**Digital Volume Emergency Ramp Down Frequency** These bits control the frequency of the digital volume updates when the volume is ramping down due to clock error or power outage, which usually needs faster ramp down compared to normal soft mute. Default value: 00 00: Update every 1 FS period 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly set the volume to zero (Instant mute)
VEDS[1:0]	**Digital Volume Emergency Ramp Down Step** These bits control the step of the digital volume updates when the volume is ramping down due to clock error or power outage, which usually needs faster ramp down compared to normal soft mute. Default value: 00

	00: Decrement by 4 dB for each update 01: Decrement by 2 dB for each update 10: Decrement by 1 dB for each update 11: Decrement by 0.5 dB for each update

Page 0 / Register 65

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
65	41	RSV	RSV	RSV	RSV	RSV	ACTL2	AMLE1	AMRE0
Reset Value							1	1	1

RSV	**Reserved** Reserved. Do not access.
ACTL[2:0]	**Auto Mute Control** This bit controls the behavior of the auto mute upon zero sample detection. The time length for zero detection is set with Page 0 / Register 59. Default value: 111 0: Auto mute left channel and right channel independently. 1: Auto mute left and right channels only when both channels are about to be auto muted.
AMLE[1:0]	**Auto Mute Left Channel** This bit enables or disables auto mute on right channel. Note that when right channel auto mute is disabled and the Page 0 / Register 65, bit 2 is set to 1, the left channel will also never be auto muted. Default value: 11 0: Disable right channel auto mute 1: Enable right channel auto mute
AMRE	**Auto Mute Right Channel** This bit enables or disables auto mute on left channel. Note that when left channel auto mute is disabled and the Page 0 / Register 65, bit 2 is set to 1, the right channel will also never be auto muted. Default value: 1 0: Disable left channel auto mute 1: Enable left channel auto mute

Page 0 / Register 80

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
80	50	RSV	RSV	RSV	G1SL4	G1SL3	G1SL2	G1SL1	G1SL0
Reset Value					0	0	0	0	0

RSV	**Reserved** Reserved. Do not access.
G1SL[4:0]	**GPIO1 Output Selection** These bits select the signal to output to GPIO1. To actually output the selected signal, the GPIO1 must be set to output mode at Page 0 / Register 8. Default value: 00000 00000: off (low) 00001: DSP GPIO1 output 00010: Register GPIO1 output (Page 0 / Register 86, bit 0) 00011: Auto mute flag (asserted when both L and R channels are auto muted) 00100: Auto mute flag for left channel 00101: Auto mute flag for right channel 00110: Clock invalid flag (clock error or clock changing or clock missing) 00111: Serial audio interface data output (SDOUT) 01000: Analog mute flag for left channel (low active)

	01001: Analog mute flag for right channel (low active) 01010: PLL lock flag 01011: Charge pump clock 01100: Reserved 01101: Reserved 01110: Under voltage flag, asserted when XSMUTE voltage is higher than 0.7 DVDD 01111: Under voltage flag, asserted when XSMUTE voltage is higher than 0.3 DVDD 010000: PLL Output/4 (Requires Clock Flex Register) OTHERS: RESERVED

Page 0 / Register 81

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
81	51	RSV	RSV	RSV	G2SL4	G2SL3	G2SL2	G2SL1	G2SL0
Reset Value					0	0	0	0	0

RSV	**Reserved** Reserved. Do not access.
G2SL[4:0]	**GPIO2 Output Selection** These bits select the signal to output to GPIO2. To actually output the selected signal, the GPIO2 must be set to output mode at Page 0 / Register 8. Default value: 00000 00000: off (low) 00001: DSP GPIO2 output 00010: Register GPIO2 output (Page 0 / Register 86, bit 1) 00011: Auto mute flag (asserted when both L and R channels are auto muted) 00100: Auto mute flag for left channel 00101: Auto mute flag for right channel 00110: Clock invalid flag (clock error or clock changing or clock missing) 00111: Serial audio interface data output (SDOUT) 01000: Analog mute flag for left channel (low active) 01001: Analog mute flag for right channel (low active) 01010: PLL lock flag 01011: Charge pump clock 01100: Reserved 01101: Reserved 01110: Under voltage flag, asserted when XSMUTE voltage is higher than 0.7 DVDD 01111: Under voltage flag, asserted when XSMUTE voltage is higher than 0.3 DVDD 010000: PLL Output/4 (Requires Clock Flex Register) OTHERS: RESERVED

Page 0 / Register 82

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
82	52	RSV	RSV	RSV	G3SL4	G3SL3	G3SL2	G3SL1	G3SL0
Reset Value					0	0	0	0	0

RSV	**Reserved** Reserved. Do not access.
G3SL[4:0]	**GPIO3 Output Selection** These bits select the signal to output to GPIO3. To actually output the selected signal, the GPIO3 must be set to output mode at Page 0 / Register 8.

	Default value: 00000 0000: off (low) 0001: DSP GPIO3 output 0010: Register GPIO3 output (Page 0 / Register 86, bit 2) 00011: Auto mute flag (asserted when both L and R channels are auto muted) 00100: Auto mute flag for left channel 00101: Auto mute flag for right channel 00110: Clock invalid flag (clock error or clock changing or clock missing) 00111: Serial audio interface data output (SDOUT) 01000: Analog mute flag for left channel (low active) 01001: Analog mute flag for right channel (low active) 01010: PLL lock flag 01011: Charge pump clock 01100: Reserved 01101: Reserved 01110: Under voltage flag, asserted when XSMUTE voltage is higher than 0.7 DVDD 01111: Under voltage flag, asserted when XSMUTE voltage is higher than 0.3 DVDD 010000: PLL Output/4 (Requires Clock Flex Register) OTHERS: RESERVED

Page 0 / Register 83

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
83	53	RSV	RSV	RSV	G4SL4	G4SL3	G4SL2	G4SL1	G4SL0
Reset Value					0	0	0	0	0

RSV	**Reserved** Reserved. Do not access.
G4SL[4:0]	**GPIO4 Output Selection** These bits select the signal to output to GPIO4. To actually output the selected signal, the GPIO4 must be set to output mode at Page 0 / Register 8. Default value: 00000 00000: off (low) 00001: DSP GPIO4 output 00010: Register GPIO4 output (Page 0 / Register 86, bit 3) 00011: Auto mute flag (asserted when both L and R channels are auto muted) 00100: Auto mute flag for left channel 00101: Auto mute flag for right channel 00110: Clock invalid flag (clock error or clock changing or clock missing) 00111: Serial audio interface data output (SDOUT) 01000: Analog mute flag for left channel (low active) 01001: Analog mute flag for right channel (low active) 01010: PLL lock flag 01011: Charge pump clock 01100: Reserved 01101: Reserved 01110: Under voltage flag, asserted when XSMUTE voltage is higher than 0.7 DVDD 01111: Under voltage flag, asserted when XSMUTE voltage is higher than 0.3 DVDD 010000: PLL Output/4 (Requires Clock Flex Register) OTHERS: RESERVED

Page 0 / Register 84

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
84	54	RSV	RSV	RSV	G5SL4	G5SL3	G5SL2	G5SL1	G5SL0
Reset Value					0	0	0	0	0

RSV	**Reserved** Reserved. Do not access.
G5SL[4:0]	**GPIO5 Output Selection** These bits select the signal to output to GPIO5. To actually output the selected signal, the GPIO5 must be set to output mode at Page 0 / Register 8. Default value: 00000 00000: off (low) 00001: DSP GPIO5 output 00010: Register GPIO5 output (Page 0 / Register 86, bit 4 00011: Auto mute flag (asserted when both L and R channels are auto muted) 00100: Auto mute flag for left channel 00101: Auto mute flag for right channel 00110: Clock invalid flag (clock error or clock changing or clock missing) 00111: Serial audio interface data output (SDOUT) 01000: Analog mute flag for left channel (low active) 01001: Analog mute flag for right channel (low active) 01010: PLL lock flag 01011: Charge pump clock 01100: Reserved 01101: Reserved 01110: Under voltage flag, asserted when XSMUTE voltage is higher than 0.7 DVDD 01111: Under voltage flag, asserted when XSMUTE voltage is higher than 0.3 DVDD 010000: PLL Output/4 (Requires Clock Flex Register) OTHERS: RESERVED

Page 0 / Register 85

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
85	55	RSV	RSV	RSV	G6SL4	G6SL3	G6SL2	G6SL1	G6SL0
Reset Value					0	0	0	0	0

RSV	**Reserved** Reserved. Do not access.
G6SL[4:0]	**GPIO6 Output Selection** These bits select the signal to output to GPIO6. To actually output the selected signal, the GPIO6 must be set to output mode at Page 0 / Register 8. Default value: 00000 00000: off (low) 00001: DSP GPIO6 output 00010: Register GPIO6 output (Page 0 / Register 86, bit 5) 00011: Auto mute flag (asserted when both L and R channels are auto muted) 00100: Auto mute flag for left channel 00101: Auto mute flag for right channel 00110: Clock invalid flag (clock error or clock changing or clock missing) 00111: Serial audio interface data output (SDOUT) 01000: Analog mute flag for left channel (low active)

	01001: Analog mute flag for right channel (low active) 01010: PLL lock flag 01011: Charge pump clock 01100: Reserved 01101: Reserved 01110: Under voltage flag, asserted when XSMUTE voltage is higher than 0.7 DVDD 01111: Under voltage flag, asserted when XSMUTE voltage is higher than 0.3 DVDD 010000: PLL Output/4 (Requires Clock Flex Register) OTHERS: RESERVED

Page 0 / Register 86

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
86	56	RSV	RSV	GOUT5	GOUT4	GOUT3	GOUT2	GOUT1	GOUT0
Reset Value				0	0	0	0	0	0

RSV	**Reserved** Reserved. Do not access.
GOUT5	**GPIO6 Output Control** This bit controls the GPIO6 output when the selection at Page 0 / Register 85 is set to 0010 (register output) Default value: 0 0: Output low 1: Output high
GOUT4	**GPIO5 Output Control** This bit controls the GPIO5 output when the selection at Page 0 / Register 84 is set to 0010 (register output) Default value: 0 0: Output low 1: Output high
GOUT3	**GPIO4 Output Control** This bit controls the GPIO4 output when the selection at Page 0 / Register 83 is set to 0010 (register output) Default value: 0 0: Output low 1: Output high
GOUT2	**GPIO3 Output Control** This bit controls the GPIO3 output when the selection at Page 0 / Register 82 is set to 0010 (register output) Default value: 0 0: Output low 1: Output high
GOUT1	**GPIO2 Output Control** This bit controls the GPIO2 output when the selection at Page 0 / Register 81 is set to 0010 (register output) Default value: 0 0: Output low 1: Output high
GOUT0	**GPIO1 Output Control** This bit controls the GPIO1 output when the selection at Page 0 / Register 80 is set to 0010 (register output) Default value: 0 0: Output low 1: Output high

Page 0 / Register 87

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
87	57	RSV	RSV	GINV5	GINV4	GINV3	GINV2	GINV1	GINV0
Reset Value				0	0	0	0	0	0

RSV	**Reserved** Reserved. Do not access.
GINV5	**GPIO6 Output Inversion** This bit controls the polarity of GPIO6 output. When set to 1, the output will be inverted for any signal being selected. Default value: 0 0: Non-inverted 1: Inverted
GINV4	**GPIO5 Output Inversion** This bit controls the polarity of GPIO5 output. When set to 1, the output will be inverted for any signal being selected. Default value: 0 0: Non-inverted 1: Inverted
GINV3	**GPIO4 Output Inversion** This bit controls the polarity of GPIO4 output. When set to 1, the output will be inverted for any signal being selected. Default value: 0 0: Non-inverted 1: Inverted
GINV2	**GPIO3 Output Inversion** This bit controls the polarity of GPIO3 output. When set to 1, the output will be inverted for any signal being selected. Default value: 0 0: Non-inverted 1: Inverted
GINV1	**GPIO2 Output Inversion** This bit controls the polarity of GPIO2 output. When set to 1, the output will be inverted for any signal being selected. Default value: 0 0: Non-inverted 1: Inverted
GINV0	**GPIO1 Output Inversion** This bit controls the polarity of GPIO1 output. When set to 1, the output will be inverted for any signal being selected. Default value: 0 0: Non-inverted 1: Inverted

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Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
90	5A	RSV	RSV	RSV	L1OV	R1OV	L2OV	R2OV	SFOV
Reset Value									

RSV	**Reserved** Reserved. Do not access.
L1OV	**Left1 Overflow (Read Only)** This bit indicates whether the left channel of DSP first output port has overflow. This bit is sticky and is cleared when read. 0: No overflow 1: Overflow occurred
R1OV	**Right1 Overflow (Read Only)** The bit indicates whether the right channel of DSP first output port has overflow. This bit is sticky and is cleared when read. 0: No overflow 1: Overflow occurred
L2OV	**Left2 Overflow (Read Only)** This bit indicates whether the left channel of DSP second output port has overflow. This bit is sticky and is cleared when read. 0: No overflow 1: Overflow occurred
R2OV	**Right2 Overflow (Read Only)** The bit indicates whether the right channel of DSP second output port has overflow. This bit is sticky and is cleared when read. 0: No overflow 1: Overflow occurred
SFOV	**Shifter Overflow (Read Only)** This bit indicates whether overflow occurred in the DSP shifter (possible sample corruption). This bit is sticky and is cleared when read. 0: No overflow 1: Overflow occurred

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Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
91	5B	RSV	DTFS2	DTFS1	DTFS0	DTSR3	DTSR2	DTSR1	DTSR0
Reset Value									

RSV	**Reserved** Reserved. Do not access.
DTFS[2:0]	**Detected FS (Read Only)** These bits indicate the currently detected audio sampling rate. 000: Error (Out of valid range) 001: 8 kHz 010: 16 kHz 011: 32-48 kHz 100: 88.2-96 kHz 101: 176.4-192 kHz 110: 384 kHz
DTSR[3:0]	**Detected SCK Ratio (Read Only)** These bits indicate the currently detected SCK ratio. Note that even if the SCK ratio is not indicated as error, clock error might still be flagged due to incompatible combination with the sampling rate. Specifically the SCK ratio must be high enough to allow enough DSP cycles for minimal audio processing when PLL is disabled. The absolute SCK frequency must also be lower than 50 MHz. 0000: Ratio error (The SCK ratio is not allowed) 0001: SCK = 32 FS 0010: SCK = 48 FS

	0011: SCK = 64 FS 0100: SCK = 128 FS 0101: SCK = 192 FS 0110: SCK = 256 FS 0111: SCK = 384 FS 1000: SCK = 512 FS 1001: SCK = 768 FS 1010: SCK = 1024 FS 1011: SCK = 1152 FS 1100: SCK = 1536 FS 1101: SCK = 2048 FS 1110: SCK = 3072 FS

Page 0 / Register 92

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
92	5C	RSV	RSV	RSV	RSV	RSV	RSV	RSV	DTBR8
Reset Value									

Page 0 / Register 93

93	5D	DTBR7	DTBR6	DTBR5	DTBR4	DTBR3	DTBR2	DTBR1	DTBR0
Reset Value									

RSV	**Reserved** Reserved. Do not access.
DTBR[8:0]	**Detected BCK Ratio (MSB) (Read Only)** These bits indicate the currently detected BCK ratio, i.e. the number of BCK clocks in one audio frame. Note that for extreme case of BCK = 1 FS (which is not usable anyway), the detected ratio will be unreliable.

Page 0 / Register 94

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
94	5E	RSV	CDST	PLL-L	LrckBck	fS-SCKr	SCKval	BCKval	fSval
Reset Value									

RSV	**Reserved** Reserved. Do not access.
CDST	**Clock Detector Status (Read Only)** This bit indicates whether the SCK clock is present or not. 0: SCK is present 1: SCK is missing (halted)
PLL-L	**PLL locked (Read Only)** This bit indicates whether the PLL is locked or not. The PLL will be reported as unlocked when it is disabled. 0: PLL is locked 1: PLL is unlocked
LrckBck	**LRCK-BCK present (Read Only)** This bit indicates whether the both LRCK and BCK are missing (tied low) or not. 0: LRCK and/or BCK is present 1: LRCK and BCK are missing
fS-SCKr	**Sample rate SCK ratio valid (Read Only)** This bit indicates whether the combination of current sampling rate and SCK ratio is valid for clock auto set. 0: The combination of FS/SCK ratio is valid

	1: Error (clock auto set is not possible)
SCKval	**SCK valid (Read Only)** This bit indicates whether the SCK is valid or not. The SCK ratio must be detectable to be valid. There is a limitation with this flag, that is, when the low period of LRCK is less than or equal to 5 BCKs, this flag will be asserted (SCK invalid reported). 0: SCK is valid 1: SCK is invalid
BCKval	**BCK valid (Read Only)** This bit indicates whether the BCK is valid or not. The BCK ratio must be stable and in the range of 32-256FS to be valid. 0: BCK is valid 1: BCK is invalid
fSval	**fS valid (Read Only)** This bit indicated whether the audio sampling rate is valid or not. The sampling rate must be detectable to be valid. There is a limitation with this flag, that is when this flag is asserted and Page 0 / Register 37 is set to ignore all asserted error flags such that the DAC recovers, this flag will be de-asserted (sampling rate invalid not reported anymore). 0: Sampling rate is valid 1: Sampling rate is invalid

Page 0 / Register 95

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
95	5F	RSV	RSV	RSV	LTSH	RSV	CKMF	CSRF	CERF
Reset Value									

RSV	**Reserved** Reserved. Do not access.
LTSH	**Latched Clock Halt (Read Only)** This bit indicates whether SCK halt has occurred. The bit is cleared when read. 0: SCK halt has not occurred 1: SCK halt has occurred since last read
CKMF	**Clock Missing (Read Only)** This bit indicates whether the LRCK and BCK are missing (tied low). 0: LRCK and/or BCK is present 1: LRCK and BCK are missing
CSRF	**Clock Resync Request (Read Only)** This bit indicates whether the clock resynchronization is in progress. 0: Not resynchronizing 1: Clock resynchronization is in progress
CERF	**Clock Error (Read Only)** This bit indicates whether a clock error is being reported. 0: Clock is valid 1: Clock is invalid (Error)

Page 0 / Register 108

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
108	6C	RSV	RSV	RSV	RSV	RSV	RSV	AMLM	AMRM
Reset Value									

RSV	**Reserved** Reserved. Do not access.
AMLM	**Left Analog Mute Monitor (Read Only)** This bit is a monitor for left channel analog mute status. 0: Mute 1: Unmute
AMRM	**Right Analog Mute Monitor (Read Only)** This bit is a monitor for right channel analog mute status. 0: Mute 1: Unmute

Page 0 / Register 109

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
109	6D	RSV	RSV	RSV	SDTM	RSV	RSV	RSV	SHTM
Reset Value									

RSV	**Reserved** Reserved. Do not access.
SDTM	**Short detect monitor (Read Only)** This bit indicates whether line output short is occuring. 0: Normal (No short) 1: Line output is being shorted
SHTM	**Short detected monitor (Read Only)** This bit indicates whether line output short has occurred since last read. This bit is sticky and is cleared when read. 0: No short 1: Line output short occurred

Page 0 / Register 114

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
114	72	RSV	RSV	RSV	RSV	RSV	RSV	MTST1	MTST0
Reset Value									

RSV	**Reserved** Reserved. Do not access.
MTST[1:0]	**MUTEZ status (Read Only)** These bits indicate the output of the XSMUTE level decoder for monitoring purpose. 11: 0.7 VDD ≤ XSMUTE 01: 0.3 VDD ≤ XSMUTE < 0.7 VDD 00: 0.3 VDD > XSMUTE

Page 0 / Register 115

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
115	73	RSV	RSV	RSV	RSV	RSV	RSV	FSMM1	FSMM0
Reset Value									

RSV	**Reserved** Reserved. Do not access.
FSMM[1:0]	**FS Speed Mode Monitor (Read Only)** These bits indicate the actual FS operation mode being used. The actual value is the auto set one when clock auto set is active and register set one when clock auto set is disabled.

	00: Single speed (FS ≤ 48 kHz) 01: Double speed (48 kHz < FS ≤ 96 kHz) 10: Quad speed (96 kHz < FS ≤ 192 kHz) 11: Octal speed (192 kHz < FS ≤ 384 kHz)

Page 0 / Register 118

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
118	76	BOTM	RSV	RSV	RSV	PSTM3	PSTM2	PSTM1	PSTM0
Reset Value									

RSV	**Reserved** Reserved. Do not access.
BOTM	**DSP Boot Done Flag (Read Only)** This bit indicates whether the DSP boot is completed. 0: DSP is booting 1: DSP boot completed
PSTM[3:0]	**Power State (Read Only)** These bits indicate the current power state of the DAC. 0000: Powerdown 0001: Wait for CP voltage valid 0010: Calibration 0011: Calibration 0100: Volume ramp up 0101: Run (Playing) 0110: Line output short / Low impedance 0111: Volume ramp down 1000: Standby

Page 0 / Register 119

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
119	77	RSV	RSV	GPIN5	GPIN4	GPIN3	GPIN2	GPIN1	RSV
Reset Value									

RSV	**Reserved** Reserved. Do not access.
GPIN[5:0]	**GPIO Input States (Read Only)** This bit indicates the logic level at GPIO6 pin. 0: Low 1: High

Page 0 / Register 120

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
120	78	RSV	RSV	RSV	AMFL	RSV	RSV	RSV	AMFR
Reset Value									

RSV	**Reserved** Reserved. Do not access.
AMFL	**Auto Mute Flag for Left Channel (Read Only)** This bit indicates the auto mute status for left channel. 0: Not auto muted

	1: Auto muted
AMFR	**Auto Mute Flag for Right Channel (Read Only)** This bit indicates the auto mute status for right channel. 0: Not auto muted 1: Auto muted

Page 0 / Register 121

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
121	79	RSV	RSV	RSV	RSV	RSV	RSV	RSV	DAMD
Reset Value									0

RSV	**Reserved** Reserved. Do not access.
DAMD	**DAC Mode** This bit controls the DAC architecture to vary the DAC auditory signature. Default value: 0 0: Mode1 - New hyper-advanced current-segment architecture 1: Mode2 - Classic PCM1792 advanced current-segment architecture

Page 0 / Register 122

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
122	7A	RSV	RSV	RSV	RSV	RSV	RSV	RSV	EIFM
Reset Value									0

RSV	**Reserved** Reserved. Do not access.
EIFM	**External Interpolation Filter Mode** This bit enables or disables the PCM1792 External Interpolation Filter Mode. This mode is used with a PCM1792 in external digital filter mode. Default value: 0 0: Normal mode 1: External Interpolation Filter Mode

Page 0 / Register 123

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
123	7B	RSV	G1MC2	G1MC1	G1MC0	RSV	G2MC2	G2MC1	G2MC0
Reset Value			0	0	0		0	0	0

RSV	**Reserved** Reserved. Do not access.
G1MC[2:0]	**GPIO1 output for External Interpolation Filter Mode** These bits select a signal to be output to GPIO1 in External Interpolation Filter mode. Default value: 000 000: Logic low 001: MS 010: BCK (256FS) 011: WDCK (8FS) 100: DATAL 101: DATAR 110: Raw DIN (from DIN pin)

	111: Raw LRCK (from LRCK pin)
G2MC[2:0]	**GPIO2 output for External Interpolation Filter Mode** These bits select a signal to be output to GPIO2 in External Interpolation Filter mode. Default value: 000 000: Logic low 001: MS 010: BCK (256FS) 011: WDCK (8FS) 100: DATAL 101: DATAR 110: Raw DIN (from DIN pin) 111: Raw LRCK (from LRCK pin)

Page 0 / Register 124

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
124	7C	RSV	G3MC2	G3MC1	G3MC0	RSV	G4MC2	G4MC1	G4MC0
Reset Value			0	0	0		0	0	0

RSV	**Reserved** Reserved. Do not access.
G3MC[2:0]	**GPIO3 output for External Interpolation Filter Mode** These bits select a signal to be output to GPIO3 in External Interpolation Filter Mode. Default value: 000 000: Logic low 001: MS 010: BCK (256FS) 011: WDCK (8FS) 100: DATAL 101: DATAR 110: Raw DIN (from DIN pin) 111: Raw LRCK (from LRCK pin)
G4MC[2:0]	**GPIO4 output for External Interpolation Filter Mode** These bits select a signal to be output to GPIO4 in External Interpolation Filter Mode. Default value: 000 000: Logic low 001: MS 010: BCK (256FS) 011: WDCK (8FS) 100: DATAL 101: DATAR 110: Raw DIN (from DIN pin) 111: Raw LRCK (from LRCK pin)

Page 0 / Register 125

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
125	7D	RSV	G5MC2	G5MC1	G5MC0	RSV	G6MC2	G6MC1	G6MC0
Reset Value			0	0	0		0	0	0

RSV	**Reserved** Reserved. Do not access.
G5MC[2:0]	**GPIO5 output for External Interpolation Filter Mode** These bits select a signal to be output to GPIO5 in External Interpolation Filter mode. Default value: 000 000: Logic low 001: MS 010: BCK (256FS) 011: WDCK (8FS) 100: DATAL 101: DATAR 110: Raw DIN (from DIN pin) 111: Raw LRCK (from LRCK pin)
G6MC[2:0]	**GPIO6 output for External Interpolation Filter Mode** These bits select a signal to be output to GPIO6 in External Interpolation Filter mode. Default value: 000 000: Logic low 001: MS 010: BCK (256FS) 011: WDCK (8FS) 100: DATAL 101: DATAR 110: Raw DIN (from DIN pin) 111: Raw LRCK (from LRCK pin)

12.3.1.3 Page 1 Registers

Page 1 / Register 1

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
1	01	RSV	RSV	RSV	RSV	RSV	RSV	RSV	OSEL
Reset Value									0

RSV	**Reserved** Reserved. Do not access.
OSEL	**Output Amplitude Type** This bit selects the output amplitude type. The clock autoset feature will not work with PLL enabled in VCOM mode. In this case this feature has to be disabled via Page 0 / Register 37 and the clock dividers must be set manually. Default value: 0 0: VREF mode (Constant output amplitude against AVDD variation) 1: VCOM mode (Output amplitude is proportional to AVDD variation)

Page 1 / Register 2

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
2	02	RSV	RSV	RSV	LAGN	RSV	RSV	RSV	RAGN
Reset Value					0				0

RSV	**Reserved** Reserved. Do not access.
LAGN	**Analog Gain Control for Left Channel** This bit controls the left channel analog gain.

	Default value: 0 0: 0 dB 1:-6 dB
RAGN	**Analog Gain Control for Right Channel** This bit controls the right channel analog gain. Default value: 0 0: 0 dB 1: -6 dB

Page 1 / Register 5

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
5	05	RSV	RSV	RSV	RSV	RSV	RSV	UEPD	UIPD
Reset Value								0	0

RSV	**Reserved** Reserved. Do not access.
UEPD	**External UVP Control** This bit enables or disables detection of power supply drop via XSMUTE pin (External Under Voltage Protection). Default value: 0 0: Enabled 1: Disabled
UIPD	**Internal UVP Control** This bit enables or disables internal detection of AVDD voltage drop (Internal Under Voltage Protection). Default value: 0 0: Enabled 1: Disabled

Page 1 / Register 6

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
6	06	RSV	RSV	RSV	RSV	RSV	RSV	RSV	AMCT
Reset Value									0

RSV	**Reserved** Reserved. Do not access.
AMCT	**Analog Mute Control** This bit enables or disables analog mute following digital mute. Default value: 0 0: Enabled 1: Disabled

Page 1 / Register 7

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
7	07	RSV	RSV	RSV	AGBL	RSV	RSV	RSV	AGBR
Reset Value					0				0

RSV	**Reserved** Reserved. Do not access.
AGBL	**Analog +10% Gain for Left Channel** This bit enables or disables amplitude boost mode for left channel.

	Default value: 0 0: Normal amplitude 1: +10% (+0.8 dB) boosted amplitude
AGBR	**Analog +10% Gain for Right Channel** This bit enables or disables amplitude boost mode for right channel. Default value: 0 0: Normal amplitude 1: +10% (+0.8 dB) boosted amplitude

Page 1 / Register 8

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
8	08	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RCMF
Reset Value									0

RSV	**Reserved** Reserved. Do not access.
RCMF	**VCOM Reference Ramp Up** This bit controls the VCOM voltage ramp up speed. Default value: 0 0: Normal ramp up, ~600ms with external capacitance = 1uF 1: Fast ramp up, ~3ms with external capacitance = 1uF

Page 1 / Register 9

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
9	09	RSV	RSV	RSV	RSV	RSV	RSV	RSV	VCPD
Reset Value									1

RSV	**Reserved** Reserved. Do not access.
VCPD	**Power down control for VCOM** This bit controls VCOM powerdown switch. Default value: 1 0: VCOM is powered on 1: VCOM is powered down

12.3.1.4 Page 44 Registers

Page 44 / Register 1

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
1	01	RSV	RSV	RSV	RSV	ACRM	AMDC	ACRS	ACSW
Reset Value							0		0

RSV	**Reserved** Reserved. Do not access.
ACRM	**Active CRAM Monitor (Read Only)** This bit indicates which CRAM is being accessed by the DSP when adaptive mode is disabled. When adaptive mode is enabled, this bit has no meaning. 0: CRAM A is being used by the DSP 1: CRAM B is being used by the DSP
AMDC	**Adaptive Mode Control**

	This bit controls the DSP adaptive mode. When in adaptive mode, only CRAM A is accessible via serial interface when the DSP is disabled (DAC in standby state), while when the DSP is enabled (DAC is run state) the CRAM A can only be accessed by the DSP and the CRAM B can only be accessed by the serial interface, or vice versa depending on the value of CRAMSTAT. When not in adaptive mode, both CRAM A and B can be accessed by the serial interface when the DSP is disabled, but when the DSP is enabled, no CRAM can be accessed by serial interface. The DSP can access either CRAM, which can be monitored at SWPMON. Default value: 0 0: Adaptive mode disabled 1: Adaptive mode enabled
ACRS	**Active CRAM Selection (Read Only)** This bit indicates which CRAM currently serves as the active one. The other CRAM serves as an update buffer, and can accessed by serial interface (SPI/I2C) 0: CRAM A is active and being used by the DSP 1: CRAM B is active and being used by the DSP
ACSW	**Switch Active CRAM** This bit is used to request switching roles of the two buffers, i.e. switching the active buffer role between CRAM A and CRAM B. This bit is cleared automatically when the switching process completed. Default value: 0 0: No switching requested or switching completed 1: Switching is being requested

12.3.1.5 Page 253 Registers

Page 253 / Register 63

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
63	3F	PLLFLEX17	PLLFLEX16	PLLFLEX15	PLLFLEX14	PLLFLEX13	PLLFLEX12	PLLFLEX11	PLLFLEX10
Reset Value		0	0	0	0	0	0	0	0

PLLFLEX1[7:0]	**Clock Flex Register #1** Clock Flex Register #1. Write 0x11 to this register to allow advanced clock tree functions. See Clocking Overview section. Default value: 00000000

Page 253 / Register 64

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
64	40	PLLFLEX27	PLLFLEX26	PLLFLEX25	PLLFLEX24	PLLFLEX23	PLLFLEX22	PLLFLEX21	PLLFLEX20
Reset Value		0	0	0	0	0	0	0	0

PLLFLEX2[7:0]	**Clock Flex Register #2** Clock Flex Register #2. Write 0xFF to this register to allow advanced clock tree functions. See Clocking Overview section. Default value: 00000000

12.3.2 PLL Tables for Software Controlled Devices

Table 50. Recommended Clock Divider Settings for PLL as Master Clock (VREF Mode)

f_S (kHz)	RSCK	SCK (MHz)	PLL VCO (MHz)	P	PLL REF (MHz)	M = K*R	K = J.D	R	PLL f_S	DSP f_S	NMAC	DSP CLK (MHz)	MOD f_S	MOD f (kHz)	NDAC	DOSR	% Error	NCP	CP f (kHz)
8	128	1.024	98.304	1	1.024	96	48	2	12288	1024	12	8.192	768	6144	16	48	0	4	1536
8	192	1.536	98.304	1	1.536	64	32	2	12288	1024	12	8.192	768	6144	16	48	0	4	1536
8	256	2.048	98.304	1	2.048	48	48	1	12288	1024	12	8.192	768	6144	16	48	0	4	1536
8	384	3.072	98.304	3	1.024	96	48	2	12288	1024	12	8.192	768	6144	16	48	0	4	1536
8	512	4.096	98.304	3	1.365	72	36	2	12288	1024	12	8.192	768	6144	16	48	0	4	1536
8	768	6.144	98.304	3	2.048	48	48	1	12288	1024	12	8.192	768	6144	16	48	0	4	1536
8	1024	8.192	98.304	3	2.731	36	36	1	12288	1024	12	8.192	768	6144	16	48	0	4	1536
8	1152	9.216	98.304	9	1.024	96	48	2	12288	1024	12	8.192	768	6144	16	48	0	4	1536
8	1536	12.288	98.304	9	1.365	72	36	2	12288	1024	12	8.192	768	6144	16	48	0	4	1536
8	2048	16.384	98.304	9	1.82	54	54	1	12288	1024	12	8.192	768	6144	16	48	0	4	1536
8	3072	24.576	98.304	9	2.731	36	36	1	12288	1024	12	8.192	768	6144	16	48	0	4	1536
11.025	128	1.4112	90.3168	1	1.411	64	32	2	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
11.025	192	2.1168	90.3168	3	0.706	128	32	4	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
11.025	256	2.8224	90.3168	1	2.822	32	32	1	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
11.025	384	4.2336	90.3168	3	1.411	64	32	2	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
11.025	512	5.6448	90.3168	3	1.882	48	48	1	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
11.025	768	8.4672	90.3168	3	2.822	32	32	1	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
11.025	1024	11.2896	90.3168	3	3.763	24	24	1	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
11.025	1152	12.7008	90.3168	9	1.411	64	32	2	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
11.025	1536	16.9344	90.3168	9	1.882	48	48	1	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
11.025	2048	22.5792	90.3168	9	2.509	36	36	1	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
11.025	3072	33.8688	90.3168	9	3.763	24	24	1	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
16	64	1.024	98.304	1	1.024	96	48	2	6144	1024	6	16.384	384	6144	16	24	0	4	1536
16	128	2.048	98.304	1	2.048	48	48	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
16	192	3.072	98.304	1	3.072	32	32	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
16	256	4.096	98.304	1	4.096	24	24	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
16	384	6.144	98.304	3	2.048	48	48	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
16	512	8.192	98.304	3	2.731	36	36	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
16	768	12.288	98.304	3	4.096	24	24	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
16	1024	16.384	98.304	3	5.461	18	18	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
16	1152	18.432	98.304	3	6.144	16	16	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
16	1536	24.576	98.304	9	2.731	36	36	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
16	2048	32.768	98.304	9	3.641	27	27	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
16	3072	49.152	98.304	9	5.461	18	18	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
22.05	64	1.4112	90.3168	1	1.411	64	32	2	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
22.05	128	2.8224	90.3168	1	2.822	32	32	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
22.05	192	4.2336	90.3168	3	1.411	64	32	2	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
22.05	256	5.6448	90.3168	1	5.645	16	16	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2

Table 50. Recommended Clock Divider Settings for PLL as Master Clock (VREF Mode) (continued)

f_S (kHz)	RSCK	SCK (MHz)	PLL VCO (MHz)	P	PLL REF (MHz)	M = K*R	K = J.D	R	PLL f_S	DSP f_S	NMAC	DSP CLK (MHz)	MOD f_S	MOD f (kHz)	NDAC	DOSR	% Error	NCP	CP f (kHz)
22.05	384	8.4672	90.3168	3	2.822	32	32	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
22.05	512	11.2896	90.3168	3	3.763	24	24	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
22.05	768	16.9344	90.3168	3	5.645	16	16	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
22.05	1024	22.5792	90.3168	3	7.526	12	12	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
22.05	1152	25.4016	90.3168	9	2.822	32	32	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
22.05	1536	33.8688	90.3168	9	3.763	24	24	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
22.05	2048	45.1584	90.3168	9	5.018	18	18	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
32	32	1.024	98.304	1	1.024	96	48	2	3072	1024	3	32.768	192	6144	16	12	0	4	1536
32	48	1.536	98.304	1	1.536	64	16	4	3072	1024	3	32.768	192	6144	16	12	0	4	1536
32	64	2.048	98.304	1	2.048	48	24	2	3072	1024	3	32.768	192	6144	16	12	0	4	1536
32	128	4.096	98.304	1	4.096	24	24	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
32	192	6.144	98.304	3	2.048	48	48	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
32	256	8.192	98.304	2	4.096	24	24	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
32	384	12.288	98.304	3	4.096	24	24	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
32	512	16.384	98.304	3	5.461	18	18	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
32	768	24.576	98.304	3	8.192	12	12	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
32	1024	32.768	98.304	3	10.923	9	9	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
32	1152	36.864	98.304	9	4.096	24	24	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
32	1536	49.152	98.304	6	8.192	12	12	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
44.1	32	1.4112	90.3168	1	1.411	64	32	2	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
44.1	64	2.8224	90.3168	1	2.822	32	16	2	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
44.1	128	5.6448	90.3168	1	5.645	16	16	1	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
44.1	192	8.4672	90.3168	3	2.822	32	32	1	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
44.1	256	11.2896	90.3168	2	5.645	16	16	1	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
44.1	384	16.9344	90.3168	3	5.645	16	16	1	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
44.1	512	22.5792	90.3168	3	7.526	12	12	1	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
44.1	768	33.8688	90.3168	3	11.29	8	8	1	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
44.1	1024	45.1584	90.3168	3	15.053	6	6	1	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
48	32	1.536	98.304	1	1.536	64	32	2	2048	1024	2	49.152	128	6144	16	8	0	4	1536
48	64	3.072	98.304	1	3.072	32	16	2	2048	1024	2	49.152	128	6144	16	8	0	4	1536
48	128	6.144	98.304	1	6.144	16	16	1	2048	1024	2	49.152	128	6144	16	8	0	4	1536
48	192	9.216	98.304	3	3.072	32	32	1	2048	1024	2	49.152	128	6144	16	8	0	4	1536
48	256	12.288	98.304	2	6.144	16	16	1	2048	1024	2	49.152	128	6144	16	8	0	4	1536
48	384	18.432	98.304	3	6.144	16	16	1	2048	1024	2	49.152	128	6144	16	8	0	4	1536
48	512	24.576	98.304	3	8.192	12	12	1	2048	1024	2	49.152	128	6144	16	8	0	4	1536
48	768	36.864	98.304	3	12.288	8	8	1	2048	1024	2	49.152	128	6144	16	8	0	4	1536
48	1024	49.152	98.304	3	16.384	6	6	1	2048	1024	2	49.152	128	6144	16	8	0	4	1536
96	32	3.072	98.304	1	3.072	32	16	2	1024	512	2	49.152	64	6144	16	4	0	4	1536

Table 50. Recommended Clock Divider Settings for PLL as Master Clock (VREF Mode) (continued)

f_S (kHz)	RSCK	SCK (MHz)	PLL VCO (MHz)	P	PLL REF (MHz)	M = K*R	K = J.D	R	PLL f_S	DSP f_S	NMAC	DSP CLK (MHz)	MOD f_S	MOD f (kHz)	NDAC	DOSR	% Error	NCP	CP f (kHz)
96	48	4.608	98.304	3	1.536	64	32	2	1024	512	2	49.152	64	6144	16	4	0	4	1536
96	64	6.144	98.304	1	6.144	16	8	2	1024	512	2	49.152	64	6144	16	4	0	4	1536
96	128	12.288	98.304	2	6.144	16	16	1	1024	512	2	49.152	64	6144	16	4	0	4	1536
96	192	18.432	98.304	3	6.144	16	16	1	1024	512	2	49.152	64	6144	16	4	0	4	1536
96	256	24.576	98.304	4	6.144	16	16	1	1024	512	2	49.152	64	6144	16	4	0	4	1536
96	384	36.864	98.304	6	6.144	16	16	1	1024	512	2	49.152	64	6144	16	4	0	4	1536
96	512	49.152	98.304	8	6.144	16	16	1	1024	512	2	49.152	64	6144	16	4	0	4	1536
192	32	6.144	98.304	1	6.144	16	8	2	512	256	2	49.152	32	6144	16	2	0	4	1536
192	48	9.216	98.304	3	3.072	32	16	2	512	256	2	49.152	32	6144	16	2	0	4	1536
192	64	12.288	98.304	1	12.288	8	4	2	512	256	2	49.152	32	6144	16	2	0	4	1536
192	128	24.576	98.304	2	12.288	8	8	1	512	256	2	49.152	32	6144	16	2	0	4	1536
192	192	36.864	98.304	3	12.288	8	8	1	512	256	2	49.152	32	6144	16	2	0	4	1536
192	256	49.152	98.304	4	12.288	8	8	1	512	256	2	49.152	32	6144	16	2	0	4	1536
384	32	12.288	98.304	2	6.144	16	8	2	256	128	2	49.152	16	6144	16	1	0	4	1536
384	48	18.432	98.304	3	6.144	16	8	2	256	128	2	49.152	16	6144	16	1	0	4	1536
384	64	24.576	98.304	2	12.288	8	4	2	256	128	2	49.152	16	6144	16	1	0	4	1536
384	128	49.152	98.304	4	12.288	8	8	1	256	128	2	49.152	16	6144	16	1	0	4	1536

Table 51. Recommended Clock Divider Settings for PLL as Master Clock (VCOM Mode)

f_S (kHz)	RSCK	SCK (MHz)	PLL VCO (MHz)	P	PLL REF (MHz)	M = K*R	K = J.D	R	PLL f_S	DSP f_S	NMAC	DSP CLK (MHz)	MOD f_S	MOD f (kHz)	NDAC	DOSR	% Error	NCP	CP f (kHz)
8	128	1.024	73.728	1	1.024	72	36	2	9216	768	12	6.144	768	6144	12	48	0	4	1536
8	192	1.536	73.728	1	1.536	48	24	2	9216	768	12	6.144	768	6144	12	48	0	4	1536
8	256	2.048	73.728	1	2.048	36	36	1	9216	768	12	6.144	768	6144	12	48	0	4	1536
8	384	3.072	73.728	1	3.072	24	12	2	9216	768	12	6.144	768	6144	12	48	0	4	1536
8	512	4.096	73.728	2	2.048	36	36	1	9216	768	12	6.144	768	6144	12	48	0	4	1536
8	768	6.144	73.728	3	2.048	36	36	1	9216	768	12	6.144	768	6144	12	48	0	4	1536
8	1024	8.192	73.728	4	2.048	36	36	1	9216	768	12	6.144	768	6144	12	48	0	4	1536
8	1152	9.216	73.728	6	1.536	48	48	1	9216	768	12	6.144	768	6144	12	48	0	4	1536
8	1536	12.288	73.728	6	2.048	36	36	1	9216	768	12	6.144	768	6144	12	48	0	4	1536
8	2048	16.384	73.728	8	2.048	36	36	1	9216	768	12	6.144	768	6144	12	48	0	4	1536
8	3072	24.576	73.728	12	2.048	36	36	1	9216	768	12	6.144	768	6144	12	48	0	4	1536
11.025	128	1.4112	84.672	1	1.411	60	30	2	7680	960	8	10.584	512	5644.8	15	32	0	4	1411.2
11.025	192	2.1168	84.672	1	2.117	40	10	4	7680	960	8	10.584	512	5644.8	15	32	0	4	1411.2
11.025	256	2.8224	84.672	1	2.822	30	30	1	7680	960	8	10.584	512	5644.8	15	32	0	4	1411.2
11.025	384	4.2336	84.672	2	2.117	40	20	2	7680	960	8	10.584	512	5644.8	15	32	0	4	1411.2
11.025	512	5.6448	84.672	2	2.822	30	30	1	7680	960	8	10.584	512	5644.8	15	32	0	4	1411.2
11.025	768	8.4672	84.672	3	2.822	30	30	1	7680	960	8	10.584	512	5644.8	15	32	0	4	1411.2
11.025	1024	11.2896	84.672	4	2.822	30	30	1	7680	960	8	10.584	512	5644.8	15	32	0	4	1411.2
11.025	1152	12.7008	84.672	6	2.117	40	20	2	7680	960	8	10.584	512	5644.8	15	32	0	4	1411.2
11.025	1536	16.9344	84.672	8	2.117	40	40	1	7680	960	8	10.584	512	5644.8	15	32	0	4	1411.2
11.025	2048	22.5792	84.672	8	2.822	30	30	1	7680	960	8	10.584	512	5644.8	15	32	0	4	1411.2
11.025	3072	33.8688	84.672	8	4.234	20	20	1	7680	960	8	10.584	512	5644.8	15	32	0	4	1411.2
16	64	1.024	73.728	1	1.024	72	36	2	4608	768	6	12.288	384	6144	12	24	0	4	1536
16	128	2.048	73.728	1	2.048	36	36	1	4608	768	6	12.288	384	6144	12	24	0	4	1536
16	192	3.072	73.728	1	3.072	24	24	1	4608	768	6	12.288	384	6144	12	24	0	4	1536
16	256	4.096	73.728	2	2.048	36	36	1	4608	768	6	12.288	384	6144	12	24	0	4	1536
16	384	6.144	73.728	3	2.048	36	36	1	4608	768	6	12.288	384	6144	12	24	0	4	1536
16	512	8.192	73.728	4	2.048	36	36	1	4608	768	6	12.288	384	6144	12	24	0	4	1536
16	768	12.288	73.728	6	2.048	36	36	1	4608	768	6	12.288	384	6144	12	24	0	4	1536
16	1024	16.384	73.728	8	2.048	36	36	1	4608	768	6	12.288	384	6144	12	24	0	4	1536
16	1152	18.432	73.728	9	2.048	36	36	1	4608	768	6	12.288	384	6144	12	24	0	4	1536
16	1536	24.576	73.728	8	3.072	24	24	1	4608	768	6	12.288	384	6144	12	24	0	4	1536
16	2048	32.768	73.728	8	4.096	18	18	1	4608	768	6	12.288	384	6144	12	24	0	4	1536
16	3072	49.152	73.728	8	6.144	12	12	1	4608	768	6	12.288	384	6144	12	24	0	4	1536
22.05	64	1.4112	84.672	1	1.411	60	30	2	3840	960	4	21.168	256	5644.8	15	16	0	4	1411.2
22.05	128	2.8224	84.672	1	2.822	30	30	1	3840	960	4	21.168	256	5644.8	15	16	0	4	1411.2
22.05	192	4.2336	84.672	3	1.411	60	30	2	3840	960	4	21.168	256	5644.8	15	16	0	4	1411.2
22.05	256	5.6448	84.672	2	2.822	30	30	1	3840	960	4	21.168	256	5644.8	15	16	0	4	1411.2

Table 51. Recommended Clock Divider Settings for PLL as Master Clock (VCOM Mode) (continued)

f_S (kHz)	RSCK	SCK (MHz)	PLL VCO (MHz)	P	PLL REF (MHz)	M = K*R	K = J.D	R	PLL f_S	DSP f_S	NMAC	DSP CLK (MHz)	MOD f_S	MOD f (kHz)	NDAC	DOSR	% Error	NCP	CP f (kHz)
22.05	384	8.4672	84.672	3	2.822	30	30	1	3840	960	4	21.168	256	5644.8	15	16	0	4	1411.2
22.05	512	11.2896	84.672	2	5.645	15	15	1	3840	960	4	21.168	256	5644.8	15	16	0	4	1411.2
22.05	768	16.9344	84.672	3	5.645	15	15	1	3840	960	4	21.168	256	5644.8	15	16	0	4	1411.2
22.05	1024	22.5792	84.672	4	5.645	15	15	1	3840	960	4	21.168	256	5644.8	15	16	0	4	1411.2
22.05	1152	25.4016	84.672	9	2.822	30	30	1	3840	960	4	21.168	256	5644.8	15	16	0	4	1411.2
22.05	1536	33.8688	84.672	8	4.234	20	20	1	3840	960	4	21.168	256	5644.8	15	16	0	4	1411.2
22.05	2048	45.1584	84.672	8	5.645	15	15	1	3840	960	4	21.168	256	5644.8	15	16	0	4	1411.2
32	32	1.024	73.728	1	1.024	72	36	2	2304	768	3	24.576	192	6144	12	12	0	4	1536
32	48	1.536	73.728	1	1.536	48	12	4	2304	768	3	24.576	192	6144	12	12	0	4	1536
32	64	2.048	73.728	1	2.048	36	18	2	2304	768	3	24.576	192	6144	12	12	0	4	1536
32	128	4.096	73.728	2	2.048	36	36	1	2304	768	3	24.576	192	6144	12	12	0	4	1536
32	192	6.144	73.728	3	2.048	36	36	1	2304	768	3	24.576	192	6144	12	12	0	4	1536
32	256	8.192	73.728	4	2.048	36	36	1	2304	768	3	24.576	192	6144	12	12	0	4	1536
32	384	12.288	73.728	6	2.048	36	36	1	2304	768	3	24.576	192	6144	12	12	0	4	1536
32	512	16.384	73.728	8	2.048	36	36	1	2304	768	3	24.576	192	6144	12	12	0	4	1536
32	768	24.576	73.728	6	4.096	18	18	1	2304	768	3	24.576	192	6144	12	12	0	4	1536
32	1024	32.768	73.728	8	4.096	18	18	1	2304	768	3	24.576	192	6144	12	12	0	4	1536
32	1152	36.864	73.728	9	4.096	18	18	1	2304	768	3	24.576	192	6144	12	12	0	4	1536
32	1536	49.152	73.728	12	4.096	18	18	1	2304	768	3	24.576	192	6144	12	12	0	4	1536
44.1	32	1.4112	84.672	1	1.411	60	30	2	1920	960	2	42.336	128	5644.8	15	8	0	4	1411.2
44.1	48	2.1168	84.672	1	2.117	40	10	4	1920	960	2	42.336	128	5644.8	15	8	0	4	1411.2
44.1	64	2.8224	84.672	1	2.822	30	15	2	1920	960	2	42.336	128	5644.8	15	8	0	4	1411.2
44.1	128	5.6448	84.672	1	5.645	15	15	1	1920	960	2	42.336	128	5644.8	15	8	0	4	1411.2
44.1	192	8.4672	84.672	2	4.234	20	20	1	1920	960	2	42.336	128	5644.8	15	8	0	4	1411.2
44.1	256	11.2896	84.672	2	5.645	15	15	1	1920	960	2	42.336	128	5644.8	15	8	0	4	1411.2
44.1	384	16.9344	84.672	3	5.645	15	15	1	1920	960	2	42.336	128	5644.8	15	8	0	4	1411.2
44.1	512	22.5792	84.672	4	5.645	15	15	1	1920	960	2	42.336	128	5644.8	15	8	0	4	1411.2
44.1	768	33.8688	84.672	6	5.645	15	15	1	1920	960	2	42.336	128	5644.8	15	8	0	4	1411.2
44.1	1024	45.1584	84.672	8	5.645	15	15	1	1920	960	2	42.336	128	5644.8	15	8	0	4	1411.2
48	32	1.536	73.728	1	1.536	48	24	2	1536	768	2	36.864	128	6144	12	8	0	4	1536
48	48	2.304	73.728	1	2.304	32	8	4	1536	768	2	36.864	128	6144	12	8	0	4	1536
48	64	3.072	73.728	1	3.072	24	12	2	1536	768	2	36.864	128	6144	12	8	0	4	1536
48	128	6.144	73.728	2	3.072	24	24	1	1536	768	2	36.864	128	6144	12	8	0	4	1536
48	192	9.216	73.728	3	3.072	24	24	1	1536	768	2	36.864	128	6144	12	8	0	4	1536
48	256	12.288	73.728	4	3.072	24	24	1	1536	768	2	36.864	128	6144	12	8	0	4	1536
48	384	18.432	73.728	6	3.072	24	24	1	1536	768	2	36.864	128	6144	12	8	0	4	1536
48	512	24.576	73.728	4	6.144	12	12	1	1536	768	2	36.864	128	6144	12	8	0	4	1536
48	768	36.864	73.728	6	6.144	12	12	1	1536	768	2	36.864	128	6144	12	8	0	4	1536

Table 51. Recommended Clock Divider Settings for PLL as Master Clock (VCOM Mode) (continued)

f_S (kHz)	RSCK	SCK (MHz)	PLL VCO (MHz)	P	PLL REF (MHz)	M = K*R	K = J.D	R	PLL f_S	DSP f_S	NMAC	DSP CLK (MHz)	MOD f_S	MOD f (kHz)	NDAC	DOSR	% Error	NCP	CP f (kHz)
48	1024	49.152	73.728	8	6.144	12	12	1	1536	768	2	36.864	128	6144	12	8	0	4	1536
96	32	3.072	73.728	2	1.536	48	24	2	768	384	2	36.864	64	6144	12	4	0	4	1536
96	48	4.608	73.728	3	1.536	48	24	2	768	384	2	36.864	64	6144	12	4	0	4	1536
96	64	6.144	73.728	2	3.072	24	12	2	768	384	2	36.864	64	6144	12	4	0	4	1536
96	128	12.288	73.728	4	3.072	24	24	1	768	384	2	36.864	64	6144	12	4	0	4	1536
96	192	18.432	73.728	6	3.072	24	24	1	768	384	2	36.864	64	6144	12	4	0	4	1536
96	256	24.576	73.728	8	3.072	24	24	1	768	384	2	36.864	64	6144	12	4	0	4	1536
96	384	36.864	73.728	6	6.144	12	12	1	768	384	2	36.864	64	6144	12	4	0	4	1536
96	512	49.152	73.728	8	6.144	12	12	1	768	384	2	36.864	64	6144	12	4	0	4	1536
192	32	6.144	73.728	2	3.072	24	12	2	384	192	2	36.864	32	6144	12	2	0	4	1536
192	48	9.216	73.728	3	3.072	24	12	2	384	192	2	36.864	32	6144	12	2	0	4	1536
192	64	12.288	73.728	4	3.072	24	12	2	384	192	2	36.864	32	6144	12	2	0	4	1536
192	128	24.576	73.728	8	3.072	24	24	1	384	192	2	36.864	32	6144	12	2	0	4	1536
192	192	36.864	73.728	6	6.144	12	12	1	384	192	2	36.864	32	6144	12	2	0	4	1536
192	256	49.152	73.728	8	6.144	12	12	1	384	192	2	36.864	32	6144	12	2	0	4	1536
384	32	12.288	73.728	2	6.144	12	6	2	192	96	2	36.864	16	6144	12	1	0	4	1536
384	48	18.432	73.728	3	6.144	12	6	2	192	96	2	36.864	16	6144	12	1	0	4	1536
384	64	24.576	73.728	4	6.144	12	6	2	192	96	2	36.864	16	6144	12	1	0	4	1536
384	128	49.152	73.728	8	6.144	12	12	1	192	96	2	36.864	16	6144	12	1	0	4	1536

Table 52. Recommended Clock Divider Settings for SCK as Master Clock

f_S (kHz)	RSCK	SCK (MHz)	DSP f_S	NMAC	DSP CLK (MHz)	MOD f_S	MOD f (kHz)	NDAC	DOSR	NCP	CP f (kHz)
8	256	2.048	256	1	2.048	256	2048	1	16	2	1024
8	384	3.072	384	1	3.072	384	3072	1	24	2	1536
8	512	4.096	512	1	4.096	512	4096	1	32	2	2048
8	768	6.144	768	1	6.144	768	6144	1	48	4	1536
8	1024	8.192	1024	1	8.192	512	4096	2	32	2	2048
8	1152	9.216	1152	1	9.216	576	4608	2	36	4	1152
8	1536	12.288	1536	1	12.288	768	6144	2	48	4	1536
8	2048	16.384	2048	1	16.384	512	4096	4	32	2	2048
8	3072	24.576	3072	1	24.576	768	6144	4	48	4	1536
11.025	256	2.8224	256	1	2.822	256	2822.4	1	16	2	1411.2
11.025	384	4.2336	384	1	4.234	384	4233.6	1	24	4	1058.4
11.025	1152	12.7008	1152	1	12.701	384	4233.6	3	24	4	1058.4
11.025	1536	16.9344	1536	1	16.934	512	5644.8	3	32	4	1411.2
11.025	2048	22.5792	2048	1	22.579	512	5644.8	4	32	4	1411.2
11.025	3072	33.8688	3072	1	33.869	512	5644.8	6	32	4	1411.2
16	256	4.096	256	1	4.096	256	4096	1	16	2	2048
16	384	6.144	384	1	6.144	384	6144	1	24	4	1536
16	512	8.192	512	1	8.192	256	4096	2	16	2	2048
16	768	12.288	768	1	12.288	384	6144	2	24	4	1536
16	1152	18.432	1152	1	18.432	288	4608	4	18	4	1152
16	1536	24.576	1536	1	24.576	384	6144	4	24	4	1536
16	2048	32.768	2048	1	32.768	256	4096	8	16	2	2048
16	3072	49.152	3072	1	49.152	384	6144	8	24	4	1536
22.05	256	5.6448	256	1	5.645	256	5644.8	1	16	4	1411.2
22.05	384	8.4672	384	1	8.467	192	4233.6	2	12	4	1058.4
22.05	512	11.2896	512	1	11.29	256	5644.8	2	16	4	1411.2
22.05	768	16.9344	768	1	16.934	256	5644.8	3	16	4	1411.2
22.05	1024	22.5792	1024	1	22.579	256	5644.8	4	16	4	1411.2
22.05	1152	25.4016	1152	1	25.402	192	4233.6	6	12	4	1058.4
22.05	1536	33.8688	1536	1	33.869	256	5644.8	6	16	4	1411.2
22.05	2048	45.1584	2048	1	45.158	256	5644.8	8	16	4	1411.2
32	256	8.192	256	1	8.192	128	4096	2	8	2	2048
32	384	12.288	384	1	12.288	128	4096	3	8	2	2048
32	512	16.384	512	1	16.384	128	4096	4	8	2	2048
32	768	24.576	768	1	24.576	128	4096	6	8	2	2048
32	1024	32.768	1024	1	32.768	128	4096	8	8	2	2048
32	1152	36.864	1152	1	36.864	128	4096	9	8	4	1024
32	1536	49.152	1536	1	49.152	128	4096	12	8	4	1024
44.1	256	11.2896	256	1	11.29	128	5644.8	2	8	4	1411.2
44.1	384	16.9344	384	1	16.934	128	5644.8	3	8	4	1411.2
44.1	512	22.5792	512	1	22.579	128	5644.8	4	8	4	1411.2
44.1	768	33.8688	768	1	33.869	128	5644.8	6	8	4	1411.2
44.1	1024	45.1584	1024	1	45.158	128	5644.8	8	8	4	1411.2
48	256	12.288	256	1	12.288	128	6144	2	8	4	1536
48	384	18.432	384	1	18.432	128	6144	3	8	4	1536
48	512	24.576	512	1	24.576	128	6144	4	8	4	1536
48	768	36.864	768	1	36.864	128	6144	6	8	4	1536
48	1024	49.152	1024	1	49.152	128	6144	8	8	4	1536
96	192	18.432	192	1	18.432	48	4608	4	3	6	768
96	256	24.576	256	1	24.576	64	6144	4	4	4	1536
96	384	36.864	384	1	36.864	64	6144	6	4	4	1536
96	512	49.152	512	1	49.152	64	6144	8	4	4	1536

Table 52. Recommended Clock Divider Settings for SCK as Master Clock (continued)

f_S (kHz)	RSCK	SCK (MHz)	DSP f_S	NMAC	DSP CLK (MHz)	MOD f_S	MOD f (kHz)	NDAC	DOSR	NCP	CP f (kHz)
192	128	24.576	128	1	24.576	32	6144	4	2	4	1536
192	192	36.864	192	1	36.864	32	6144	6	2	4	1536
192	256	49.152	256	1	49.152	32	6144	8	2	4	1536
384	64	24.576	64	1	24.576	16	6144	4	1	4	1536
384	128	49.152	128	1	49.152	16	6144	8	1	4	1536

13 Device and Documentation Support

13.1 Community Resources

E2E™ Audio Converters Forum TI

E2E Community

13.2 Trademarks

System Two Cascade, Audio Precision are trademarks of Audio Precision.
DirectPath is a trademark of Texas, Instruments, Inc..
All other trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, see the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCM5242RHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-25 to 85	PCM5242	Samples
PCM5242RHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	PCM5242	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

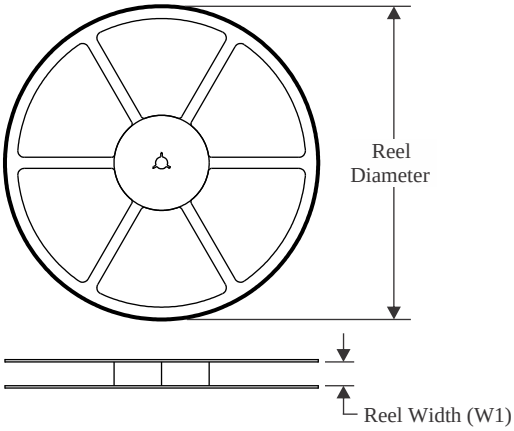
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

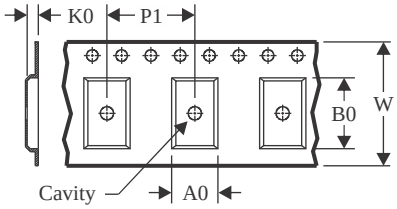
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

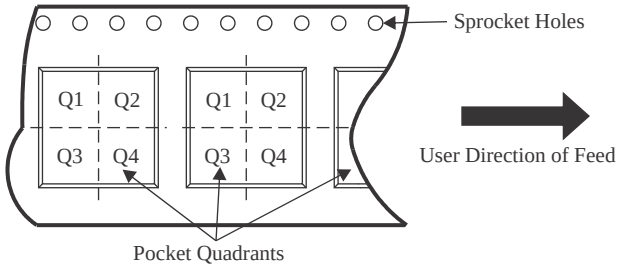


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

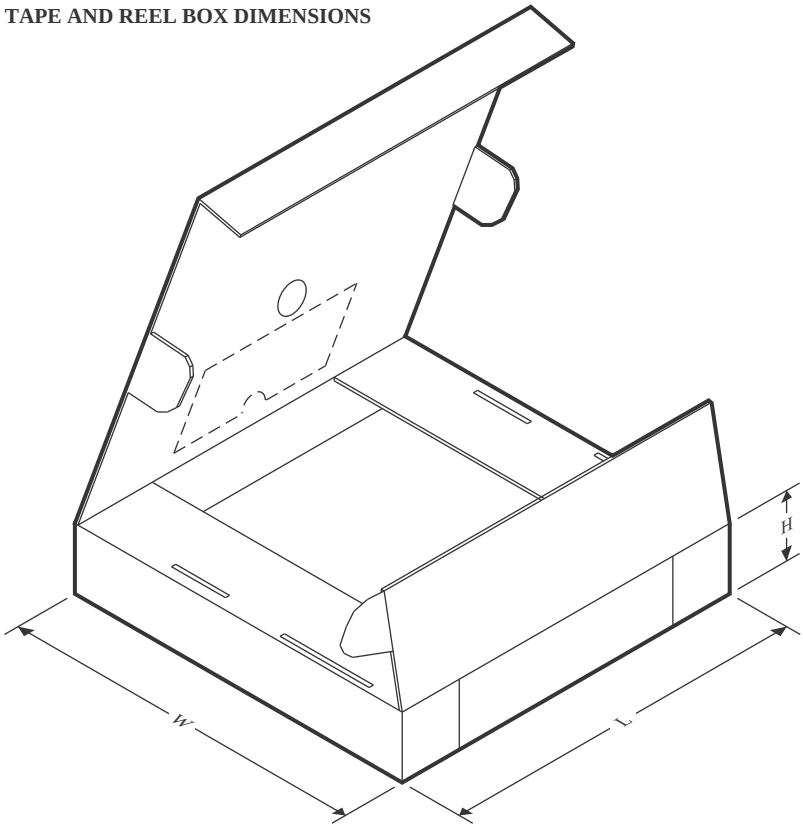
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM5242RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
PCM5242RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM5242RHBR	VQFN	RHB	32	3000	346.0	346.0	33.0
PCM5242RHBT	VQFN	RHB	32	250	210.0	185.0	35.0

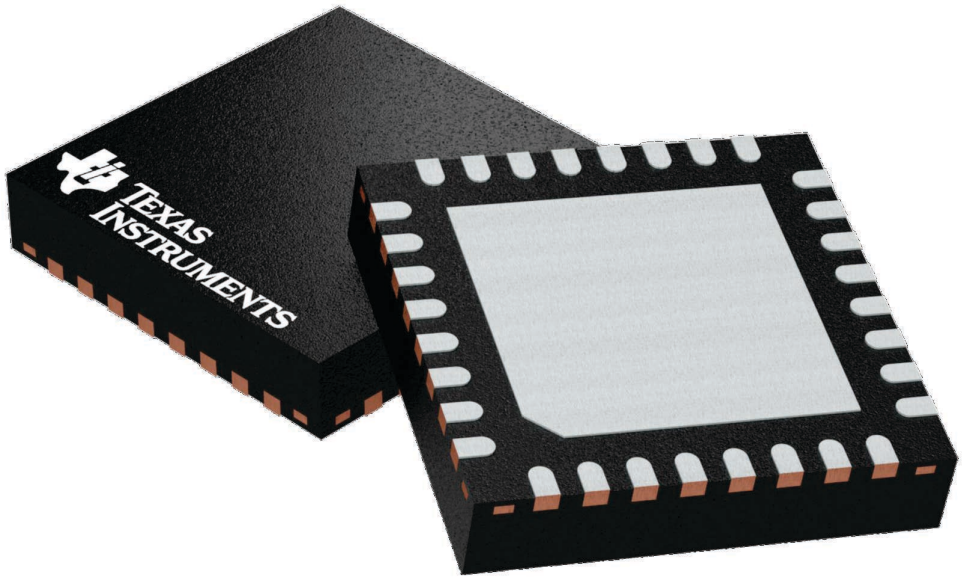
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

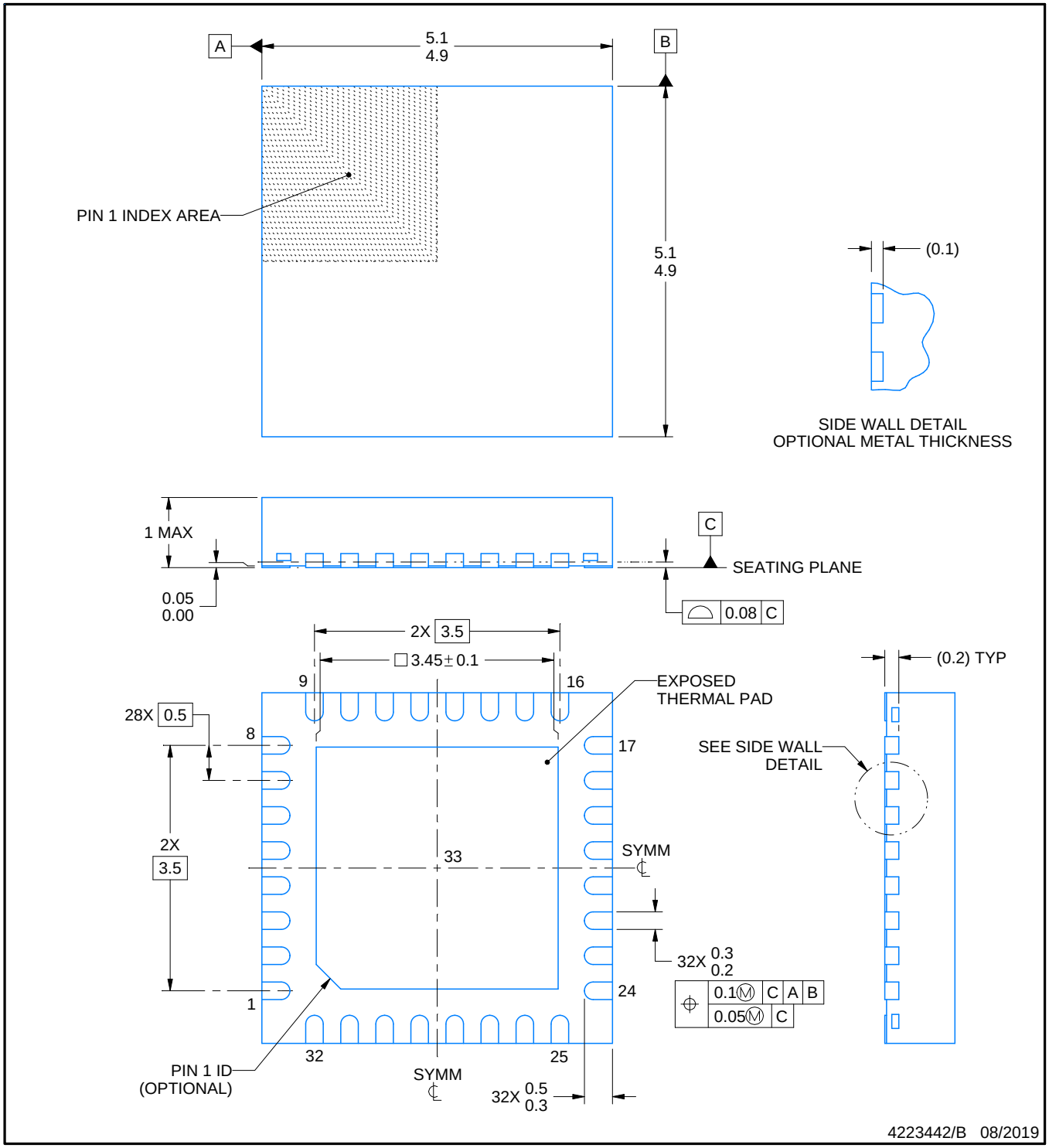
4224745/A

RHB0032E

PACKAGE OUTLINE

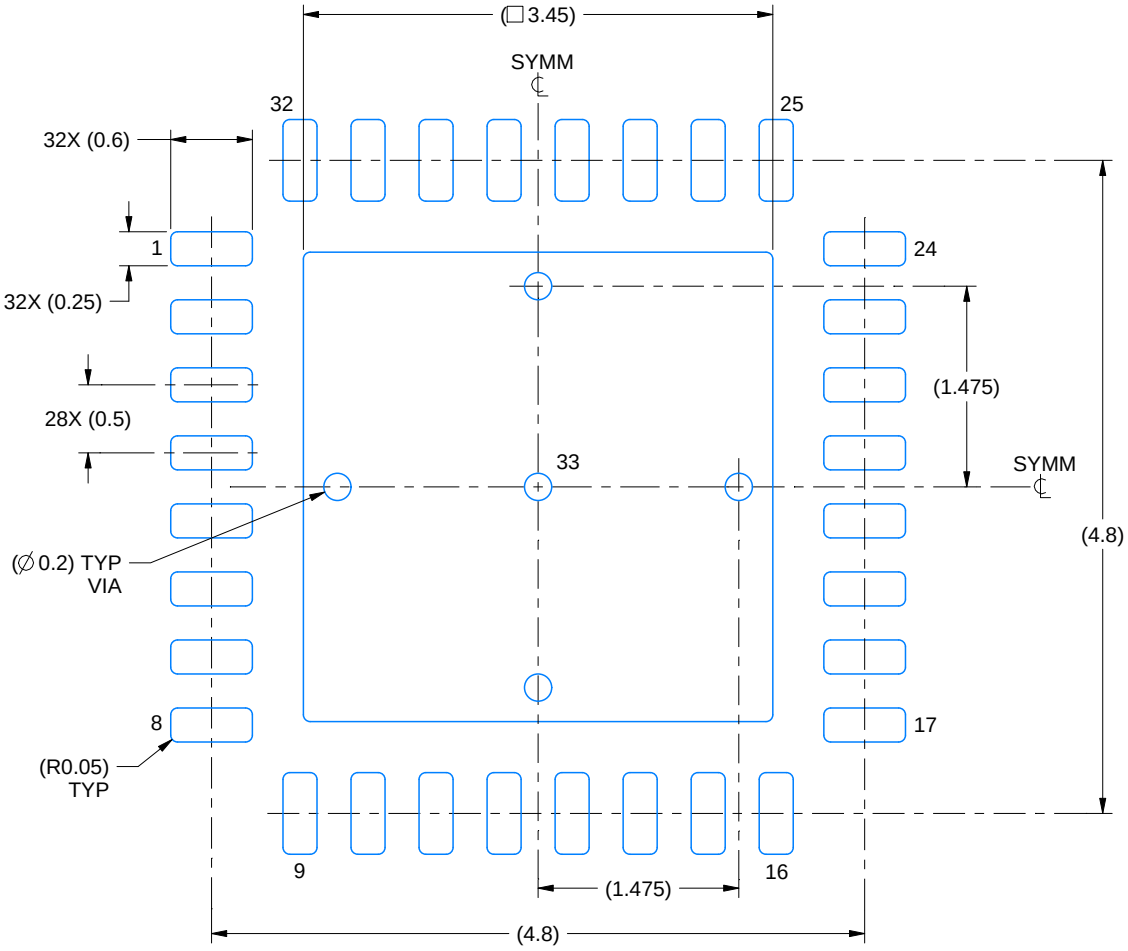
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

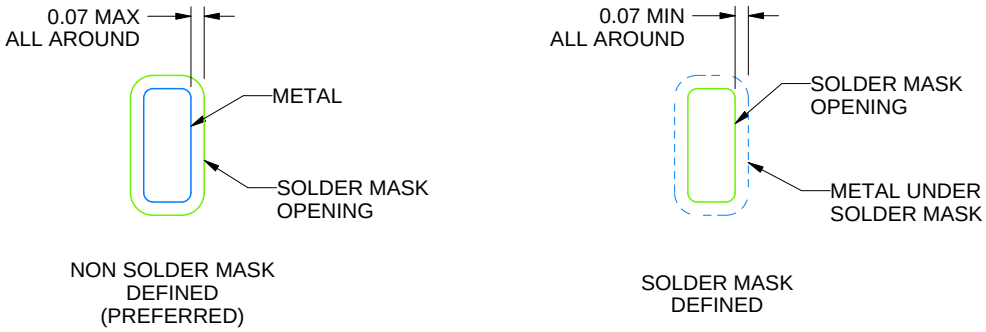


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

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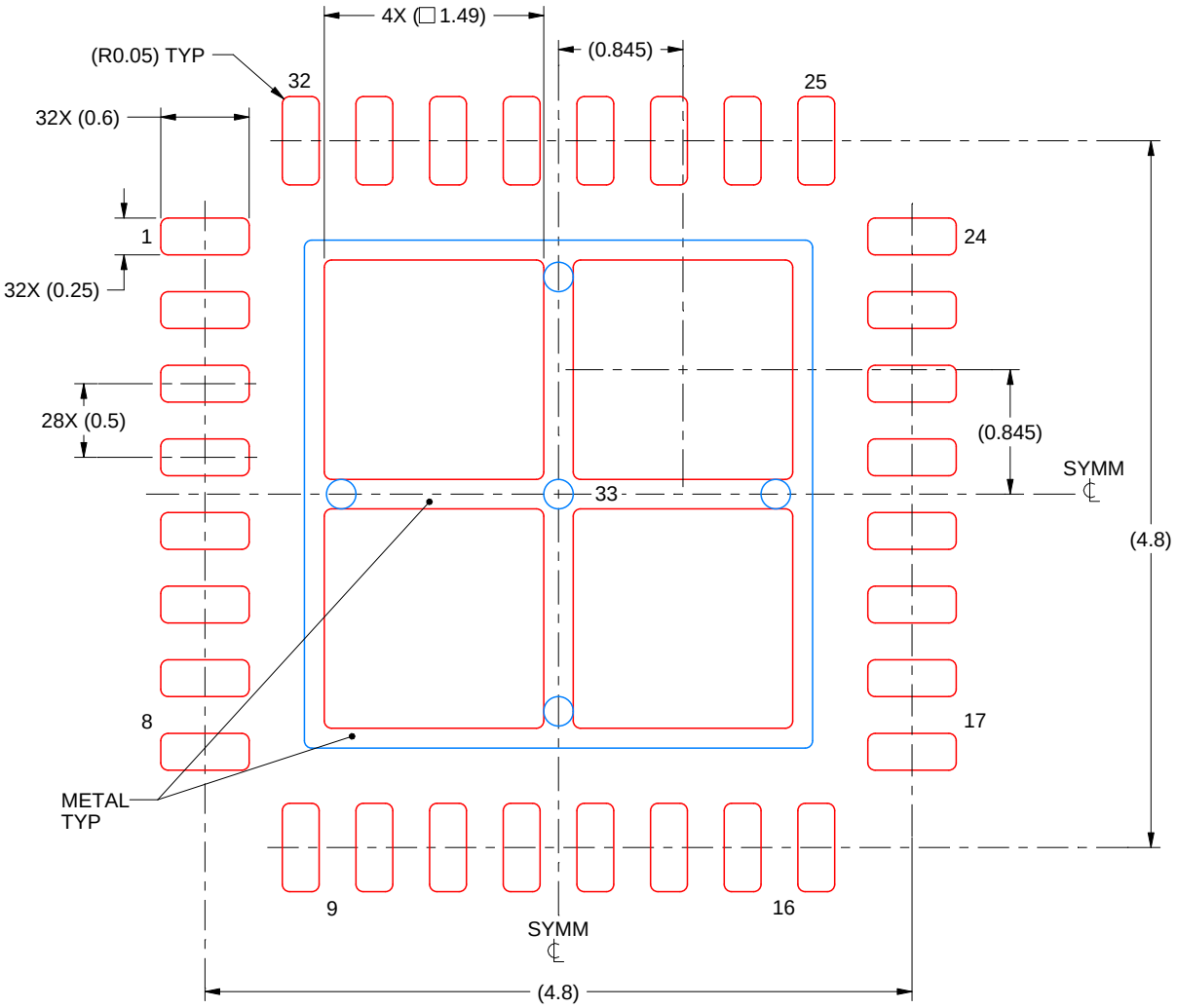
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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