

100-W STEREO DIGITAL AMPLIFIER POWER STAGE CONTROLLER

FEATURES

- Stereo H-Bridge Controller
- Efficiency > 95%[†]
- 2x100 W (RMS) at 6 Ω (BTL)[†]
- THD+N < 0.15% (Typical at 100 W at 6 Ω, 1 kHz)[‡]
- Half-Bridge Independent Control
- Glueless Interface to TAS50XX Digital Audio PWM Processors
- 3.3-V Digital Interface
- Fault Detection
 - Overcurrent
 - Overtemperature
 - Undervoltage Protection for External MOSFETs
- Low Profile 56-Terminal TSSOP SMD Package

- Power Amplifiers
- Home Theater
- Subwoofer Driver

DESCRIPTION

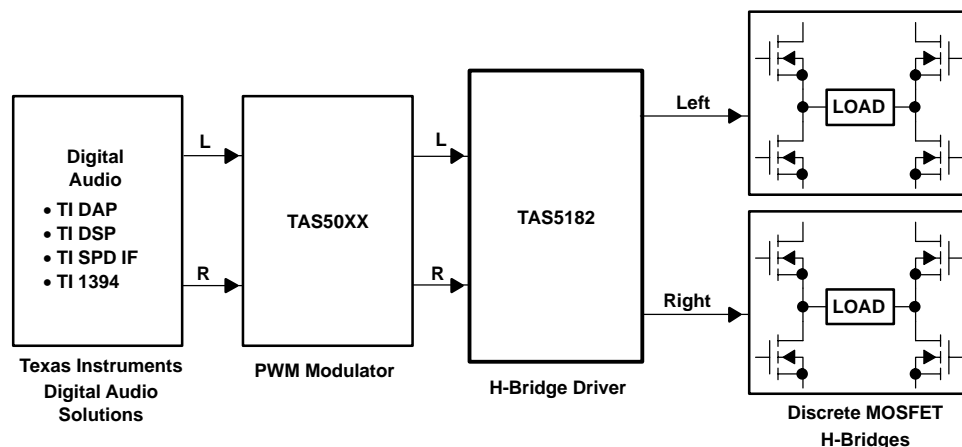
The TAS5182 device is a high-performance, stereo digital amplifier power stage controller. It is designed to drive two discrete bridge-tied-load (BTL) MOSFET output stages at up to 100 W per channel at 6 Ω. The TAS5182 device, incorporating Texas Instrument's PurePath™ technology, is used in conjunction with a digital audio PWM processor (TAS50XX) and two discrete MOSFET H-bridges (4 MOSFETs per H-Bridge) to deliver high-power, true digital audio amplification. The efficiency of this digital amplifier can be greater than 95%, reducing the size of both the power supplies and heat sinks needed. The TAS5182 device accepts a stereo PWM 3.3-V input, and it controls the switching of the discrete H-bridges.

Overcurrent, overtemperature, and undervoltage protections are built into the TAS5182 device, safeguarding the H-bridge and speakers against output short-circuit conditions, overtemperature conditions, and other fault conditions that could damage the system.

APPLICATIONS

- AV Receivers
- High Power DVD Receivers

Typical Stereo Audio System Using TAS5182 H-Bridge Driver



[†] When using appropriate MOSFETs.

[‡] When using recommended design.



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TAS5182

SLES045E - JUNE 2002 - REVISED MAY 2004

ORDERING INFORMATION

| T _A | PACKAGE |
|----------------|-------------|
| 0°C to 70°C | TAS5182DCA |
| -40°C to 85°C | TAS5182IDCA |



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (T_A) unless otherwise noted⁽¹⁾

| | | TAS5182 |
|------------------------------------------------------------------------|--------------------------------------|------------------------------------|
| Supply voltage range | GV _{DD} to GV _{SS} | -0.3 V to 15 V |
| | DV _{DD} to DV _{SS} | -0.3 V to 3.6 V |
| AP, AM, BP, BM, CP, CM, DP, DM | | -0.3 V to DV _{DD} + 0.3 V |
| RESET, SHUTDOWN | | -0.3 V to DV _{DD} + 0.3 V |
| BST_A, BST_B, BST_C, BST_D to GV _{SS} for pulse width <100 ns | | 63 V |
| Switching frequency | | 1500 kHz |
| Operating junction temperature range, T _J | | 150°C |
| Storage temperature range, T _{stg} | | -65°C to 150°C |

⁽¹⁾ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

| | | MIN | NOM | MAX | UNIT |
|-------------------------------------------|--------------------------------------|-----|-----|------|------|
| Supply voltage range | GV _{DD} to GV _{SS} | 9 | 12 | 12.6 | V |
| | DV _{DD} to DV _{SS} | 3 | 3.3 | 3.6 | V |
| High-side bootstrap supply voltage range | BST_A, BST_B, BST_C, BST_D | | 50 | 52.6 | V |
| High-side drain connection voltage range | DHS_A, DHS_B, DHS_C, DHS_D | | 40 | 42 | V |
| High-side source connection voltage range | SHS_A, SHS_B, SHS_C, SHS_D | | 40 | 42 | V |

ELECTRICAL CHARACTERISTICS

 $T_C = 25^\circ\text{C}$, $DV_{DD} = 3.3\text{ V}$, $GV_{DD} = 12\text{ V}$, Frequency = 384 kHz

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------------------------------------------------------------|------------------------------------------|------------------------------|------|-----|------------|
| INPUT TERMINALS: AM, AP, BM, BP, CM, CP, DM, DP | | | | | |
| V_{IH} | High input voltage | 2 | | | V |
| V_{IL} | Low input voltage | | | 0.8 | V |
| R_I | Input resistance | | 50 | | k Ω |
| R_{dtp} | Dead time resistor range | 0 | | 100 | k Ω |
| INPUT TERMINAL: RESET_X | | | | | |
| $V_{IH}(\text{RESET})$ | High input voltage | 2 | | | V |
| $V_{IL}(\text{RESET})$ | Low input voltage | | | 0.8 | V |
| GATE DRIVE OUTPUT: GHS_A, GHS_B, GHS_C, GHS_D, GLS_A, GLS_B, GLS_C, GLS_D | | | | | |
| I_{oso} | Source current, peak | $V_O = 2\text{ V}$ | -1.2 | | A |
| I_{osi} | Sink current, peak | $V_O = 8\text{ V}$ | 1.6 | | A |
| BST DIODE | | | | | |
| V_d | Forward current voltage drop | $I_d = 100\text{ mA}$ | 2 | | V |
| SUPPLY CURRENTS | | | | | |
| I_{DVDD} | Operating supply current | No load on gate drive output | 3 | | mA |
| I_{DVDDQ} | Quiescent supply current | No switching | 3 | | mA |
| I_{GVDD} | Operating supply current | No load on gate drive output | 15 | | mA |
| I_{GVDDQ} | Quiescent supply current | No switching | 2 | | mA |
| VOLTAGE PROTECTION | | | | | |
| $V_{uvp,G}$ | Undervoltage protection limit, GV_{DD} | | | 8.3 | V |

SWITCHING CHARACTERISTICS

 $T_C = 25^\circ\text{C}$, $DV_{DD} = 3.3\text{ V}$, $GV_{DD} = 12\text{ V}$

| PARAMETER | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|----------------------------------------|----------------------------------------------------------|--------------------------------|-----|------|------|
| TIMING, OUTPUT TERMINALS | | | | | |
| f_{op} | Operating frequency | | | 1500 | kHz |
| $t_{pd}(\text{if-O})$ | Positive input falling to GHS_x falling | $C_L = 1\text{ nF}$ | 45 | | ns |
| $t_{pd}(\text{ir-O})$ | Positive input rising to GLS_x falling | $C_L = 1\text{ nF}$ | 45 | | ns |
| t_{dtp} | Dead time programming range ⁽¹⁾ | $R_{dtp} = 100\text{ k}\Omega$ | | 110 | ns |
| $t_r(\text{GD})$ | Rise time, gate drive output (0.5 to 3 V) | $C_L = 1\text{ nF}$ | 4.5 | | ns |
| $t_f(\text{GD})$ | Fall time, gate drive output (9 to 3 V) | $C_L = 1\text{ nF}$ | 7 | | ns |
| TIMING, PROTECTION, AND CONTROL | | | | | |
| $t_{pd}(\text{R-SD})$ | Delay, $\overline{\text{RESET}}$ low to SHUTDOWN high | | 40 | | ns |
| $t_{pd}(\text{R-LH})$ | Delay, $\overline{\text{RESET}}$ low to GLS_x high | | 44 | | ns |
| $t_{pd}(\text{R-OP})$ | Delay, $\overline{\text{RESET}}$ high to operation state | | 50 | | ns |
| $t_{pd}(\text{E-L})$ | Delay, error event to all gates low | | 180 | | ns |
| $t_{pd}(\text{E-SD})$ | Delay, error event to SHUTDOWN low | | 170 | | ns |

⁽¹⁾ Dead time programming definition: Adjustable delay from AP (BP, CP, or DP) rising edge to GHS_A (GHS_B, GHS_C, or GHS_D) rising edge, and AM (BM, CM, or DM) rising edge to GLS_A (GLS_B, GLS_C, or GLS_D) rising edge.

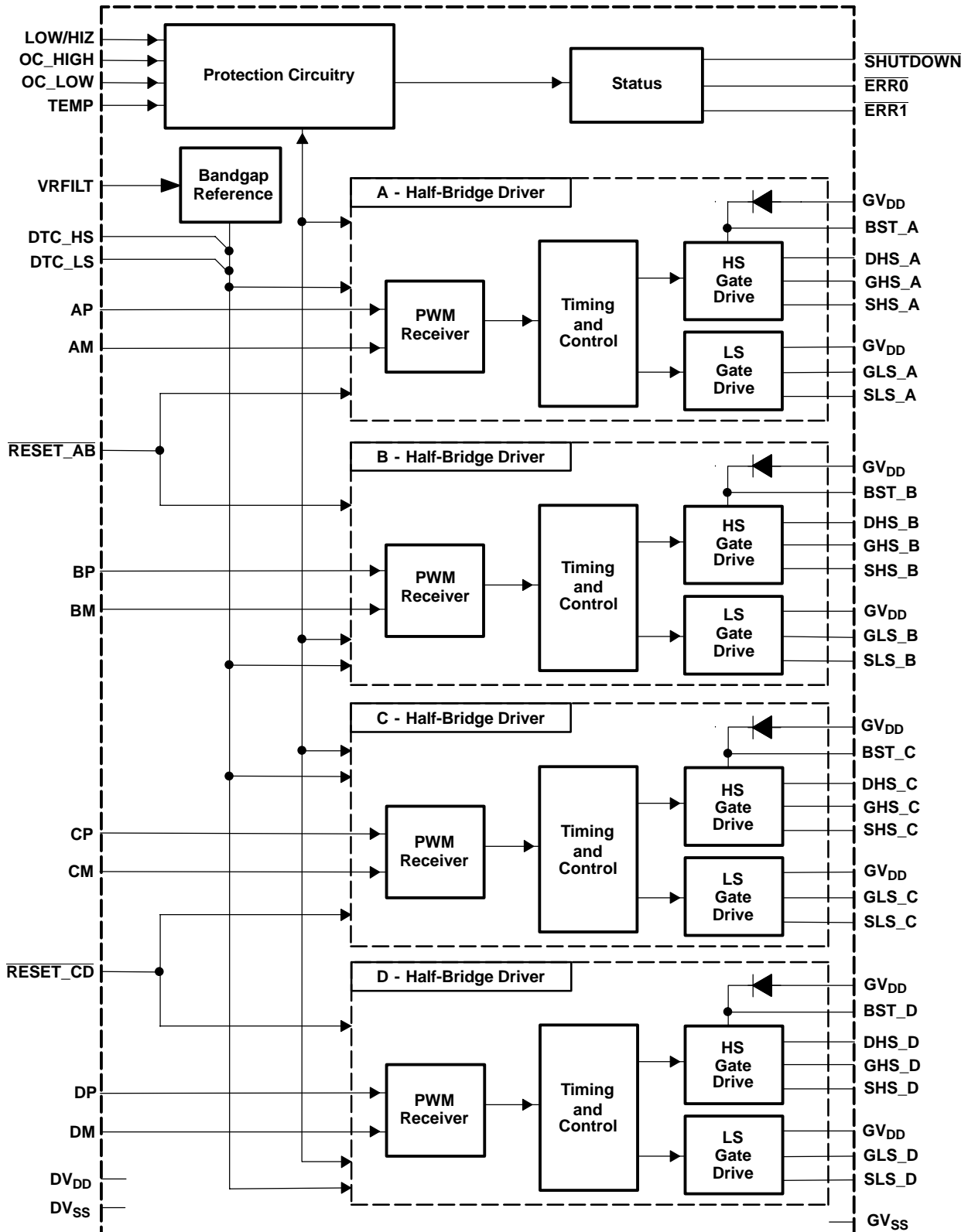
Terminal Functions (continued)

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|------------------------|--------------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DHS_A | 49 | I | High-side drain connection, used for high-side V_{DS} sensing |
| DHS_B | 43 | I | High-side drain connection, used for high-side V_{DS} sensing |
| DHS_C | 37 | I | High-side drain connection, used for high-side V_{DS} sensing |
| DHS_D | 31 | I | High-side drain connection, used for high-side V_{DS} sensing |
| DTC_HS | 6 | I | High-side dead-time programming, external resistor to DV_{SS} required |
| DTC_LS | 7 | I | Low-side dead-time programming, external resistor to DV_{SS} required |
| DV_{DD} | 3 | P | Logic supply voltage |
| DV_{SS} | 4, 24 | P | Digital ground, reference for input signals |
| $\overline{ERR0}$ | 21 | O | Logic output, signals chip operation mode/state. This output is open drain with internal pullup resistor. |
| $\overline{ERR1}$ | 22 | O | Logic output, signals chip operation mode/state. This output is open drain with internal pullup resistor. |
| GHS_A | 51 | O | Gate drive output for high-side MOSFET, half-bridge A |
| GHS_B | 45 | O | Gate drive output for high-side MOSFET, half-bridge B |
| GHS_C | 39 | O | Gate drive output for high-side MOSFET, half-bridge C |
| GHS_D | 33 | O | Gate drive output for high-side MOSFET, half-bridge D |
| GLS_A | 54 | O | Gate drive output for low-side MOSFET, half-bridge A |
| GLS_B | 48 | O | Gate drive output for low-side MOSFET, half-bridge B |
| GLS_C | 42 | O | Gate drive output for low-side MOSFET, half-bridge C |
| GLS_D | 36 | O | Gate drive output for low-side MOSFET, half-bridge D |
| GV_{DD} | 30, 55 | P | Gate drive voltage supply terminal |
| GV_{SS} | 29, 56 | P | Gate drive voltage supply ground return |
| LOW/HIZ | 23 | I | Logic signal that determines the drive output state during a reset. When $\overline{RESET_AB}$ or $\overline{RESET_CD}$ is low, LOW/HIZ = 1 indicates that the outputs are low impedance LOW/HIZ = 0 indicates that the outputs are high impedance |
| NC | 1, 2, 5, 25, 26 | | Not connected. Terminals 1, 2, 5, 25, and 26 may be connected to DV_{SS} . |
| OC_HIGH | 8 | I | High-side overcurrent trip value programming. OC configuration circuit (see Figure 5) is required. |
| OC_LOW | 27 | I | Low-side overcurrent trip value programming. OC configuration circuit (see Figure 5) is required. |
| $\overline{RESET_AB}$ | 12 | I | Reset signal half-bridge A and B, active low |
| $\overline{RESET_CD}$ | 17 | I | Reset signal half-bridge C and D, active low |
| SHUTDOWN | 20 | O | Error/warning report indicator. This output is open drain with internal pull-up resistor. |
| SHS_A | 52 | I | High-side source connection, used as BST floating ground (and high-side V_{DS} sensing) |
| SHS_B | 46 | I | High-side source connection, used as BST floating ground (and high-side V_{DS} sensing) |
| SHS_C | 40 | I | High-side source connection, used as BST floating ground (and high-side V_{DS} sensing) |
| SHS_D | 34 | I | High-side source connection, used as BST floating ground (and high-side V_{DS} sensing) |
| SLS_A | 53 | I | Source connection low-side MOSFET, ground return terminal, half-bridge A |
| SLS_B | 47 | I | Source connection low-side MOSFET, ground return terminal, half-bridge B |
| SLS_C | 41 | I | Source connection low-side MOSFET, ground return terminal, half-bridge C |
| SLS_D | 35 | I | Source connection low-side MOSFET, ground return terminal, half-bridge D |
| TEMP | 28 | I | External temperature sensing connection |
| VRFILT | 9 | I | Bandgap reference = 1.8 V. Capacitor must be connected from VRFILT to DV_{SS} . |

TAS5182

SLES045E - JUNE 2002 - REVISED MAY 2004

FUNCTIONAL BLOCK DIAGRAM



TIMING DIAGRAMS

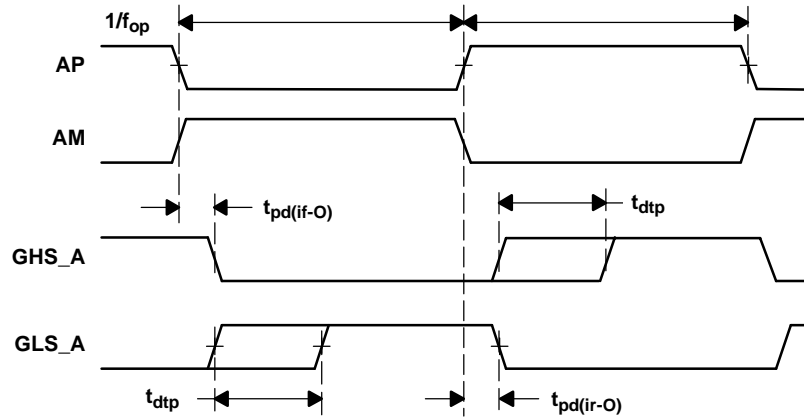


Figure 1. PWM Input to Gate Drive Output Timing (Same for A, B, C, and D Half-Bridge Drivers)

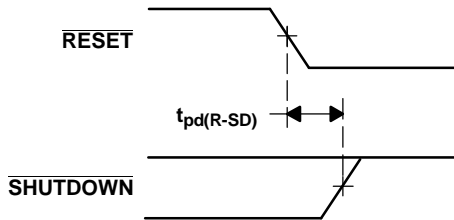


Figure 2. RESET to SHUTDOWN Propagation Delay

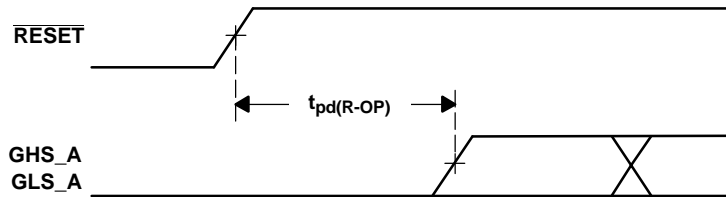
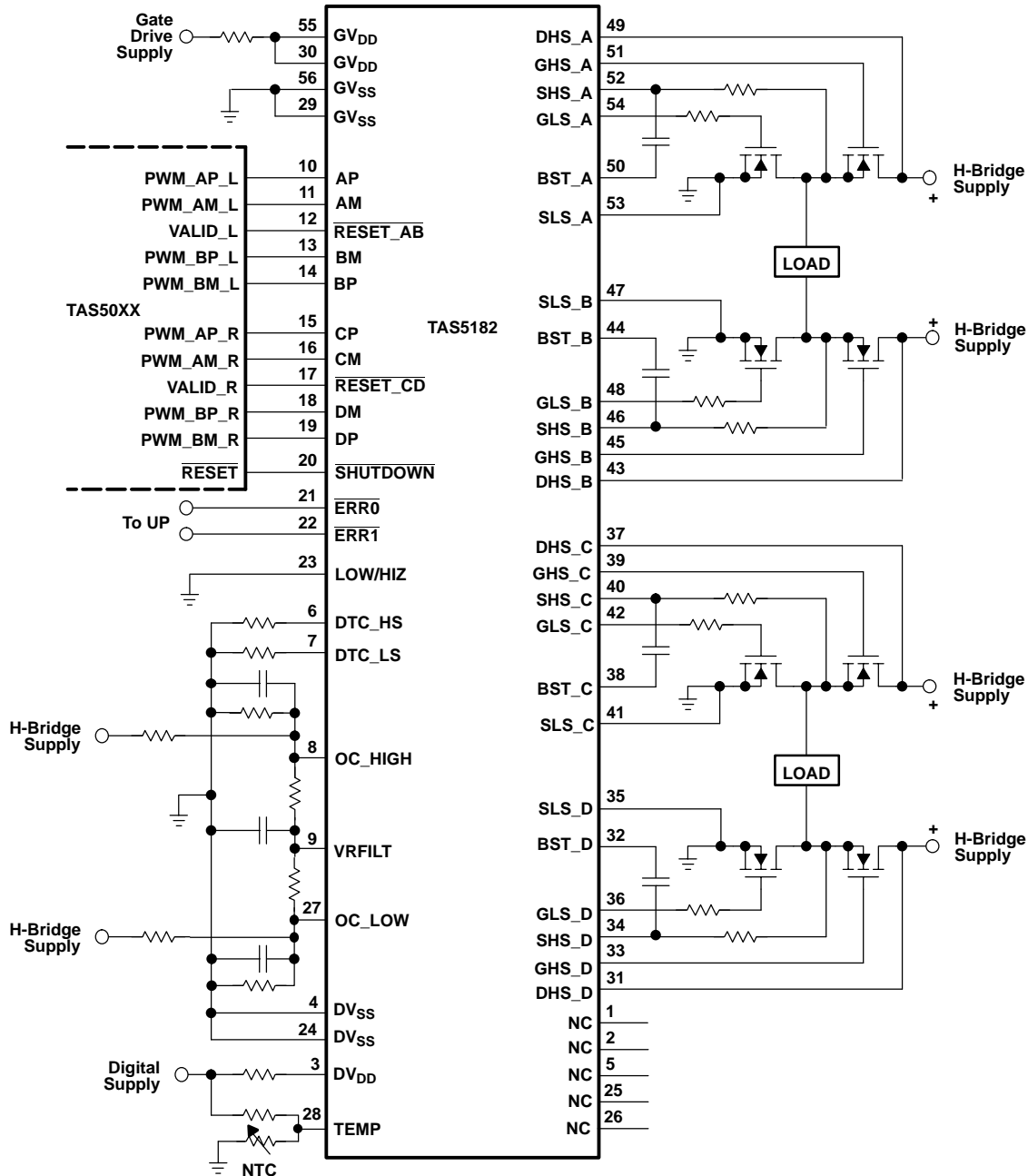


Figure 3. RESET to Gate Drive Output Propagation Delay (Same for Half-Bridge A, B, C, and D)

TAS5182

SLES045E - JUNE 2002 - REVISED MAY 2004

SIMPLIFIED APPLICATION CONNECTION DIAGRAM (BRIDGE-TIED-LOAD CONFIGURATION)



NOTE: Recommended power MOSFETs
International Rectifier IRFIZ24N (8 places)
For complete reference schematics contact Texas Instruments.

FUNCTIONAL DESCRIPTION

Power Stage Protection

The TAS5182 device provides overcurrent, overtemperature, and undervoltage protection for the MOSFET power stage.

Overcurrent Protection (OCP)

To protect the power stage from damage due to high currents, a V_{DS} sensing system is implemented in the TAS5182 device. Based on $R_{DS(on)}$ of the power MOSFETs and the maximum allowed I_{DS} , a voltage threshold can be calculated which, when exceeded, triggers the protection latch, causing the $\overline{SHUTDOWN}$ terminal to go low. This voltage threshold is resistor programmable. See the *Calculation of Overcurrent Resistor Values* section for more details.

Overtemperature Protection (OTP)

The TAS5182 device has a temperature protection system that uses an external negative temperature coefficient (NTC) resistor as a temperature sensor. See the *Overtemperature Programming Circuit* section for implementation details.

Undervoltage Protection (UVP)

To protect the power output stage during start-up, shutdown, and other possible undervoltage conditions, the TAS5182 device provides power stage undervoltage protection by driving its outputs low whenever GV_{DD} is under 7 V. With the TAS5182 outputs driven low, the MOSFETs go to a high-impedance state.

Control Terminals

The TAS5182 device provides input control terminals to reset each audio channel and also to control the electrical characteristics of the MOSFET output power stage.

Channel Reset

The reset function enables operation after power up, re-enables operation after an error event, and disables the MOSFET output stage switching during power down and mute. The falling edge of $\overline{RESET_AB}$ (left audio channel) or $\overline{RESET_CD}$ (right audio channel) causes the TAS5182 device to reset. The rising edge of $\overline{RESET_AB}$ or $\overline{RESET_CD}$ causes the TAS5182 device to clear the error latch and resume normal operation.

MOSFET Output Reset Control

The LOW/HIZ control terminal selects whether the MOSFET output stage goes into a high-impedance (HI-Z) state or LOW-LOW state when $\overline{RESET_AB}$ or $\overline{RESET_CD}$ is enabled. In the high-impedance state, the low-side and high-side MOSFETs are turned off causing no current flow through the MOSFETs. This effectively disconnects the load from the power supply rail. In the LOW-LOW state, the low-side MOSFETs are turned on, while the high-side MOSFETs are turned off. This causes a low or ground signal to be output to the load.

Status Terminals

The TAS5182 device provides output status terminals to report overcurrent, overtemperature, and undervoltage warnings and errors.

Shutdown Indicator

The $\overline{SHUTDOWN}$ terminal indicates an error event has occurred such as overcurrent, overtemperature, or undervoltage. The $\overline{SHUTDOWN}$ terminal is pulled high when $\overline{RESET_AB}$ or $\overline{RESET_CD}$ is asserted. $\overline{ERR0}$ and $\overline{ERR1}$ terminals along with the $\overline{SHUTDOWN}$ terminal indicate the type of warnings and errors. Note that $\overline{SHUTDOWN}$ is an open-drain signal. See Table 1 for a functional description of these signals.

Table 1. TAS5182 Status Signals

| ERR0 | ERR1 | SHUTDOWN | DESCRIPTION |
|------|------|----------|------------------------------------------------------------------------------|
| 0 | 0 | 0 | Multiple errors (TAS5182 gate outputs low, MOSFET outputs HI-Z) |
| 0 | 0 | 1 | Not valid |
| 0 | 1 | 0 | Overtemperature error (TAS5182 gate outputs low, MOSFET outputs HI-Z) |
| 0 | 1 | 1 | Overtemperature warning (normal operation) |
| 1 | 0 | 0 | Overcurrent error (TAS5182 gate outputs low, MOSFET outputs HI-Z) |
| 1 | 0 | 1 | Not valid |
| 1 | 1 | 0 | GV_{DD} undervoltage error (TAS5182 gate outputs low, MOSFET outputs HI-Z) |
| 1 | 1 | 1 | Normal operation |

TAS5182 Power Up and Reset

After power up, all gate drive outputs are held low (i.e., the error latch is set). Normal operation can be initiated by toggling $\overline{\text{RESET_AB}}$ and/or $\overline{\text{RESET_CD}}$ from a low state to a high state. If no errors are present, then the TAS5182 device is ready to accept audio inputs.

TAS5182 Reset and Error Timing

The TAS5182 device provides two output control configurations for reset and error situations. In a BTL system configuration, the MOSFET outputs must be grounded before resuming normal operation. This enables the bootstrap capacitors to charge.

Reset and Error Timing (BTL System)

When using this device in the BTL configuration, it is advisable to bring the MOSFET outputs to a high impedance state when reset ($\overline{\text{RESET_AB}}$ or $\overline{\text{RESET_CD}}$)

is asserted. Figure 4 shows the timing that occurs in this configuration. This feature is enabled by connecting the LOW/HIZ terminal to DV_{SS}.

When an error event occurs (see Table 1) and following propagation delay $t_{pd(E-SD)}$, the TAS5182 device pulls the $\overline{\text{SHUTDOWN}}$ signal low. The falling edge of $\overline{\text{SHUTDOWN}}$ forces the MOSFET outputs into a high-impedance state. The $\overline{\text{SHUTDOWN}}$ signal is usually connected to the $\overline{\text{RESET}}$ terminal of the TAS50XX PWM controller. After some delay, the controller then asserts the TAS5182 $\overline{\text{RESET_AB}}$ and $\overline{\text{RESET_CD}}$ terminals low. The falling edge of $\overline{\text{RESET}}$ forces the MOSFET outputs to ground potential (this event also brings the $\overline{\text{SHUTDOWN}}$ signal high). This allows the bootstrap capacitors to charge through the grounded MOSFET outputs. When $\overline{\text{RESET}}$ is pulled high, the system resumes normal operation.

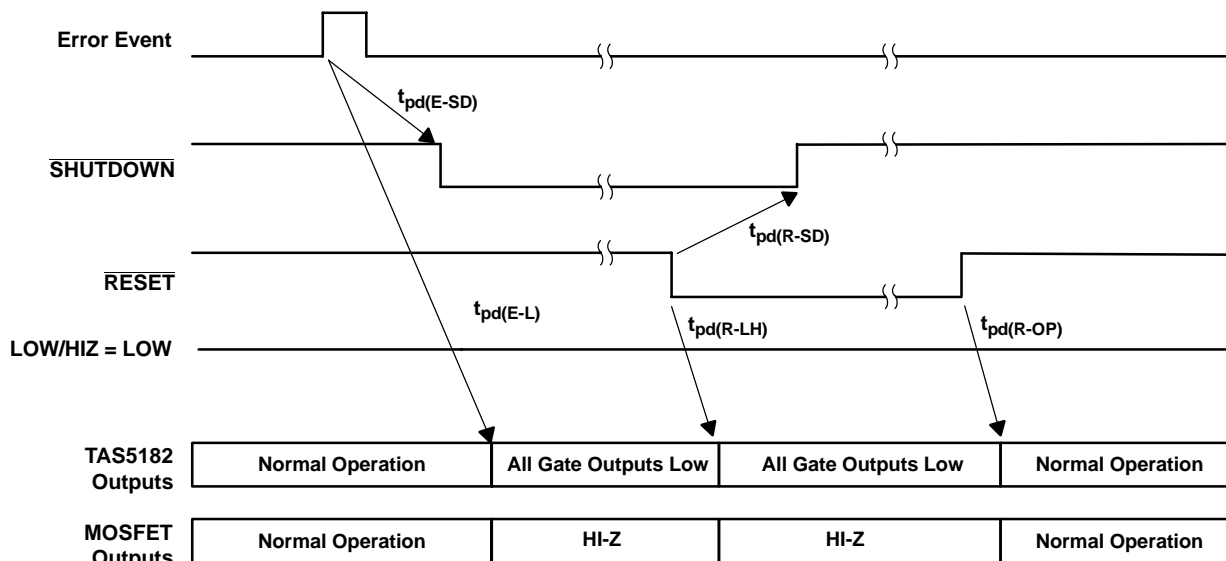


Figure 4. Reset and Error Timing (BTL System)

Overcurrent Configuration From Circuit

The output current flows through internal resistance $R_{DS(on)}$ of the external MOSFETs, which creates voltage drop V_{DS} . The overcurrent detector senses this voltage to trigger an error event. The exact current limit depends on parasitics from the PCB layout, resistance of the MOSFET at the operation temperature, and the configuration of the H-bridge output stage.

See Table 2 for the OCL and OCH reference voltages. Figure 5 shows the recommended overcurrent configuration circuit.

Table 2. OCL and OCH Reference Voltages (Overcurrent Configuration Circuit)

| | VOLTAGE | OUTPUT INDUCTOR SHUTDOWN CURRENT RANGE ⁽¹⁾ |
|-----|---------------------|-------------------------------------------------------|
| OCL | 0.7 V (terminal 27) | 12-19 A |
| OCH | 1.17 V (terminal 8) | 14-24 A |

⁽¹⁾ Measured on Texas Instruments reference board TAS5182C6REF.

Board configuration:

- 1R0 resistors on SHS and GLS connections
- $GV_{DD} = 12\text{ V}$, $PV_{DD} = 40\text{ V}$
- 10BQ060 voltage clamp on output node
- TT snubbers: $L = 75\text{ nH}$, $C = 10\text{ nF}$, $R = 5.4\ \Omega$

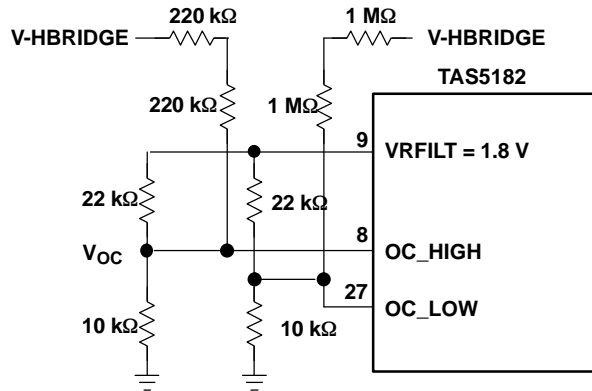


Figure 5. Overcurrent Configuration Circuit

Overtemperature Programming Circuit

The TAS5182 device features a temperature protection system that uses an external negative temperature coefficient (NTC) resistor as a temperature sensor. Figure 6 shows a typical application.

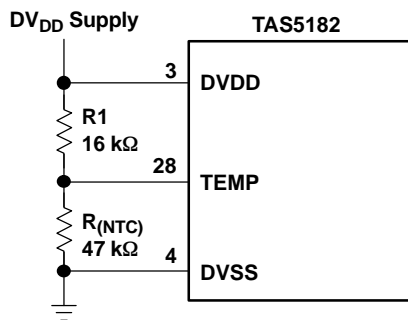


Figure 6. Temperature Sensing Circuit

The temperature protection system has two trigger limits: OT warning and OT error. OT warning occurs when the voltage at the TEMP terminal is approximately 36% of

DV_{DD} . OT error occurs when the voltage at the TEMP terminal is approximately 23% of DV_{DD} . OT warning is decoded when $\overline{ERR0} = 0$, $\overline{ERR1} = 1$, and $\overline{SHUTDOWN} = 1$. OT error is decoded when $\overline{ERR0} = 0$, $\overline{ERR1} = 1$, and $\overline{SHUTDOWN} = 0$. The user for a particular application determines the values of $R1$ and R_{NTC} . Typical values are $R1 = 16\text{ k}\Omega$ and $R_{NTC} = 47\text{ k}\Omega$.

THERMAL INFORMATION

The thermally enhanced DCA package is based on the 56-pin HTSSOP, but includes a thermal pad (see Figure 7) to provide an effective thermal contact between the IC and the PCB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO-220 type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, have two shortcomings: they do not address the low profile requirements ($< 2\text{ mm}$) of many of today's advanced systems and they do not offer a terminal count high enough to accommodate increasing integration. However, traditional low-power, surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits

The PowerPAD™ package (thermally enhanced HTSSOP) combines fine-pitch, surface-mount technology with thermal performance comparable to much larger power packages.

The PowerPAD package is designed to optimize the heat transfer to the PCB. Because of the small size and limited mass of a HTSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a patented lead-frame design and manufacturing technique to provide a direct connection to the heat-generating IC. When this pad is soldered to the PCB, good power dissipation in the ultrathin, fine-pitch, surface-mount package can be reliably achieved. See Reference 4 for recommended soldering procedure.

THERMAL DATA

| PARAMETER | | MIN | TYP | MAX | UNIT |
|-----------------------------------|-----------------------------------|-------|-----|-----|----------------------|
| Junction temperature, $T_{J(SD)}$ | | | | 150 | $^{\circ}\text{C}$ |
| Operating temperature, T_C | Commercial | 0 | 25 | 70 | $^{\circ}\text{C}$ |
| | Industrial | -40 | 25 | 85 | $^{\circ}\text{C}$ |
| Thermal resistance, θ_{jc} | Pad with solder ⁽¹⁾ | 0.27 | | | $^{\circ}\text{C/W}$ |
| Thermal resistance, θ_{ja} | | 21.17 | | | $^{\circ}\text{C/W}$ |
| Thermal resistance, θ_{jc} | Pad without solder ⁽¹⁾ | 0.27 | | | $^{\circ}\text{C/W}$ |
| Thermal resistance, θ_{ja} | | 36.42 | | | $^{\circ}\text{C/W}$ |

(1) Values taken from Table 6 *Thermal Characteristics for Different Package and PCB Configurations* of the *PowerPAD Thermally Enhanced Package* application note (SLMA002). See pages 32 and 33 for a description of the printed circuit board (PCB) used for these measurements. Note that the PCB used for these measurements is not the recommended PCB for TAS5182 applications but is cited here for reference only.

Power Dissipation

The equation for TAS5182 power dissipation using N external MOSFETs is:

$$P_d = V_{gd} \times Q_g \times f \times N$$

where:

$$V_{gd} = GV_{DD} \text{ (typically 12 V)}$$

$$Q_g = \text{MOSFET gate charge}$$

f = operating frequency

N = number of external MOSFETs driven (eight for two-channel operation)

Example power dissipation calculation:

Given a TAS5182 system with eight external IRFIZ24N MOSFETs and $GV_{DD} = 12 \text{ V}$. The power dissipation is:

$$P_d = V_{gd} \times Q_g \times f \times N = 12\text{V} \times 22.5\text{nC} \times 384 \text{ kHz} \times 8 = 0.8 \text{ W}$$

Note: Lab measurements yield a power dissipation of 0.8 W ($PV_{DD} = 40 \text{ V}$).

REFERENCES

1. *TAS5000 Digital Audio PWM Process data manual*, Texas Instruments Literature Number SLAS270
2. *System Design Considerations for True Digital Audio Power Amplifiers*, Texas Instruments Literature Number SLAA117
3. *Digital Audio Measurements*, Texas Instruments Literature Number SLAA114
4. *PowerPAD Thermally Enhanced Package*, Texas Instruments Literature Number SLMA002

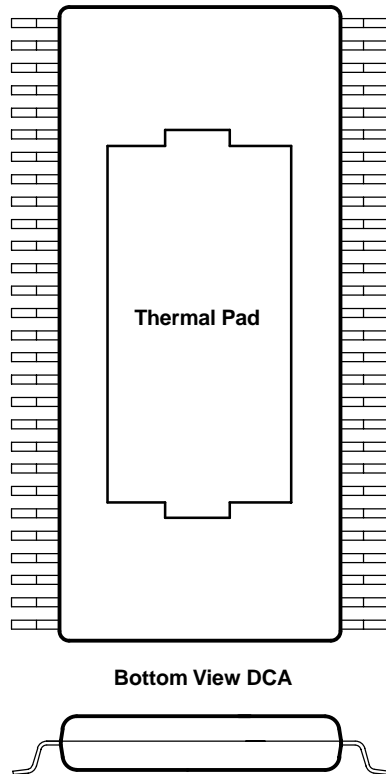
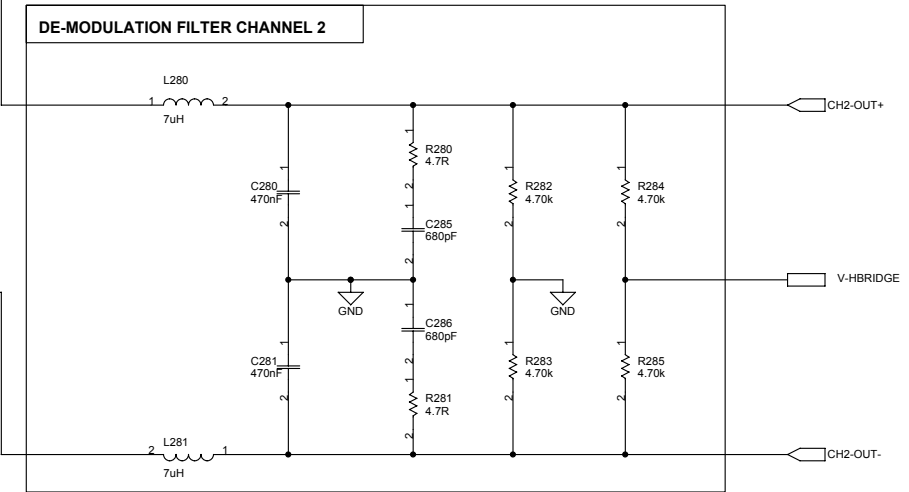
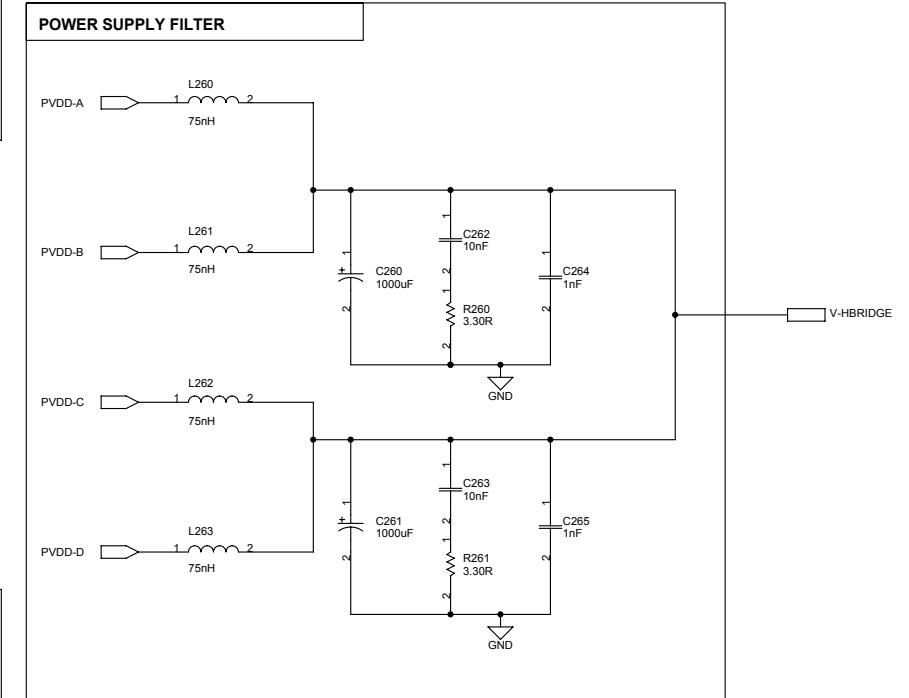
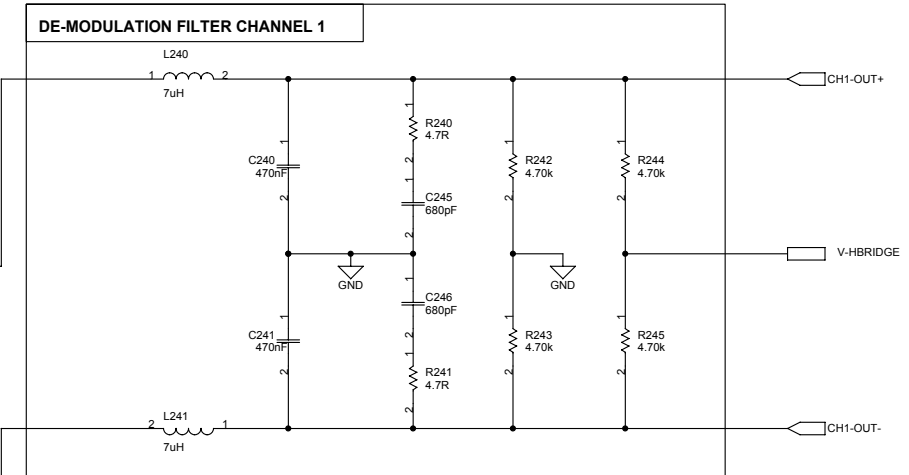
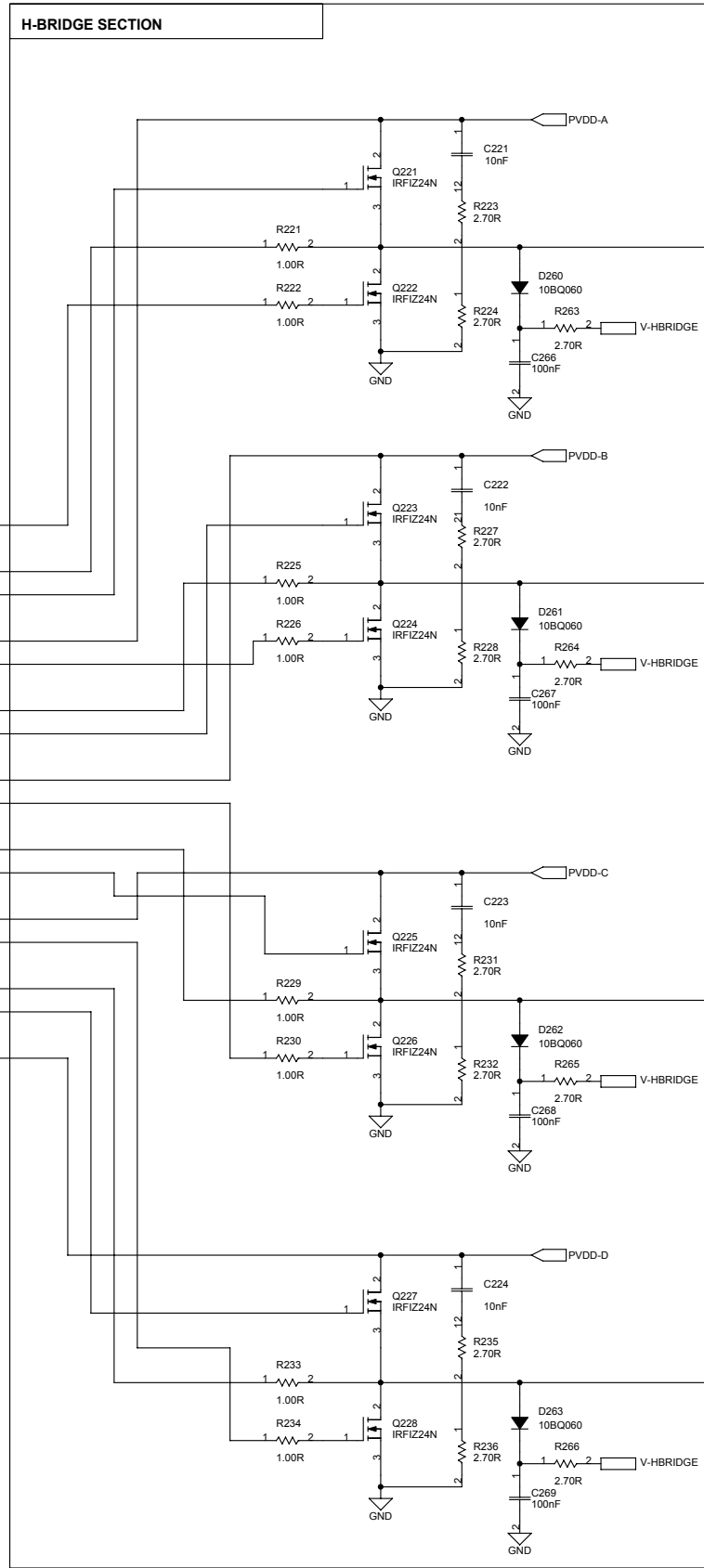
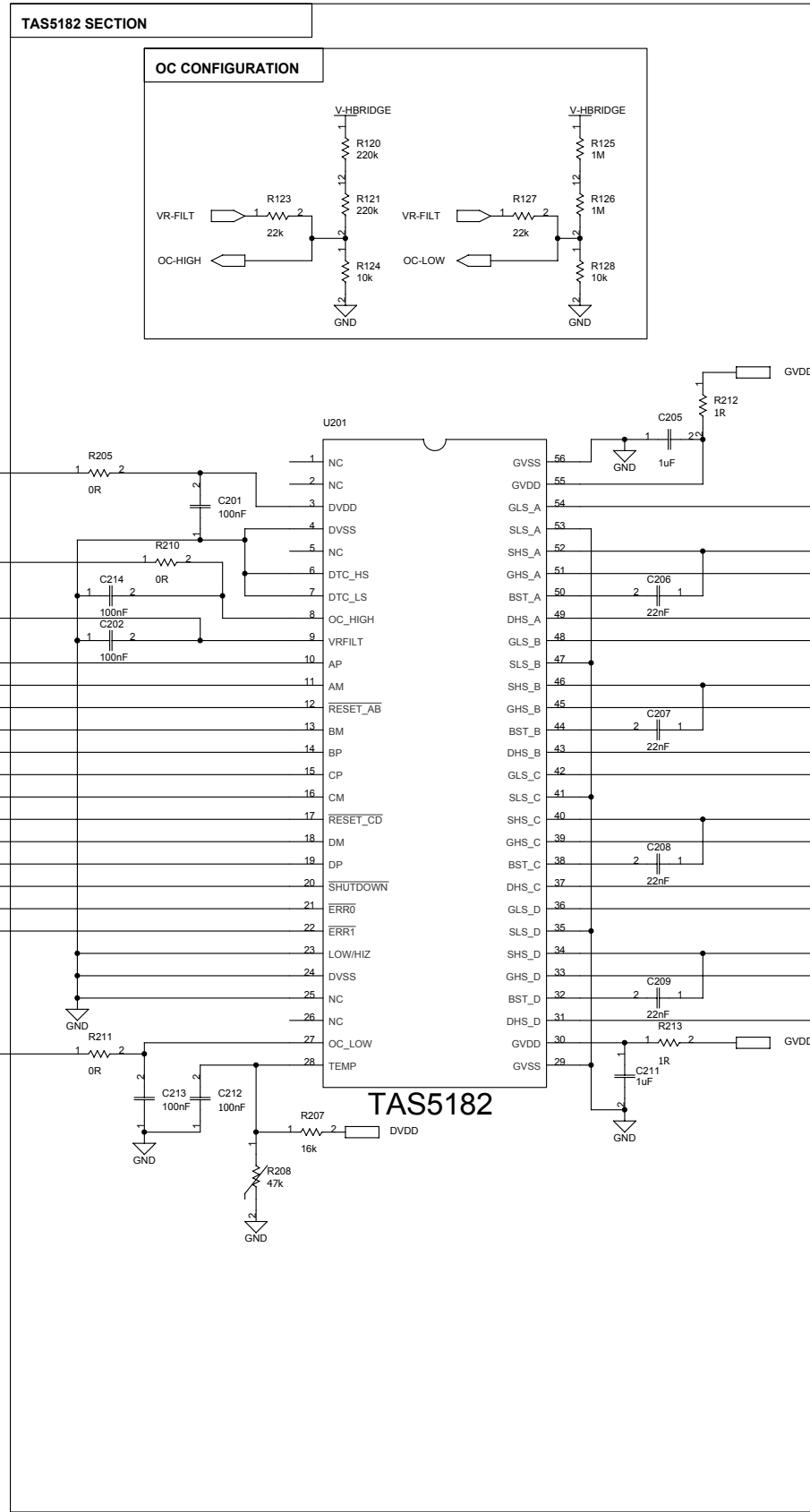


Figure 7. Views of a Thermally Enhanced DCA Package

TAS5182 OUTPUT STAGE

To/From Texas Instruments TAS5036 PWM Modulator



| | | | |
|---------------------------------------|-----------|--------------------------------|--|
| TI | | DIGITAL AUDIO & VIDEO DIVISION | |
| ALL RIGHTS RESERVED - PATENTS PENDING | | | |
| TEXAS INSTRUMENTS INCORPORATED | | | |
| Project: TAS5182C8REF | Rev: 6.00 | | |
| Page Title: CHANNEL 1 & CHANNEL 2 | Size: | | |
| File Name: | Engineer: | | |
| Date: | Page: of | | |

Patents pending in circuitry design and layout (WO99/59241 & WO99/59242).
This circuitry may only be used together with the integrated circuit TAS5100/TAS5110/TAS5111/TAS5112/TAS5182 from Texas Instruments Incorporated.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TAS5182DCA | ACTIVE | HTSSOP | DCA | 56 | 35 | Green (RoHS & no Sb/Br) | NIPDAU | Level-3-260C-168 HR | 0 to 70 | TAS5182 | Samples |
| TAS5182IDCA | ACTIVE | HTSSOP | DCA | 56 | 35 | Green (RoHS & no Sb/Br) | NIPDAU | Level-3-260C-168 HR | -40 to 85 | TAS5182I | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

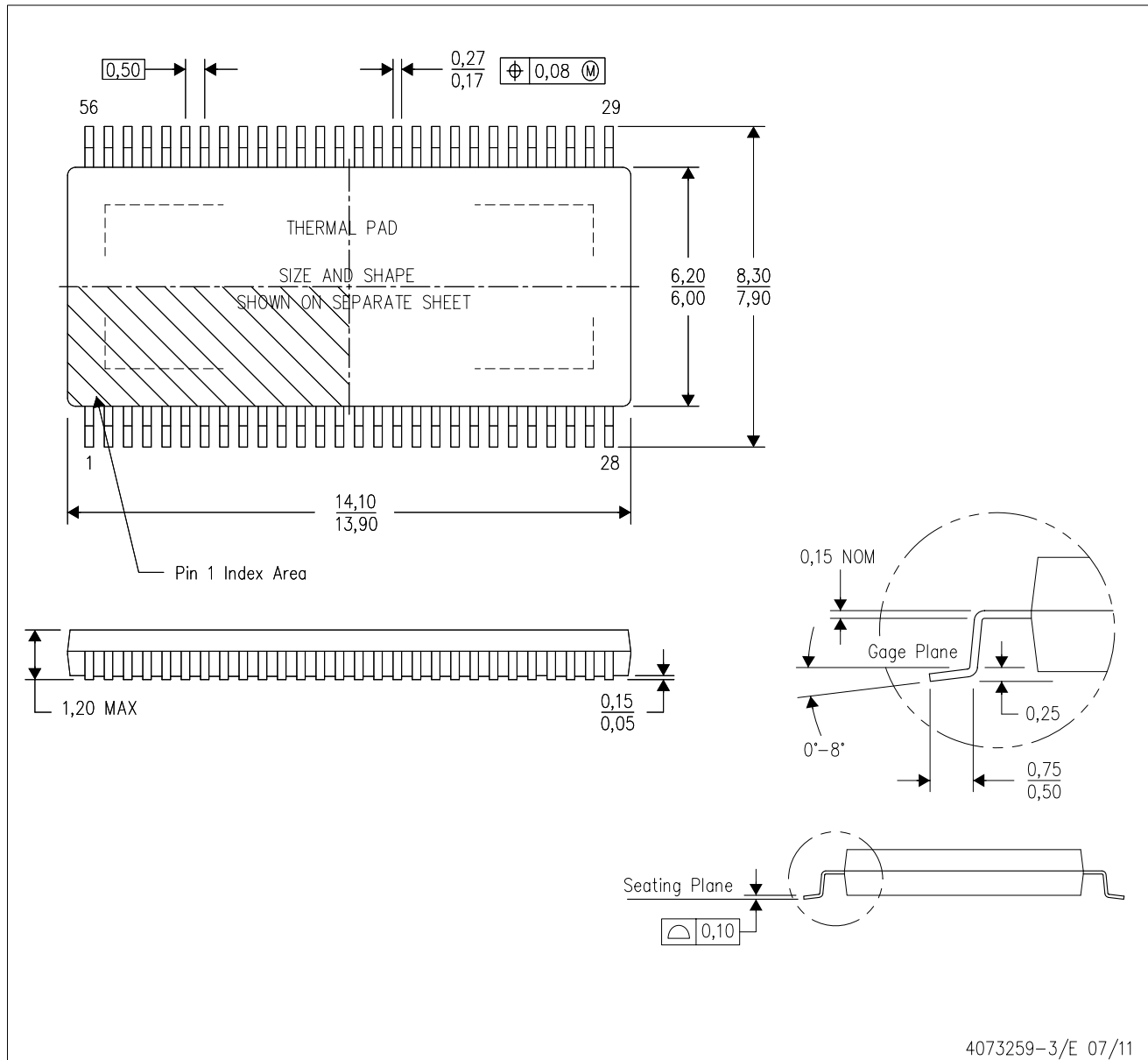
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MECHANICAL DATA

DCA (R-PDSO-G56)

PowerPAD™ PLASTIC SMALL-OUTLINE



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

DCA (R-PDSO-G56)

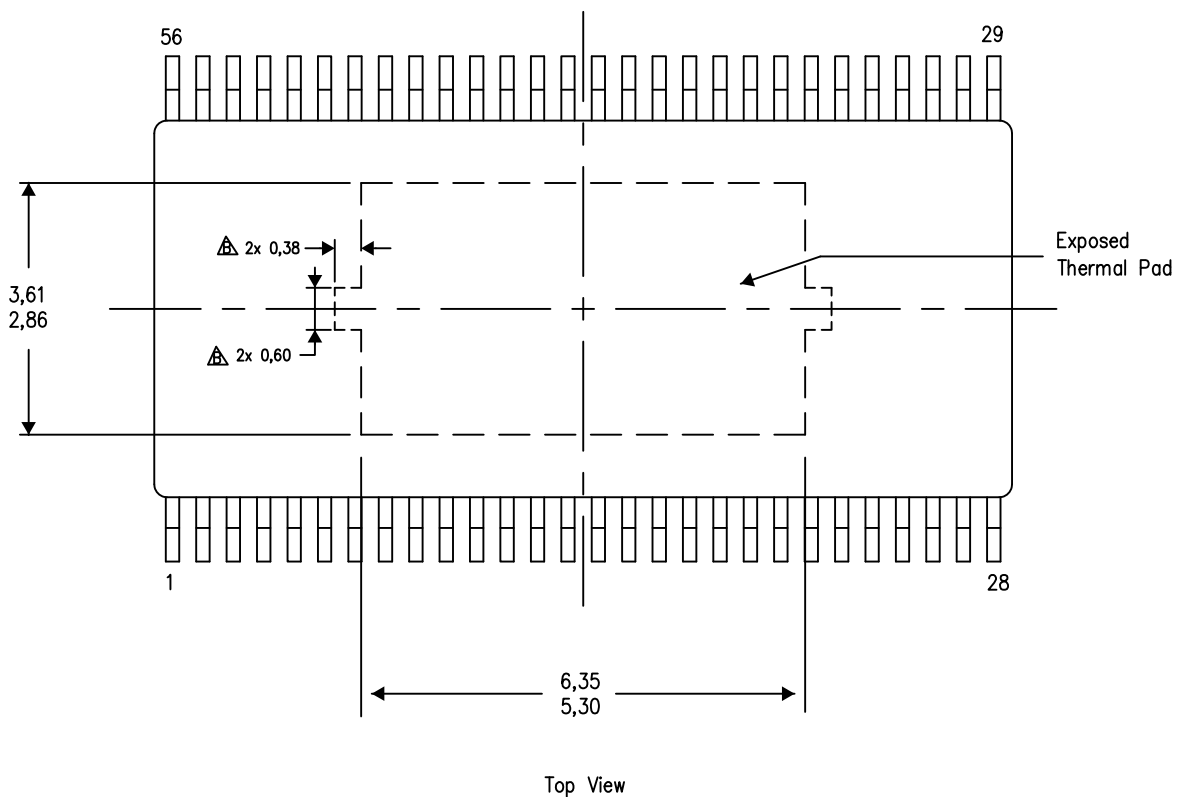
PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



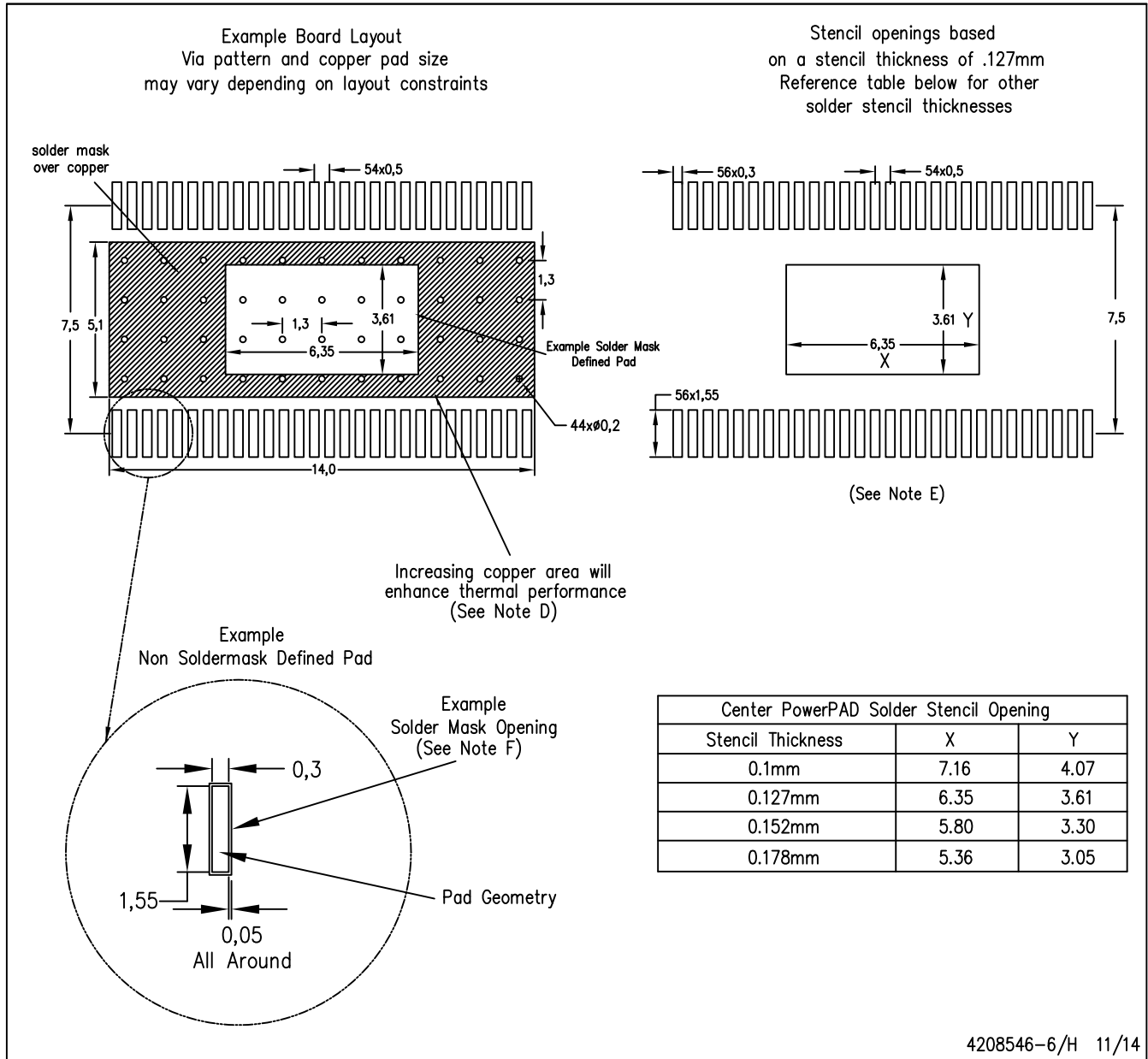
Exposed Thermal Pad Dimensions

4206320-15/S 11/14

NOTES: A. All linear dimensions are in millimeters

- △ Keep-out features are identified to prevent board routing interference. These exposed metal features may vary within the identified area or completely absent on some devices.

PowerPAD is a trademark of Texas Instruments.



4208546-6/H 11/14

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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