PC Card Controllers

FEATURES

- **Fully compatible with the Intel™ 430TX (Mobile Triton II) chipset**
- **A 208-pin Low-Profile QFP (PDV), 209-terminal MicroStar BGA™ package (GHK), or the 209-terminal lead-free (Pb, atomic number 82) MicroStar BGA™ package (ZHK).**
- **3.3-V core logic with universal PCI interfaces compatible with 3.3-V and 5-V PCI signaling environments**
- **Mix-and-match 5-V/3.3-V 16-bit PC Cards and 3.3-V CardBus Cards**
- **Two PC Card or CardBus slots with hot insertion and removal**
- **Uses serial interface to TI™ TPS2206/2216 dual-slot PC Card power switch**
- **Burst transfers to maximize data throughput with CardBus Cards**
- **Parallel PCI interrupts, parallel ISA IRQ and parallel PCI interrupts, serial ISA IRQ with parallel PCI interrupts, and serial ISA IRQ and PCI interrupts**
- **Serial EEPROM interface for loading subsystem ID and subsystem vendor ID**
- **Pipelined architecture allows greater than 130M bps throughput from CardBus-to-PCI and from PCI-to-CardBus**
- **Up to five general-purpose I/Os**
- **Programmable output select for $\overline{\text{CLKRUN}}$**
- **Multifunction PCI device with separate configuration space for each socket**
- **Five PCI memory windows and two I/O windows available for each R2 socket**
- **Two I/O windows and two memory windows available to each CardBus socket**
- **Exchangeable Card Architecture (ExCA) compatible registers are mapped in memory and I/O space**
- **Intel 82365SL-DF and 82365SL register compatible**
- **Distributed DMA (DDMA) and PC/PCI DMA**
- **16-Bit DMA on both PC Card sockets**
- **Ring indicate, $\overline{\text{SUSPEND}}$, PCI $\overline{\text{CLKRUN}}$, and CardBus $\overline{\text{CCLKRUN}}$**
- **Socket activity LED pins**
- **PCI Bus Lock ($\overline{\text{LOCK}}$)**
- **Advanced Submicron, Low-Power CMOS Technology**
- **Internal Ring Oscillator**

DESCRIPTION

The TI PCI1420, the industry's first 208-pin controller to meet the *PCI Bus Power Management Interface Specification for PCI to CardBus Bridges*, is a high-performance PCI-to-CardBus controller that supports two independent card sockets compliant with the *1997 PC Card Standard*. The PCI1420 provides features that make it the best choice for bridging between PCI and PC Cards in both notebook and desktop computers. The *1997 PC Card Standard* retains the 16-bit PC Card specification defined in *PCI Local Bus Specification* and defines the new 32-bit PC Card, CardBus, capable of full 32-bit data transfers at 33 MHz. The PCI1420 supports any combination of 16-bit and CardBus PC Cards in the two sockets, powered at 5 V or 3.3 V, as required.

The PCI1420 is compliant with the *PCI Local Bus Specification*, and its PCI interface can act as either a PCI master device or a PCI slave device. The PCI bus mastering is initiated during 16-bit PC Card DMA transfers or CardBus PC Card bridging transactions. The PCI1420 is also compliant with the latest *PCI Bus Power Management Interface Specification*.

All card signals are internally buffered to allow hot insertion and removal without external buffering. The PCI1420 is register compatible with the Intel 82365SL-DF and 82365SL ExCA controllers. The PCI1420 internal data path logic allows the host to access 8-, 16-, and 32-bit cards using full 32-bit PCI cycles for maximum performance. Independent buffering and a pipeline architecture provide an unsurpassed performance level with sustained bursting. The PCI1420 can also be programmed to accept fast posted writes to improve system-bus utilization.

Multiple system-interrupt signaling options are provided, including: parallel PCI, parallel ISA, serialized ISA, and serialized PCI. Furthermore, general-purpose inputs and outputs are provided for the board designer to implement sideband functions. Many other features designed into the PCI1420, such as socket activity light-emitting diode (LED) outputs, are discussed in detail throughout the design specification.

An advanced complementary metal-oxide semiconductor (CMOS) process achieves low system power consumption while operating at PCI clock rates up to 33 MHz. Several low-power modes enable the host power management system to further reduce power consumption.

NOTE:

This product is for high-volume PC applications only. For a complete datasheet or more information contact support@ti.com.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCI1420PDV	LIFEBUY	LQFP	PDV	208	36	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		PCI1420PDV	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

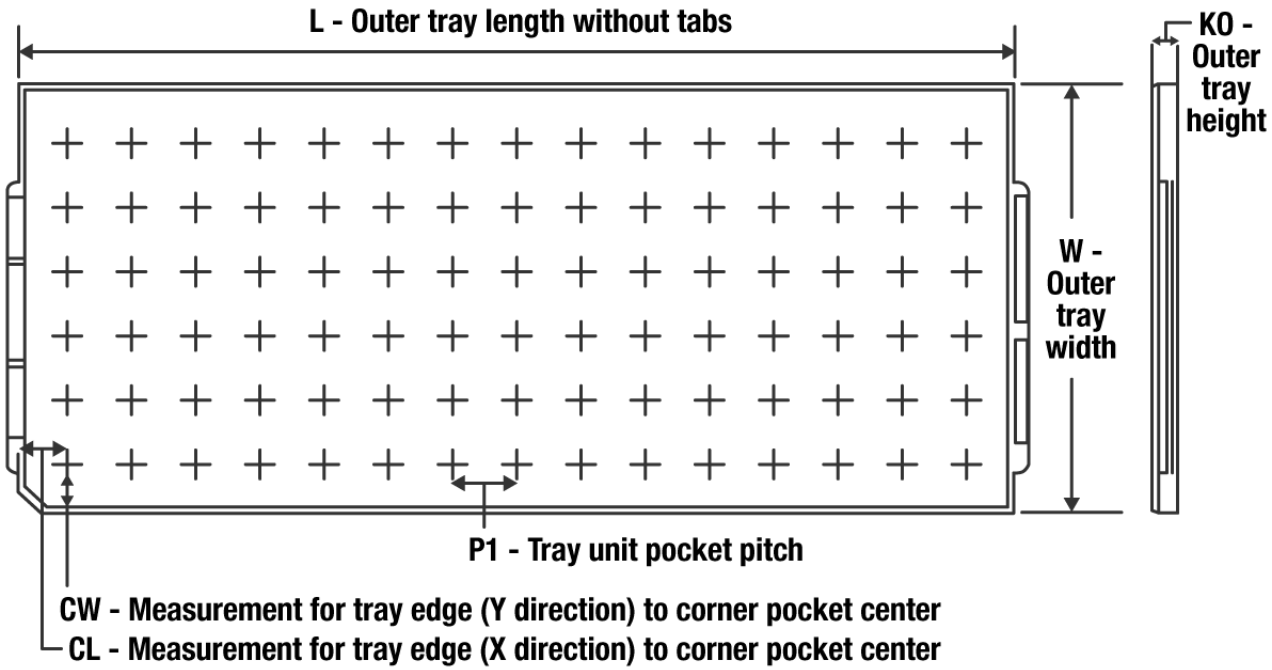
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
PCI1420PDV	PDV	LQFP	208	36	4 x 9	150	315	135.9	7620	32.2	28.7	19.65

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