

## TPD3E001 Low-Capacitance 3-Channel ESD-Protection for High-Speed Data Interfaces

### 1 Features

- IEC61000-4-2 Level-4 ESD Protection
  - $\pm 8$ -kV IEC 61000-4-2 Contact Discharge
  - $\pm 15$ -kV IEC 61000-4-2 Air-Gap Discharge
- 5.5-A Peak Pulse Current (8/20- $\mu$ s Pulse)
- I/O Capacitance: 1.5 pF (Typical)
- Low Leakage Current: 1-nA (Maximum)
- Low Supply Current: 1-nA (Typical)
- 0.9-V to 5.5-V Supply-Voltage Range
- Space-Saving DRY, DRL, and DRS Package Options
- Alternate 2-, 4-, and 6-Channel Options Available: TPD2E2U06, TPD4E1U06, and TPD6E001

### 2 Applications

- End Equipments
  - Blood Glucose Meters
  - Video Surveillance Equipment
  - Portable Data Terminal
  - Industrial Monitor
- Interfaces
  - USB2.0
  - SDIO
  - Precision Analog Interface
  - SVGA Video Connections

### 3 Description

The TPD3E001 is a three-channel Transient Voltage Suppressor (TVS) based Electrostatic Discharge (ESD) protection diode array. The TPD3E001 is rated to dissipate ESD strikes at the maximum level specified in the IEC 61000-4-2 international standard (Level 4). This device has a 1.5-pF IO capacitance per channel, making it ideal for use in high-speed data IO interfaces. The ultra low leakage current (<1 nA max) is suitable for precision analog measurements in applications like glucose meters and heart rate monitors.

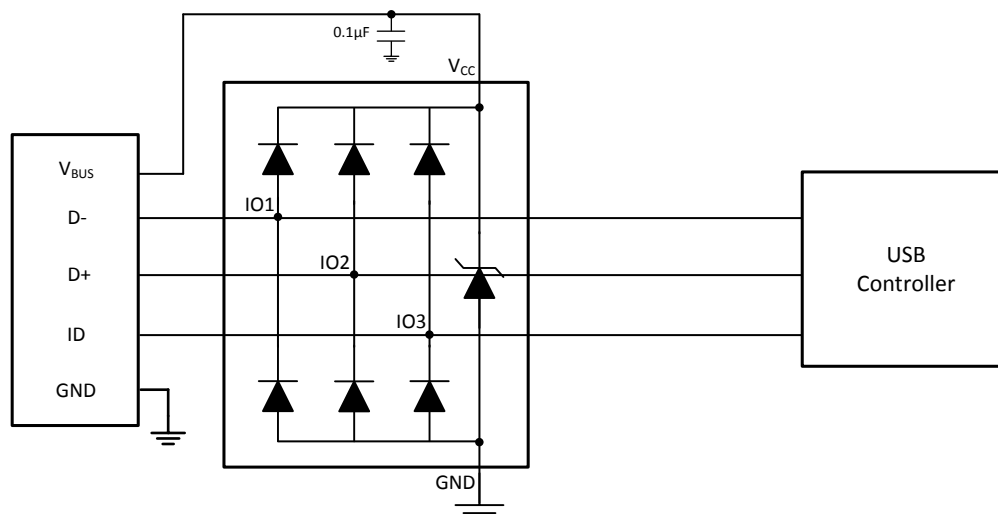
The TPD3E001 is available in space saving DRY (USON), DRL (SOT), and DRS (WSON) packages and is specified for  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  operation. Also see [TPD2E2U06](#), [TPD4E1U06](#), and [TPD6E001](#) which are 2, 4, and 6 channel ESD protection options, respectively, for ESD protection diode arrays with a different number of channels. The TPD2E2U06 provides a higher level of IEC ESD protection, when compared to the TPDxE001 family, and removes the need for an input capacitor. The TPD4E1U06 removes the need for an input capacitor, provides higher IEC ESD protection, and provides lower capacitance, when compared to the TPDxE001 family.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD3E001	SOT (5)	1.60 mm x 1.20 mm
	WSON (6)	3.00 mm x 3.00 mm
	USON (6)	1.45 mm x 1.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

#### Application Schematic



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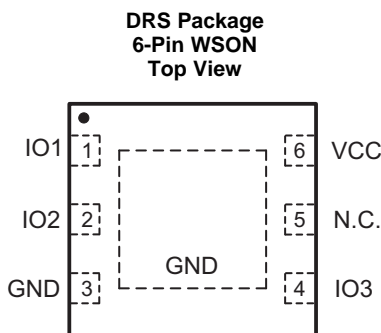
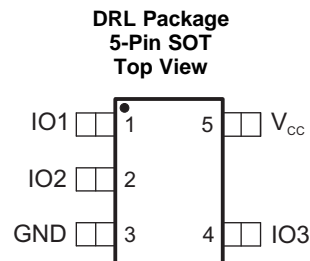
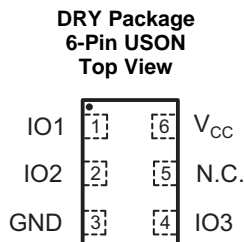
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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (April 2013) to Revision F	Page
<ul style="list-style-type: none"> <li>• Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....</li> </ul>	1

## 5 Pin Configuration and Functions



### Pin Functions

NAME	PIN			TYPE	DESCRIPTION
	DRY NO.	DRL NO.	DRS NO.		
IOx	1, 2, 4	1, 2, 4	1, 2, 4	I/O	ESD-protected channel
GND	3	3	3	GND	Ground
V <sub>CC</sub>	6	5	6	Power	Power-supply input. Bypass V <sub>CC</sub> to GND with a 0.1- $\mu$ F ceramic capacitor.
N.C.	5	–	5	–	No connection. Not internally connected.
EP	–	–	Exposed Thermal Pad	GND	Exposed thermal pad. Connect to GND or leave floating.

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>		-0.3	7	V
V <sub>I/O</sub>	IO voltage tolerance	-0.3	V <sub>CC</sub> + 0.3	V
T <sub>J</sub>	Junction temperature		150	°C
	Lead temperature (soldering, 10 s)		300	°C
	Peak pulse power (tp = 8/20 μs)		90	W
	Peak pulse power (tp = 8/20 μs)		5.5	A
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±15000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1500
		IEC 61000-4-2 Contact Discharge	±8000
		IEC 61000-4-2 Air-gap Discharge	±15000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Operating Voltage	V <sub>CC</sub> Pin	0.9		5.5	V
	IOx Pin	0		V <sub>CC</sub>	
Operating free-air temperature, T <sub>A</sub>		-40		85	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	TPD3E001			UNIT	
	DRL (SOT)	DRS (WSON)	DRY (USON)		
	5 PINS	6 PINS	6 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	266.3	91.9	374.2	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	111.5	106.9	223.4	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	84.5	64.8	227.8	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	16.0	10.2	52.9	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	84.0	64.9	224.8	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	29.9	87.5	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

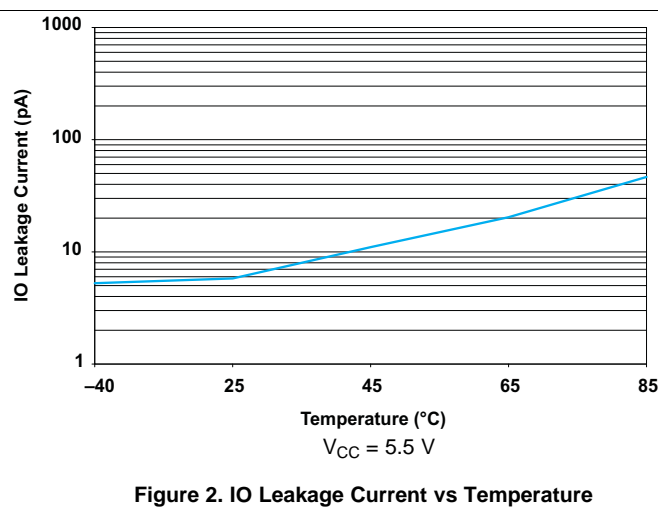
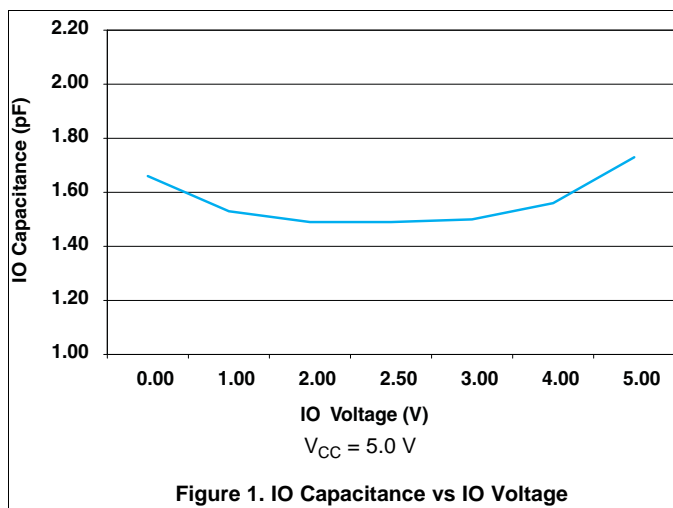
### 6.5 Electrical Characteristics

V<sub>CC</sub> = 5 V ± 10%, T<sub>A</sub> = -40°C to 85°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>CC</sub>	Supply voltage		0.9		5.5	V
I <sub>CC</sub>	Supply current			1	100	nA
V <sub>F</sub>	Diode forward voltage	I <sub>F</sub> = 10 mA	0.65		0.95	V
V <sub>BR</sub>	Breakdown Voltage	I <sub>BR</sub> = 10mA	11			V
V <sub>C</sub>	Channel clamp voltage <sup>(2)</sup>	T <sub>A</sub> = 25°C, ±15-kV HBM, I <sub>F</sub> = 10 A	Positive transients		V <sub>CC</sub> + 25	V
			Negative transients		-25	
		T <sub>A</sub> = 25°C, ±8-kV Contact Discharge (IEC 61000-4-2), I <sub>F</sub> = 24 A	Positive transients		V <sub>CC</sub> + 60	
			Negative transients		-60	
		T <sub>A</sub> = 25°C, ±15-kV Air-Gap Discharge (IEC 61000-4-2), I <sub>F</sub> = 45 A	Positive transients		V <sub>CC</sub> + 100	
			Negative transients		-100	
I <sub>i/o</sub>	Channel leakage current	V <sub>i/o</sub> = GND or V <sub>CC</sub>			±1	nA
C <sub>io</sub>	Channel input capacitance	V <sub>CC</sub> = 5 V, bias of V <sub>CC</sub> /2		1.5		pF
R <sub>dyn</sub>	Dynamic resistance	I <sub>i/o</sub> = 1 A, between IO pin and ground		1.2		Ω

- (1) Typical values are at V<sub>CC</sub> = 5 V and T<sub>A</sub> = 25°C.
- (2) Channel clamp voltage is not production tested.

### 6.6 Typical Characteristics

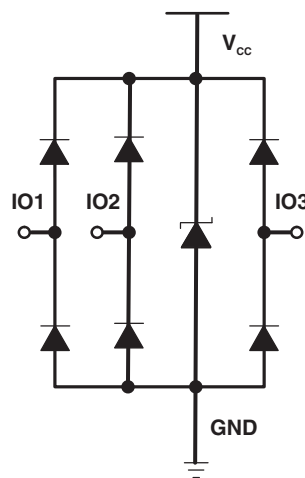


## 7 Detailed Description

### 7.1 Overview

The TPD3E001 is a three-channel Transient Voltage Suppressor (TVS) based Electrostatic Discharge (ESD) protection diode array. The TPD3E001 is rated to dissipate ESD strikes at the maximum level specified in the IEC 61000-4-2 international standard (Level 4). This device has a 1.5-pF IO capacitance per channel, making it ideal for use in high-speed data IO interfaces. The ultra low leakage current ( $< 1$  nA maximum) is suitable for precision analog measurements in applications like glucose meters and heart rate monitors. The wide voltage range on  $V_{CC}$  (up to 5.5V) gives this device the flexibility to be used in a wide variety of applications. Having 3-channels of ESD protection makes this device particularly well suited to protect a micro-AB USB connector, which has three signal lines to be protected (D+, D-, ID). The  $V_{BUS}$  pin can also be protected by connecting it to  $V_{CC}$  on TPD3E001. Therefore, TPD3E001 is a one-chip solution to provide Level 4 IEC 61000-4-2 ESD protection on every pin of the micro-AB USB connector.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

TPD3E001 is a uni-directional ESD protection device with low capacitance. The device is constructed with a central ESD clamp that features two hiding diodes per line to reduce the capacitive loading. This central ESD clamp is also connected to  $V_{CC}$  to provide protection for the  $V_{CC}$  line. Each IO line is rated to dissipate ESD strikes at the maximum level specified in the IEC 61000-4-2 level 4 international standard. The TPD3E001's low loading capacitance makes it ideal for protection high-speed signal terminals.

### 7.4 Device Functional Modes

TPD3E001 is a passive-integrated circuit that activates whenever voltages above  $V_{BR}$  or below the lower diodes  $V_{forward}$  ( $-0.6$ V) are present upon the circuit being protected. During ESD events, voltages as high as  $\pm 15$  kV can be directed to ground and  $V_{CC}$  via the internal diode network. Once the voltages on the protected lines fall below the trigger voltage of the TPD3E001 (usually within 10's of nano-seconds) the device reverts back to a high-impedance state.

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

TPD3E001 is a diode array type Transient Voltage Suppressor (TVS) which is typically used to provide a path to ground for dissipating ESD events on hi-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low  $R_{DYN}$  of the triggered TVS holds this voltage,  $V_{CLAMP}$ , to a tolerable level to the protected IC.

### 8.2 Typical Application

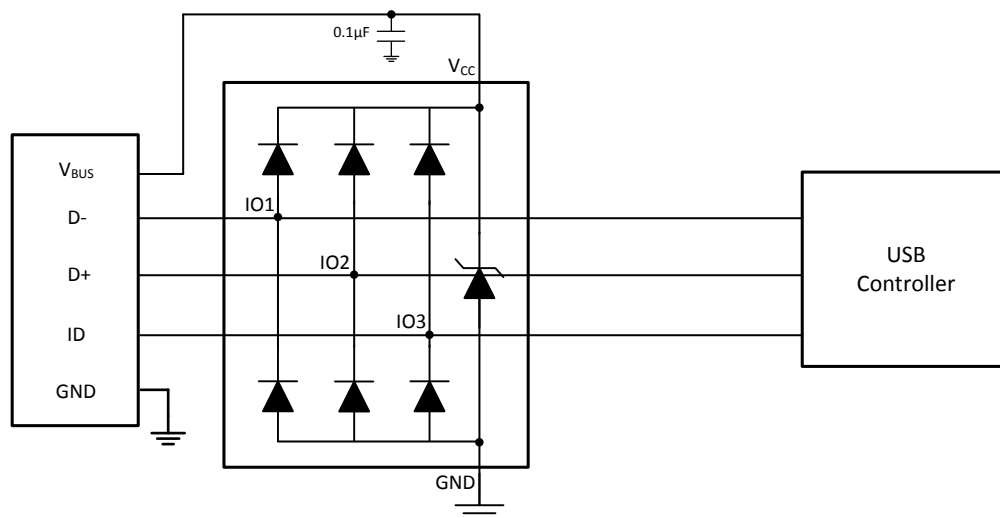


Figure 3. Typical Application Schematic

#### 8.2.1 Design Requirements

For this design example, a single TPD3E001 is used to protect all the pins of a USB2.0 micro-AB connector. The micro-AB connector has an extra pin, the ID pin, which is used by the device to determine whether it is to perform the "A" role or the "B" role. This functionality the ID offers is part of the USB On-the-Go (OTG) Standard. The TPD3E001 offers 3-channels of IEC Level ESD protection to provide complete protection for the USB micro-AB style connector, plus  $V_{CC}$  ( $V_{BUS}$ , D+, D-, ID).

Given the USB application, the following parameters are known.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Signal range on IO1, IO2	0 V to 3.6 V
State of IO3 (ID)	GND or Floating
Signal voltage range on $V_{CC}$	0 V to 5.25 V
Operating Frequency	240 MHz

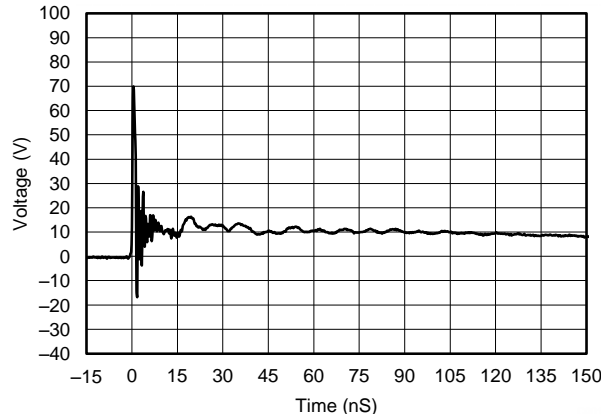
## 8.2.2 Detailed Design Procedure

When placed near the USB connectors, the TPD3E001 ESD solution offers little or no signal distortion during normal operation due to low IO capacitance and ultra-low leakage current specifications. The TPD3E001 ensures that the core circuitry is protected and the system is functioning properly in the event of an ESD strike. For proper operation, the following layout/ design guidelines should be followed:

1. Place the TPD3E001 solution close to the connectors. This allows the TPD3E001 to take away the energy associated with ESD strike before it reaches the internal circuitry of the system board.
2. Place a 0.1- $\mu$ F capacitor very close to the  $V_{CC}$  pin. This limits any momentary voltage surge at the IO pin during the ESD strike event.
3. Ensure that there is enough metallization for the  $V_{CC}$  and GND loop. During normal operation, the TPD3E001 consumes approximately 1 nA (typ.) supply current through the  $V_{CC}$  and GND loop. But during the ESD event,  $V_{CC}$  and GND may see 15 A to 30 A of current, depending on the ESD level. Sufficient current path enables safe discharge of all the energy associated with the ESD strike.
4. Leave the unused IO pins floating. In this example of protecting a micro-AB type USB port, none of the IO pins will be left unused.
5. The  $V_{CC}$  pin can be connected in two different ways:
  - (a) If the  $V_{CC}$  pin is connected to the system power supply, the TPD3E001 works as a transient suppressor for any signal swing above  $V_{CC} + V_F$ . A 0.1- $\mu$ F capacitor on the device  $V_{CC}$  pin is recommended for ESD bypass.
  - (b) If the  $V_{CC}$  pin is not connected to the system power supply, the TPD3E001 can tolerate higher signal swing in the range up to 10 V. Please note that a 0.1- $\mu$ F capacitor is still recommended at the  $V_{CC}$  pin for ESD bypass.

## 8.2.3 Application Curve

Figure 4 is a capture of the voltage clamping waveform of TPD3E001 on IO1 during a +8kV Contact IEC61000-4-2 ESD strike.



**Figure 4. TPD3E001 +8kV Contact IEC61000-4-2 Voltage Clamping Waveform**



## 9 Power Supply Recommendations

TPD3E001 is a passive TVS diode, so there is no requirement to power this device. However, for best IEC 61000-4-2 ESD performance and lowest capacitance performance, it is recommended that the  $V_{CC}$  pin is biased with a 5V supply and that a 0.1 $\mu$ F capacitor is placed near the  $V_{CC}$  pin. Take care to make sure that the maximum voltage specification for the  $V_{CC}$  pin is not violated.

## 10 Layout

### 10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

### 10.2 Layout Example

Figure 5 is an example of how to layout three data lines with the TPD3E001. One example could be protecting a USB micro-AB connector from IEC ESD, as discussed in the Application and Implementation section.

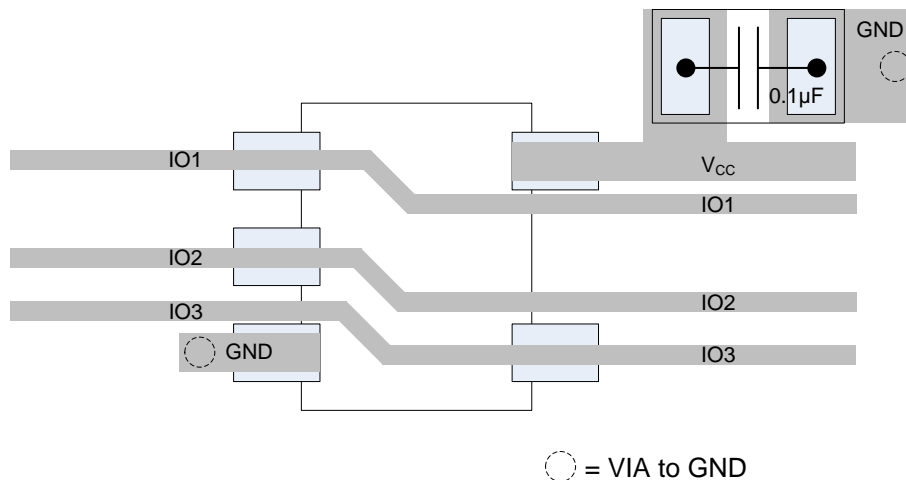


Figure 5. Routing with the DRL Package

## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation see the following:

1. TPD2E2U06 Data Sheet, [SLLSEG9](#)
2. TPD4E1U06 Data Sheet, [SLVSBQ9](#)
3. TPD6E001 Data Sheet, [SLLS685](#)

### 11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.3 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD3E001DRLR	ACTIVE	SOT-5X3	DRL	5	4000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	2BR 2BH	<a href="#">Samples</a>
TPD3E001DRLRG4	ACTIVE	SOT-5X3	DRL	5	4000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	2BR 2BH	<a href="#">Samples</a>
TPD3E001DRSR	ACTIVE	SON	DRS	6	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZWL	<a href="#">Samples</a>
TPD3E001DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2B	<a href="#">Samples</a>
TPD3E001DRYRG4	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2B	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD3E001DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TPD3E001DRSR	SON	DRS	6	1000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPD3E001DRYR	SON	DRY	6	5000	180.0	9.5	1.2	1.65	0.7	4.0	8.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD3E001DRLR	SOT-5X3	DRL	5	4000	183.0	183.0	20.0
TPD3E001DRSR	SON	DRS	6	1000	356.0	356.0	35.0
TPD3E001DRYR	SON	DRY	6	5000	189.0	185.0	36.0

## GENERIC PACKAGE VIEW

**DRY 6**

**USON - 0.6 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4207181/G

DRY0006A



# PACKAGE OUTLINE

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

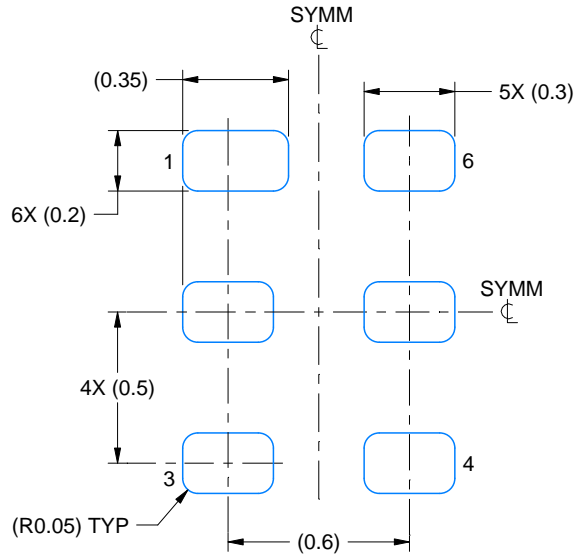


# EXAMPLE BOARD LAYOUT

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



**LAND PATTERN EXAMPLE**  
 1:1 RATIO WITH PKG SOLDER PADS  
 EXPOSED METAL SHOWN  
 SCALE:40X



**SOLDER MASK DETAILS**

4222894/A 01/2018

NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.075 - 0.1 mm THICK STENCIL  
SCALE:40X

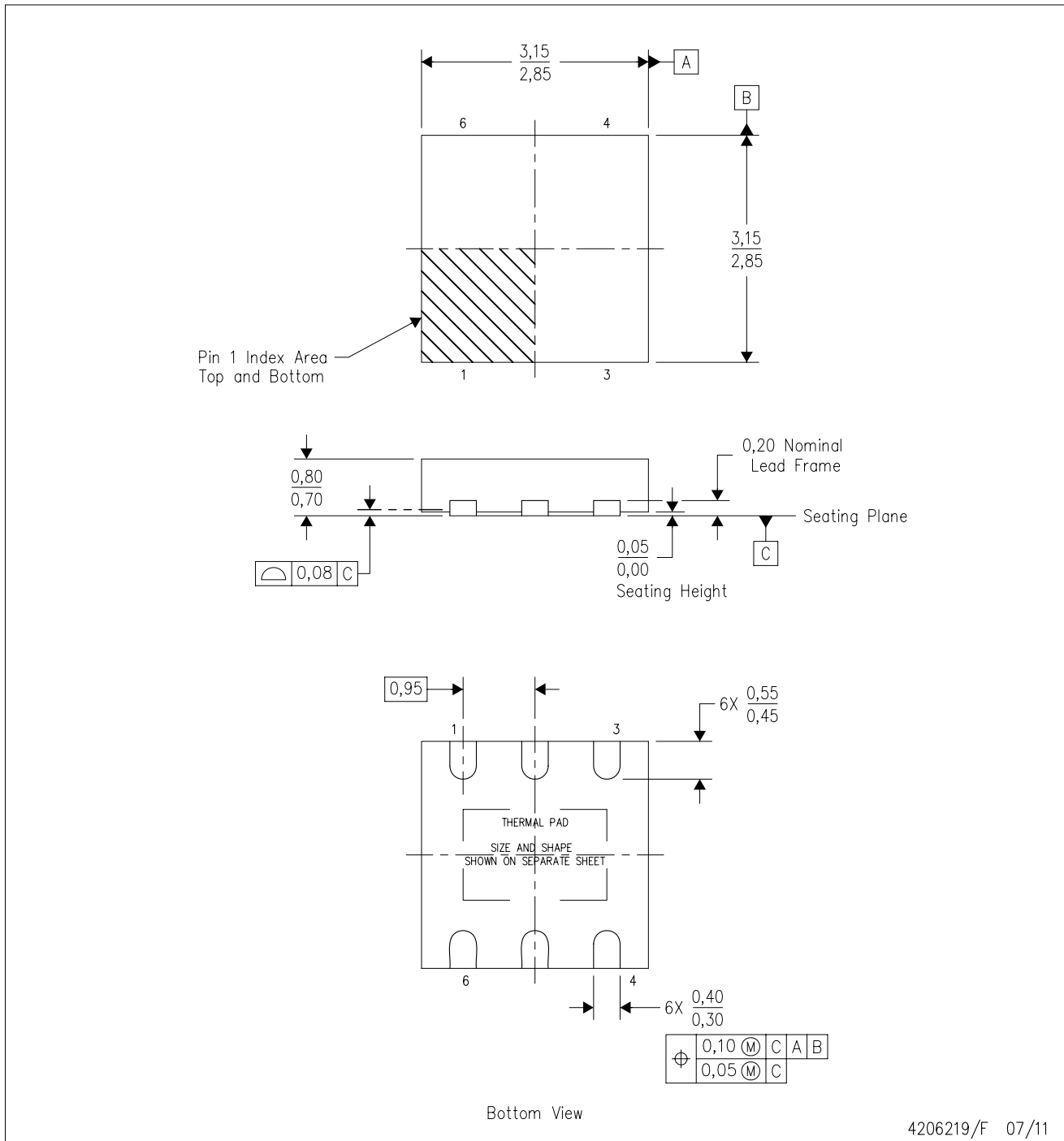
4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DRS (S-PWSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - SON (Small Outline No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

## THERMAL PAD MECHANICAL DATA

DRS (S-PWSON-N6)

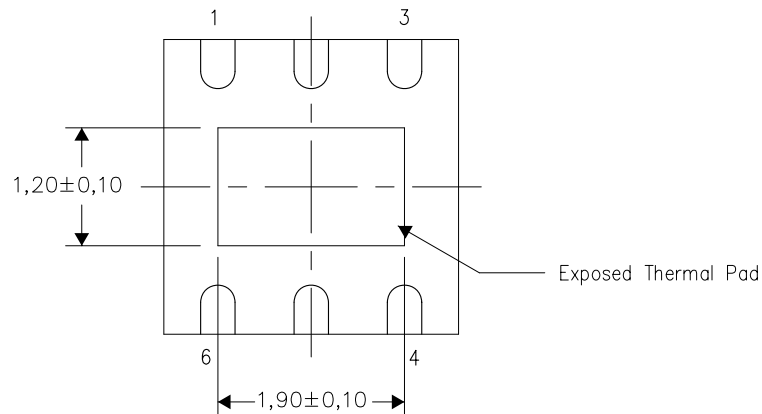
PLASTIC SMALL OUTLINE NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

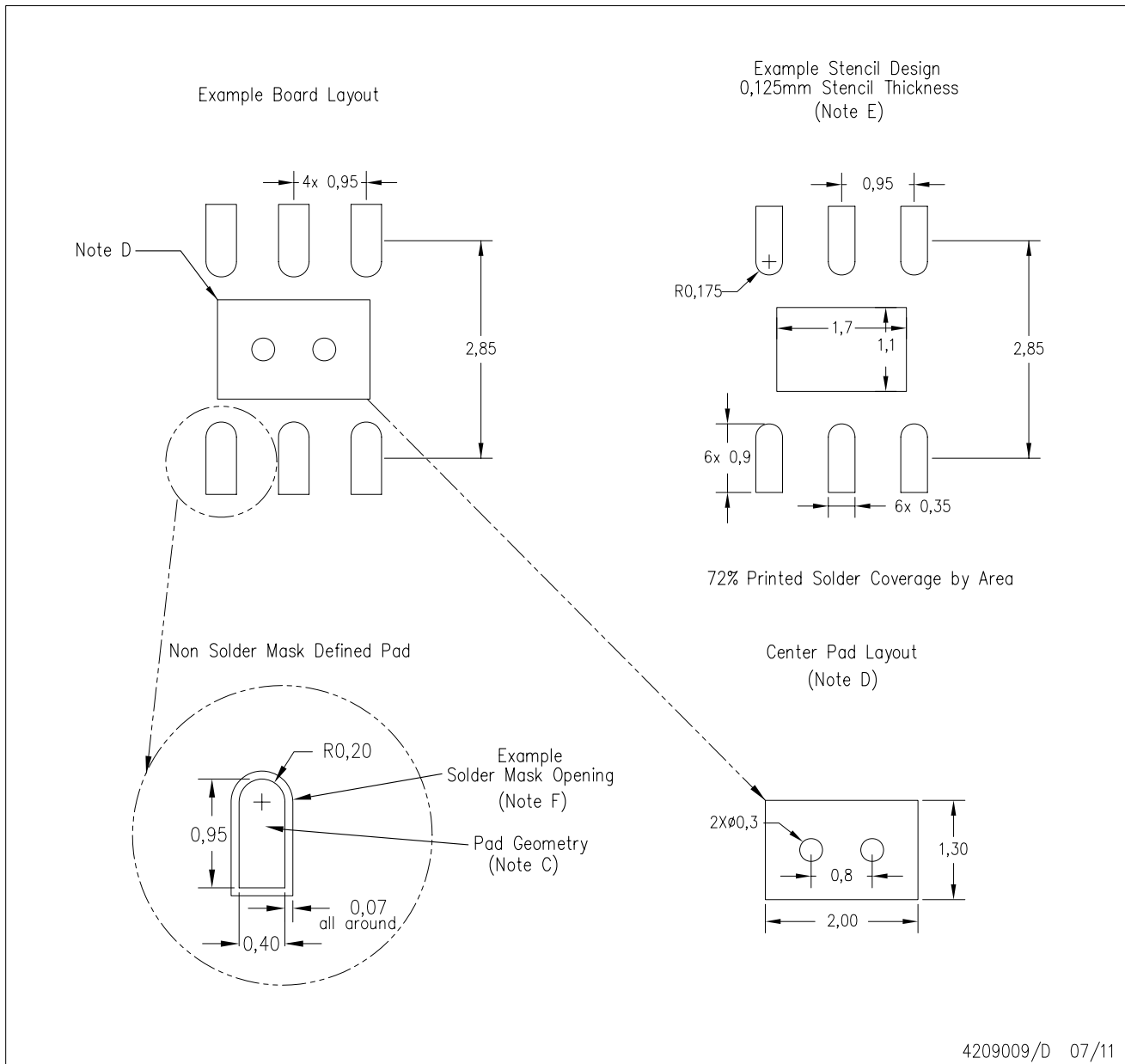
Exposed Thermal Pad Dimensions

4207663/E 07/11

NOTE: All linear dimensions are in millimeters

DRS (S-PWSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for solder mask tolerances.

DRL0005A



# PACKAGE OUTLINE

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



4220753/B 12/2020

NOTES:

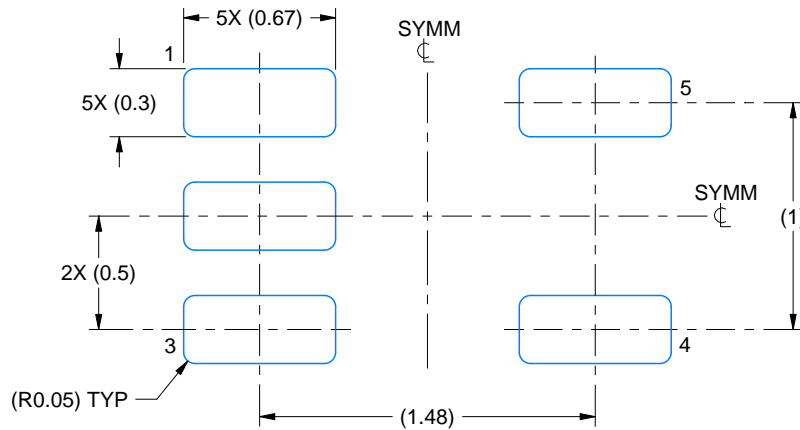
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1

# EXAMPLE BOARD LAYOUT

DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:30X



SOLDERMASK DETAILS

4220753/B 12/2020

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

4220753/B 12/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



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