1 Features

- Six-Channel EMI Filtering for Data Ports
  - -57-dB Crosstalk Attenuation at 100 MHz
  - -35-dB Insertion Loss at 800 MHz
  - -3-dB Bandwidth at 100 MHz
- Robust ESD Protection Exceeds IEC 61000-4-2 (Level 4)
  - ±20-kV IEC 61000-4-2 Contact Discharge
  - ±30-kV IEC 61000-4-2 Air-Gap Discharge
- Pi-Style (C-R-C) Filter Configuration
  \( R = 100 \Omega, C_{TOTAL} = 34 \text{ pF} \)
- Low Leakage Current: 20 nA (Maximum)
- Space-Saving WSON Package (3 mm \( \times \) 1.35 mm)

2 Applications

- LCD Display Interface
- GPIO
- Memory Interface
- Data Lines at Flex Cables
- FPD-Link

3 Description

The TPD6F002 device is a highly-integrated device that provides a six-channel Electromagnetic Interference (EMI) filter and a TVS based ESD protection diode array. The low-pass filter array suppresses EMI/RFI emissions for data ports subject to electromagnetic interference. The TVS diode array is rated to dissipate ESD strikes above the maximum level specified in the IEC 61000-4-2 international standard. The high level of integration, combined with its small easy-to-route DSV package, allows this device to provide great circuit protection for LCD displays, memory interfaces, GPIO lines, and FPD-Link.

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPD6F002</td>
<td>WSON (12)</td>
<td>3.00 mm ( \times ) 1.35 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Equivalent Schematic Representation

[Diagram showing the schematic representation of the TPD6F002 device, including Ch_In, Ch_Out, 100 Ω, C1 = 17 pF, C2 = 17 pF, and GND.]
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4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (November 2009) to Revision B

- Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. ................................................................. 1
- Removed Ordering Information table .................................................................................................................................... 1
5 Pin Configuration and Functions

![DSV Package 12-Pin WSON Top View]

<table>
<thead>
<tr>
<th>PIN</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>ChX_In</td>
<td>1, 2, 3, 4, 5, 6</td>
<td>I/O</td>
</tr>
<tr>
<td>ChX_Out</td>
<td>7, 8, 9, 10, 11, 12</td>
<td>I/O</td>
</tr>
<tr>
<td>GND</td>
<td>G</td>
<td>Ground</td>
</tr>
</tbody>
</table>

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>VIO</th>
<th>I/O to GND</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>T_J</td>
<td>Junction temperature</td>
<td>0</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>T_STG</td>
<td>Storage temperature</td>
<td>−65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Stresses beyond those listed under **Absolute Maximum Ratings** may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under **Recommended Operating Conditions**. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V(ESD)</td>
<td>Electrostatic discharge</td>
</tr>
<tr>
<td>Human-body model(^{(1)})</td>
<td>±15000</td>
</tr>
<tr>
<td>IEC 61000-4-2 contact discharge</td>
<td>±20000</td>
</tr>
<tr>
<td>IEC 61000-4-2 air-gap discharge</td>
<td>±30000</td>
</tr>
</tbody>
</table>

\(^{(1)}\) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIO</td>
<td>Input pin voltage</td>
</tr>
<tr>
<td>0</td>
<td>5.5</td>
</tr>
<tr>
<td>T_A</td>
<td>Operating free-air temperature</td>
</tr>
<tr>
<td>−40</td>
<td>85</td>
</tr>
</tbody>
</table>
6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>TPD6F002</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>DSV (WSON)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>12 PINS</td>
<td></td>
</tr>
<tr>
<td>( R_{JA} ) Junction-to-ambient thermal resistance</td>
<td>120.7</td>
<td>°C/W</td>
</tr>
<tr>
<td>( R_{JC(top)} ) Junction-to-case (top) thermal resistance</td>
<td>104.4</td>
<td>°C/W</td>
</tr>
<tr>
<td>( R_{JB} ) Junction-to-board thermal resistance</td>
<td>78.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>( \psi_{JT} ) Junction-to-top characterization parameter</td>
<td>13</td>
<td>°C/W</td>
</tr>
<tr>
<td>( \psi_{JB} ) Junction-to-board characterization parameter</td>
<td>77.7</td>
<td>°C/W</td>
</tr>
<tr>
<td>( R_{JC(bot)} ) Junction-to-case (bottom) thermal resistance</td>
<td>66.5</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics

\( T_A = -40°C \) to 85°C (Unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP(1)</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{BR} ) DC breakdown voltage</td>
<td>( I_{IO} = 10 \mu A )</td>
<td>6</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( R ) Resistance</td>
<td>85</td>
<td>100</td>
<td></td>
<td>115</td>
<td>Ω</td>
</tr>
<tr>
<td>( C ) Capacitance (C1 or C2)</td>
<td>( V_{IO} = 2.5 \text{ V} )</td>
<td>17</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>( I_{IO} ) Channel leakage current</td>
<td>( V_{IO} = 3.3 \text{ V} )</td>
<td>1</td>
<td>20</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>( f_C ) Cutoff frequency</td>
<td>( Z_{SOURCE} = 50 \Omega, Z_{LOAD} = 50 \Omega )</td>
<td>100</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
</tbody>
</table>

(1) Typical values are at \( T_A = 25°C \).
6.6 Typical Characteristics

**Figure 1. DC Voltage-Current Sweep Across Input, Output Pins**

**Figure 2. Series Resistance vs Temperature**

**Figure 3. TPD6F002 Typical Insertion-Loss Characteristics**

**Figure 4. Capacitance (C1 or C2) vs Bias Voltage**

$T_A = 25^\circ C$, DC Bias = 0 V, 50 Ω Environment
7 Detailed Description

7.1 Overview
The TPD6F002 is a highly-integrated ESD protection and EMI filtering device intended for use where small size and ease of routing are important. Common applications include LCD display interfaces, memory interfaces, GPIO lines, and FPD-Link.

7.2 Functional Block Diagram

7.3 Feature Description

7.3.1 Six-Channel EMI Filtering
This device provides six channels for EMI filtering of data lines with the following parameters:

• –57-dB Crosstalk Attenuation at 100 MHz
• –35-dB Insertion Loss at 800 MHz
• –3-dB Bandwidth at 100 MHz

7.3.2 Pi-Style Filter Configuration
This device has a pi-style filtering configuration composed of a series resistor and two capacitors in parallel with the I/O pins. The typical resistor value is 100 Ω and the typical capacitor values are 17 pF each.

7.3.3 Robust ESD Protection
The ESD protection on all pins exceeds the IEC 61000-4-2 level 4 standard. Contact ESD is rated at ±20 kV and Air-gap ESD is rated at ±30 kV.

7.3.4 Low Leakage Current
The I/O pins feature an ultra-low leakage current of 20 nA (maximum) with a bias of 3.3 V

7.3.5 Space-Saving WSON Package
The layout of this device makes it easy to add protection to existing layouts. The packages offer flow-through routing which requires minimal changes to existing layout for addition of these devices. Additionally, the device offers a small, space-saving package that takes a minimal footprint on the board.

7.4 Device Functional Modes
The TPD6F002 is a passive integrated circuit that passively filters EMI and triggers when voltages are above \( V_{BR} \) or below the lower diode voltage (–0.6 V). During ESD events, voltages as high as ±30 kV (air) can be directed to ground through the internal diode network. Once the voltages on the protected line fall below the trigger levels, the device reverts to passive.
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information
The TPD6F002 offers highly-integrated ESD protection and EMI filtering for 6 channels per device. Take care during implementation to make sure that this device fits the application appropriately.

8.2 Typical Application

Figure 5. Display Panel Schematic

8.2.1 Design Requirements
For this design example, three TPD6F002 devices are being used in an 18-bit display panel application. This provides a complete ESD and EMI protection solution for the display connector.

Table 1 lists the parameters for this display panel application.
Table 1. Design Parameters

<table>
<thead>
<tr>
<th>DESIGN PARAMETER</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signal range on all pins except GND</td>
<td>0 V to 5 V</td>
</tr>
<tr>
<td>Operating Frequency</td>
<td>50 MHz</td>
</tr>
</tbody>
</table>

8.2.2 Detailed Design Procedure
To begin the design process, some design parameters must be decided; the designer must know the following:
- Signal range of all the protected lines
- Operating frequency
- Crosstalk response

8.2.2.1 Signal Range on All Protected Lines
The TPD6F002 has 6 identical protection channels for signal lines. All I/O pins support a signal range from 0 to 5.5 V.

8.2.2.2 Operating Frequency
The TPD6F002 has a 100-MHz, –3-dB bandwidth, which supports the operating frequency for this display.

8.2.2.3 Crosstalk Response
The TPD6F002 has a –57-dB crosstalk attenuation at 100 MHz, sufficient for this display.

8.2.3 Application Curve

![Figure 6. Channel-to-Channel Crosstalk](image)
9 Power Supply Recommendations

This device is a passive EMI and ESD device so there is no need to power it. Take care not to violate the recommended $V_{\text{IO}}$ specification (5.5 V) to ensure the device functions properly.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

This application is typical of an 18-bit RGB display panel layout.
11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community**  *TI's Engineer-to-Engineer (E2E) Community.*  Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support**  *TI's Design Support*  Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.4 Glossary

**SLYZ022**  —  *TI Glossary.*  
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPD6F002DSVR</td>
<td>ACTIVE</td>
<td>SON</td>
<td>DSV</td>
<td>12</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>3NS</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

- **TBD**: The Pb-Free/Green conversion plan has not been defined.
  - **Pb-Free (RoHS)**: TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
  - **Pb-Free (RoHS Exempt)**: This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
  - **Green (RoHS & no Sb/Br)**: TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
OTHER QUALIFIED VERSIONS OF TPD6F002:

- Automotive: TPD6F002-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
TAPE AND REEL INFORMATION

*All dimensions are nominal

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0  (mm)</th>
<th>B0  (mm)</th>
<th>K0  (mm)</th>
<th>P1  (mm)</th>
<th>W (mm)</th>
<th>Pin 1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPD6F002DSVR</td>
<td>SON</td>
<td>DSV</td>
<td>12</td>
<td>3000</td>
<td>180.0</td>
<td>8.4</td>
<td>1.74</td>
<td>3.33</td>
<td>1.05</td>
<td>4.0</td>
<td>8.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPD6F002DSVR</td>
<td>SON</td>
<td>DSV</td>
<td>12</td>
<td>3000</td>
<td>183.0</td>
<td>183.0</td>
<td>20.0</td>
</tr>
</tbody>
</table>
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No-Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

Bottom View

Exposed Thermal Pad Dimensions

NOTE: All linear dimensions are in millimeters
NOTES:  
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-
requirements in connection with such selection.

and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory
requirements. Using products in an application does not by itself establish any safety features in the application. Designers must

Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life
support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all
medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

Purpose of Product Selection

Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications
and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such
products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards
and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must
ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in
life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949
and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such
products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards
and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must
ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in
life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use.
Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life
support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all
medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product).
Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications
and that proper product selection is at Designers’ own risk. Designers are solely responsible for compliance with all legal and regulatory
requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer’s non-
compliance with the terms and provisions of this Notice.