1 Features

- Bus I/O Protection
  - ±16-kV HBM Protection
  - ±12-kV IEC61000-4-2 Contact Discharge
  - ±4-kV IEC61000-4-4 Fast Transient Burst
- Industrial Temperature Range –40°C to 85°C
- Large Receiver Hysteresis (60 mV Typical) for Noise Rejection
- Low-Power Consumption
  - <1-µA Standby Current
  - <1-mA Quiescent Current
- Signaling Rate Optimized for 250 kbps
- Create a Custom Design Using the SN65HVD82 With the WEBENCH® Power Designer

2 Applications

- Electrical Meters
- Building Automation
- Industrial Networks
- Security Electronics

3 Description

This device has robust drivers and receivers for demanding industrial applications. The bus pins are robust to ESD events, with high levels of protection to Human-Body Model, Air-Gap Discharge, and Contact Discharge specifications.

The device combines a differential driver and a differential receiver, which operate from a single 5-V power supply. The driver differential outputs and the receiver differential inputs are connected internally to form a bus port suitable for half-duplex (two-wire bus) communication. The device features a wide common-mode voltage range making the device suitable for multi-point applications over long cable runs. The device is characterized from –40°C to 85°C.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN65HVD82</td>
<td>SOIC (8)</td>
<td>4.90 mm × 3.91 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the datasheet.
Table of Contents

1 Features ........................................................................................................................................... 1
2 Applications ..................................................................................................................................... 1
3 Description ...................................................................................................................................... 1
4 Revision History ............................................................................................................................... 2
5 Pin Configuration and Functions ...................................................................................................... 3
6 Specifications .....................................................................................................................................
   6.1 Absolute Maximum Ratings ........................................................................................................ 3
   6.2 ESD Ratings ................................................................................................................................. 3
   6.3 Recommended Operating Conditions .......................................................................................... 4
   6.4 Thermal Information ................................................................................................................... 4
   6.5 Electrical Characteristics .......................................................................................................... 5
   6.6 Switching Characteristics .......................................................................................................... 6
   6.7 Typical Characteristics .............................................................................................................. 6
7 Parameter Measurement Information ............................................................................................ 7
8 Detailed Description ......................................................................................................................... 10
   8.1 Overview .................................................................................................................................. 10
   8.2 Functional Block Diagram ....................................................................................................... 10
8.3 Feature Description ...................................................................................................................... 10
8.4 Device Functional Modes ............................................................................................................. 11
9 Application and Implementation ....................................................................................................... 13
   9.1 Application Information ............................................................................................................. 13
   9.2 Typical Application ................................................................................................................... 19
10 Power Supply Recommendations .................................................................................................. 21
11 Layout ............................................................................................................................................ 21
   11.1 Layout Guidelines .................................................................................................................... 21
   11.2 Layout Example ...................................................................................................................... 22
12 Device and Documentation Support ................................................................................................ 23
   12.1 Device Support ....................................................................................................................... 23
   12.2 Community Resources ........................................................................................................... 23
   12.3 Trademarks ............................................................................................................................. 23
   12.4 Electrostatic Discharge Caution .............................................................................................. 23
   12.5 Glossary ................................................................................................................................ 23
13 Mechanical, Packaging, and Orderable Information ....................................................................... 24

4 Revision History

Changes from Revision A (July 2015) to Revision B Page

• Added WEBENCH links to data sheet ................................................................................................. 1
• Changed pin 6 From: B To: A and pin 7 From: A To: B in Figure 19 .............................................. 15

Changes from Original (October 2012) to Revision A Page

• Added Pin Configuration and Functions section, ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ................................................................. 1
5 Pin Configuration and Functions

D Package
16-Pin SOIC
(Top View)

Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>6</td>
<td>Bus input/output</td>
</tr>
<tr>
<td>B</td>
<td>7</td>
<td>Bus input/output</td>
</tr>
<tr>
<td>D</td>
<td>4</td>
<td>Digital input</td>
</tr>
<tr>
<td>DE</td>
<td>3</td>
<td>Digital input</td>
</tr>
<tr>
<td>GND</td>
<td>5</td>
<td>Reference potential</td>
</tr>
<tr>
<td>R</td>
<td>1</td>
<td>Digital output</td>
</tr>
<tr>
<td>RE</td>
<td>2</td>
<td>Digital input</td>
</tr>
<tr>
<td>VCC</td>
<td>8</td>
<td>Supply</td>
</tr>
</tbody>
</table>

6 Specifications

6.1 Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>PIN</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>Supply voltage</td>
<td>−0.5 V</td>
</tr>
<tr>
<td>Voltage range at A or B Inputs</td>
<td>7 V</td>
<td></td>
</tr>
<tr>
<td>Input voltage range at any logic pin</td>
<td>−18 V</td>
<td></td>
</tr>
<tr>
<td>Voltage input range, transient pulse, A and B, through 100Ω</td>
<td>5.7 V</td>
<td></td>
</tr>
<tr>
<td>Receiver output current</td>
<td>−100 mA</td>
<td></td>
</tr>
<tr>
<td>Junction temperature</td>
<td>170 °C</td>
<td></td>
</tr>
<tr>
<td>Continuous total power dissipation</td>
<td>See Thermal Information</td>
<td></td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>±4000</td>
<td>V</td>
</tr>
<tr>
<td>±1500</td>
<td>V</td>
</tr>
<tr>
<td>±400</td>
<td>V</td>
</tr>
<tr>
<td>±12000</td>
<td>V</td>
</tr>
<tr>
<td>±16000</td>
<td>V</td>
</tr>
<tr>
<td>±4000</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
6.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{CC} ) Supply voltage</td>
<td>4.5</td>
<td>5</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>( V_i ) Input voltage at any bus terminal (separately or common mode)(^{(1)})</td>
<td>–7</td>
<td>12</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{IH} ) High-level input voltage (D, DE and RE inputs)</td>
<td>2</td>
<td>( V_{CC} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{IL} ) Low-level input voltage (D, DE and RE inputs)</td>
<td>0</td>
<td>0.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{ID} ) Differential input voltage (A and B inputs)</td>
<td>–12</td>
<td>12</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( I_O ) Output current, Driver</td>
<td>–60</td>
<td>60</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Output current, Receiver</td>
<td>–8</td>
<td>8</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( R_L ) Differential load resistance</td>
<td>54</td>
<td>60</td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>( C_L ) Differential load capacitance</td>
<td>50</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>( 1/\tau_{UI} ) Signaling rate</td>
<td></td>
<td>250</td>
<td></td>
<td>kbps</td>
</tr>
<tr>
<td>( T_A ) Operating free-air temperature (see Application and Implementation section for thermal information)</td>
<td>–40</td>
<td>85</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>( T_J ) Junction Temperature</td>
<td>–40</td>
<td>150</td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>

\(^{(1)}\) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>SN65HVD82 D (SOIC)</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{\Omega A} ) Junction-to-ambient thermal resistance</td>
<td>116.1 °C/W</td>
</tr>
<tr>
<td>( R_{\Omega C(top)} ) Junction-to-case (top) thermal resistance</td>
<td>60.8 °C/W</td>
</tr>
<tr>
<td>( R_{\Omega B} ) Junction-to-board thermal resistance</td>
<td>57.1 °C/W</td>
</tr>
<tr>
<td>( \psi_{JT} ) Junction-to-top characterization parameter</td>
<td>13.9 °C/W</td>
</tr>
<tr>
<td>( \psi_{JB} ) Junction-to-board characterization parameter</td>
<td>56.5 °C/W</td>
</tr>
</tbody>
</table>

\(^{(1)}\) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.
6.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{OD} )</td>
<td>Driver differential output voltage magnitude</td>
<td>1.5</td>
<td>2</td>
<td>2.5</td>
<td>V</td>
</tr>
<tr>
<td>( \Delta V_{OD} )</td>
<td>Change in magnitude of driver differential output voltage</td>
<td>–0.2</td>
<td>0</td>
<td>0.2</td>
<td>V</td>
</tr>
<tr>
<td>( V_{OC(SS)} )</td>
<td>Steady-state common-mode output voltage</td>
<td>1</td>
<td>( V_{CC}/2 )</td>
<td>3</td>
<td>V</td>
</tr>
<tr>
<td>( \Delta V_{OC} )</td>
<td>Change in differential output common-mode voltage</td>
<td>–0.2</td>
<td>0</td>
<td>0.2</td>
<td>V</td>
</tr>
<tr>
<td>( V_{OC(PP)} )</td>
<td>Peak-to-peak driver common-mode output voltage</td>
<td>850</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( C_{OD} )</td>
<td>Differential output capacitance</td>
<td>8</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{IT+} )</td>
<td>Positive-going receiver differential input voltage threshold</td>
<td>See (1)</td>
<td>–70</td>
<td>–20</td>
<td>mV</td>
</tr>
<tr>
<td>( V_{IT–} )</td>
<td>Negative-going receiver differential input voltage threshold</td>
<td>–200</td>
<td>–150</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>( V_{HYS} )</td>
<td>Receiver differential input voltage threshold hysteresis (( V_{IT+} – V_{IT–} ))</td>
<td>40</td>
<td>60</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>( V_{OH} )</td>
<td>Receiver high-level output voltage</td>
<td>4</td>
<td>( V_{CC}–0.3 )</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{OL} )</td>
<td>Receiver low-level output voltage</td>
<td>0.2</td>
<td>0.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( I_{I} )</td>
<td>Driver input, driver enable, and receiver enable input current</td>
<td>–2</td>
<td>2</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( I_{OZ} )</td>
<td>Receiver output high-impedance current</td>
<td>–10</td>
<td>10</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( I_{OS} )</td>
<td>Driver short-circuit output current</td>
<td>150</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{I} )</td>
<td>Bus input current (disabled driver)</td>
<td>( V_i = 12 ) V, ( V_i = –7 ) V</td>
<td>75</td>
<td>125</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( I_{CC} )</td>
<td>Supply current (quiescent)</td>
<td>Driver and Receiver enabled DE = ( V_{CC}, ) RE = GND, No load</td>
<td>900</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td>Driver enabled, receiver disabled DE = ( V_{CC}, ) RE = ( V_{CC}, ) No load</td>
<td>650</td>
<td></td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td>Driver disabled, receiver disabled DE = GND, RE = GND, No load</td>
<td>650</td>
<td></td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td>Driver and receiver disabled DE = GND, D=GND, RE = ( V_{CC}, ) No load</td>
<td>0.4</td>
<td>2</td>
<td></td>
<td>( \mu A )</td>
</tr>
</tbody>
</table>

(1) Under any specific conditions, \( V_{IT+} \) is assured to be at least \( V_{HYS} \) higher than \( V_{IT–} \).
6.6 Switching Characteristics

over recommended operating conditions (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRIVER</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{rr}$</td>
<td>Driver differential output rise/fall time</td>
<td>400</td>
<td>700</td>
<td>1200</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PHL}, t_{PLH}$</td>
<td>Driver propagation delay</td>
<td>90</td>
<td>700</td>
<td>1000</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{SK(P)}$</td>
<td>Driver pulse skew, $</td>
<td>t_{PHL} - t_{PLH}</td>
<td>$</td>
<td>25</td>
<td>200</td>
</tr>
<tr>
<td>$t_{PZH}, t_{PLZ}$</td>
<td>Driver disable time</td>
<td>50</td>
<td>500</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PZH}, t_{PLZ}$</td>
<td>Driver enable time</td>
<td>3</td>
<td>9</td>
<td></td>
<td>μs</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>RECEIVER</th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{rr}$</td>
<td>Receiver output rise/fall time</td>
<td>18</td>
<td>30</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PHL}, t_{PLH}$</td>
<td>Receiver propagation delay time</td>
<td>85</td>
<td>195</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{SK(P)}$</td>
<td>Receiver pulse skew, $</td>
<td>t_{PHL} - t_{PLH}</td>
<td>$</td>
<td>1</td>
<td>15</td>
</tr>
<tr>
<td>$t_{PLZ}, t_{PZH}$</td>
<td>Receiver disable time</td>
<td>50</td>
<td>500</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PZH}, t_{PLZ}$</td>
<td>Receiver enable time</td>
<td>20</td>
<td>130</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

6.7 Typical Characteristics

Figure 1. Driver Output Voltage vs Driver Output Current

Figure 2. Driver Rise and Fall Time vs Temperature

Figure 3. Supply Current vs Signaling Rate

Figure 4. Receiver Output vs Differential Input Voltage
7 Parameter Measurement Information

Input generator rate is 100 kbps, 50% duty cycle, rise and fall times less than 6 nsec, output impedance 50 Ω.

Figure 5. Measurement of Driver Differential Output Voltage With Common-Mode Load

Figure 6. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

Figure 7. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays

Figure 8. Measurement of Driver Enable and Disable Times With Active High Output and Pull-Down Load

D at 3V to test non-inverting output, D at 0V to test inverting output.
Parameter Measurement Information (continued)

Figure 9. Measurement of Driver Enable and Disable Times With Active Low Output and Pull-up Load

D at 0V to test non-inverting output, D at 3V to test inverting output.

Figure 10. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

Figure 11. Measurement of Receiver Enable/Disable Times With Driver Enabled
Figure 12. Measurement of Receiver Enable Times With Driver Disabled
8 Detailed Description

8.1 Overview
The SN65HVD82 device is a half-duplex RS-485 transceiver suitable for data transmission at rates up to 250 kbps over controlled-impedance transmission media (such as twisted-pair cabling). The device features a high level of internal transient protection, making it able to withstand up ESD strikes up to 12 kV (per IEC 61000-4-2) and EFT transients up to 4 kV (per IEC 61000-4-4) without incurring damage. Up to 256 units of SN65HVD82 may share a common RS-485 bus due to the device’s low bus input currents. The device also features a low standby current consumption of 400 nA (typical).

8.2 Functional Block Diagram

8.3 Feature Description

8.3.1 Receiver Failsafe
The differential receiver is failsafe to invalid bus states caused by:

• open bus conditions such as a disconnected connector
• shorted bus conditions such as cable damage shorting the twisted-pair together, or
• idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver will output a failsafe logic High state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds so that the “input indeterminate” range does not include zero volts differential. In order to comply with the RS-422 and RS-485 standards, the receiver output must output a High when the differential input $V_{ID}$ is more positive than 200 mV, and must output a Low when the $V_{ID}$ is more negative than –200 mV. The receiver parameters which determine the failsafe performance are $V_{IT+}$ and $V_{IT–}$ and $V_{HYS}$. As seen in the Electrical Characteristics table, differential signals more negative than –200 mV will always cause a Low receiver output. Similarly, differential signals more positive than 200 mV will always cause a High receiver output.

When the differential input signal is close to zero, it will still be above the $V_{IT+}$ threshold, and the receiver output will be High. Only when the differential input is more negative than $V_{IT–}$ will the receiver output transition to a Low state. So the noise immunity of the receiver inputs during a bus fault condition includes the receiver hysteresis value $V_{HYS}$ (the separation between $V_{IT+}$ and $V_{IT–}$) as well as the value of $V_{IT+}$.

Signals which transition from positive to negative (or from negative to positive) will transition only once, ensuring no spurious bits.

8.3.2 Low-Power Standby Mode
When both the driver and receiver are disabled (DE transitions to a low state and RE transitions to a high state) the device enters standby mode. If the enable inputs are in this state for a brief time (e.g. less than 100 ns), the device does not enter standby mode. This prevents inadvertently entering standby mode during driver/receiver enabling. Only when the enable inputs are held in this state a sufficient duration (e.g. for 300 ns or more), the device is assured to be in standby mode. In this low-power standby mode, most internal circuitry is powered down, and the steady-state supply current is typically less than 400 nA. When either the driver or the receiver is re-enabled, the internal circuitry becomes active.
### 8.4 Device Functional Modes

#### Table 1. Driver Function Table

<table>
<thead>
<tr>
<th>INPUT</th>
<th>ENABLE</th>
<th>OUTPUTS</th>
<th>ACTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>D</td>
<td>H</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>X</td>
<td>L</td>
<td>Z</td>
<td>Z</td>
</tr>
<tr>
<td>OPEN</td>
<td>OPEN</td>
<td>Z</td>
<td>Z</td>
</tr>
<tr>
<td>OPEN</td>
<td>H</td>
<td>H</td>
<td>L</td>
</tr>
</tbody>
</table>

#### Table 2. Receiver Function Table

<table>
<thead>
<tr>
<th>DIFFERENTIAL INPUT</th>
<th>ENABLE</th>
<th>OUTPUT</th>
<th>ACTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{ID} = V_A - V_B )</td>
<td>RE</td>
<td>R</td>
<td></td>
</tr>
<tr>
<td>( V_{IT+} &lt; V_{ID} )</td>
<td>L</td>
<td>H</td>
<td>Receive valid bus High</td>
</tr>
<tr>
<td>( V_{IT-} &lt; V_{ID} &lt; V_{IT+} )</td>
<td>L</td>
<td>?</td>
<td>Indeterminate bus state</td>
</tr>
<tr>
<td>( V_{ID} &lt; V_{IT-} )</td>
<td>L</td>
<td>L</td>
<td>Receive valid bus Low</td>
</tr>
<tr>
<td>X</td>
<td>H</td>
<td>Z</td>
<td>Receiver disabled</td>
</tr>
<tr>
<td>X</td>
<td>OPEN</td>
<td>Z</td>
<td>Receiver disabled by default</td>
</tr>
<tr>
<td>Open-circuit bus</td>
<td>L</td>
<td>H</td>
<td>Fail-safe high output</td>
</tr>
<tr>
<td>Short-circuit bus</td>
<td>L</td>
<td>H</td>
<td>Fail-safe high output</td>
</tr>
<tr>
<td>Idle (terminated) bus</td>
<td>L</td>
<td>H</td>
<td>Fail-safe high output</td>
</tr>
</tbody>
</table>
Figure 14. Equivalent Input and Output Schematic Diagrams
9 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Device Configuration

The SN65HVD82 is a half-duplex, 250-kbps, RS-485 transceiver operating from a single 5-V supply. The driver and receiver enable pins allow for the configuration of different operating modes.

Using independent enable lines provides the most flexible control as it allows for the driver and the receiver to be turned on and off individually. While this configuration requires two control lines, it allows for selective listening into the bus traffic, whether the driver is transmitting data or not.

Combining the enable signals simplifies the interface to the controller by forming a single, direction-control signal. Thus, when the direction-control line is high, the transceiver is configured as a driver, while for a low the device operates as a receiver.

Tying the receiver-enable to ground and controlling only the driver-enable input, also uses one control line only. In this configuration a node not only receives the data from the bus, but also the data it sends and thus can verify that the correct data have been transmitted.

9.1.2 Bus – Design

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, $R_T$, whose value matches the characteristic impedance, $Z_0$, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.
Application Information (continued)

Common cables used are unshielded twisted pair (UTP), such as low-cost CAT-5 cable with \( Z_0 = 100 \, \Omega \), and proper RS-485 cable with \( Z_0 = 120 \, \Omega \).

Line measurements have shown that making \( R_T \) by up to 10% larger than \( Z_0 \) improves signal quality. Typical cable sizes are AWG 22 and AWG 24.

The theoretical maximum bus length is assumed with 4000 ft or 1200 m, and represents the length of an AWG 24 cable whose cable resistance approaches the value of the termination resistance, thus reducing the bus signal by half or 6 dB.

The theoretical maximum number of bus nodes is determined by the ratio of the RS-485 specified maximum of 32 unit loads (UL) and the actual unit load of the applied transceiver. For example, the SN65HVD82 is a 1/8 UL transceiver. Dividing 32 UL by 1/8 UL yields 256 transceivers that can be connected to one bus.

9.1.3 Cable-Length Versus Data Rate

There is an inverse relationship between data rate and cable length. That is, the higher the data rate the shorter the cable and conversely the lower the data rate the longer the cable. While most RS-485 systems utilize data rates between 10 kbps and 100 kbps, applications such as e-metering often operate at rates of up to 250 kbps even at distances of 4000 feet and above. This is possible by allowing for small signal jitter of up to 5 or 10%.

Figure 16. Typical RS-485 Network with SN65HVD82 Transceivers

Figure 17. Cable Length vs Data Rate Characteristic
Application Information (continued)

9.1.4 Stub – Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. The reason for this is that a stub presents a non-terminated piece of bus line which can introduce reflections if too long. As a rule of thumb the electrical length or round-trip delay of a stub should be less than one tenth of the driver’s rise time, thus leading to a maximum physical stub length of:

\[ L_{Stub} \leq 0.1 \times t_r \times v \times c, \]

with \( t_r \) as the driver’s 10/90 rise time, \( c \) as the speed of light (3 × 10^8 m/s or 9.8 × 10^8 ft/s), and \( v \) as the signal velocity of the cable (\( v = 78\% \)) or trace (\( v = 45\% \)) as a factor of \( c \).

Thus, for the SN65HVD82 with a minimum rise time of 400 ns the maximum cable stub length yields \( L_{Stub} \leq 0.1 \times 400 \times 10^{-9} \times 3 \times 10^8 \times 0.78 = 9.4 \) m or 30.6 ft.

![Figure 18. Stub Length](image)

9.1.5 3-V to 5-V Interface

Interfacing the SN65HVD82 to a 3-V controller is easy. Because the 5-V logic inputs of the transceiver accept 3-V input signals they can be directly connected to the controller I/O. The 5-V receiver output, R, however must be level-shifted via a Schottky diode and a 10-kV resistor to connect to the controller input. When R is high, the diode is reverse biased and the controller supply potential lies at the controller input. When R is low, the diode is forward biased and conducts. In this case only the diode forward voltage of 0.2 V lies at the controller input.

![Figure 19. 3 V – 5 V Interface](image)

9.1.6 Noise Immunity

The input sensitivity of a standard RS-485 transceiver is ±200 mV. When the differential input voltage, \( V_{ID} \), is greater than +200 mV, the receiver output turns high, for \( V_{ID} \leq 200 \) mV the receiver outputs low. Bus voltages in between these levels can cause the receiver output to go high, or low, or even toggle between logic states. Small bus voltages however occur every time during the bus access hand-off from one driver to the next as the low-impedance termination resistors reduce the bus voltage to zero. To prevent receiver output toggling during bus idling, and thus increasing noise immunity, external bias resistors must be applied to create a bus voltage that is greater than the input sensitivity plus any expected differential noise.
Application Information (continued)

The SN65HVD82 transceiver circumvents idle-bus and differential noise issues by providing a positive input threshold of –20 mV and a typical hysteresis of 60 mV. In the case of an idle-bus condition therefore, a differential noise voltage of up to 160 mVpp can be present without causing the receiver output to change states from high to low. This increased noise immunity eliminates the need for idle-bus failsafe bias resistors and allows for long haul data transmissions in noisy environment.

9.1.7 Transient Protection

The bus terminals of the SN65HVD82 transceiver family possess on-chip ESD protection against ±15 kV human body model (HBM) and ±12 kV IEC61000-4-2 contact discharge. As stated in the IEC 61000-4-2 standard, contact discharge is the preferred test method; although IEC air-gap testing is less repeatable than contact testing, air discharge protection levels are inferred from the contact discharge test results. The IEC-ESD test is far more severe than the HBM-ESD test. The 50% higher charge capacitance, CS, and 78% lower discharge resistance, RD of the IEC-model produce significantly higher discharge currents than the HBM-model.

EFTs are usually caused by relay contact bounce or the interruption of inductive loads, while surge transients often results from lightning strikes (direct strike or induced voltages and currents due to an indirect strike), or the switching of power systems including load changes and short circuits switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.
Application Information (continued)

Figure 22 compares the pulse-power of the EFT and surge transients with the power caused by an IEC-ESD transient. As can be seen the tiny blue blip in the bottom left corner of the left diagram represents the power of a 10-kV ESD transient, which already dwarfs against the significantly higher EFT power spike and certainly against the 500-V surge transient. This type of transient power is well representative for factory environments in industrial and process automation. The right diagram compares the enormous power of a 6-kV surge transient, which more likely occurs in e-metering applications of power generating and power grid systems, with the aforementioned 500-V surge transient. Note that the unit of the pulse-power changes from kW to MW, thus making the power of the 500-V surge transient almost dropping off the scale.

Figure 22. Power Comparison of ESD, EFT, and Surge Transients

In the case of surge transients, their long pulse duration and slowly decreasing pulse power signifies high energy content.

The electrical energy of a transient that is dumped onto the transceiver’s internal protections cells is converted into thermal energy, or heat that literally fries the protection cells, thus destroying the transceiver. Figure 23 showcases the large differences in transient energies for single ESD, EFT, and surge transients as well as for an EFT pulse train, commonly applied during compliance testing.
Figure 23. Comparison of Transient Energies

Figure 24 suggests two circuit designs providing protection against surge transients. Table 3 presents the associated bill of material.

Table 3. Bill of Materials

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>FUNCTION</th>
<th>ORDER NUMBER</th>
<th>MANUFACTURER</th>
</tr>
</thead>
<tbody>
<tr>
<td>XCVR</td>
<td>3.3V, 250kbps RS-485 Transceiver</td>
<td>SN65HVD82D</td>
<td>TI</td>
</tr>
<tr>
<td>R1,R2</td>
<td>10Ω, Pulse-Proof Thick-Film Resistor</td>
<td>CRCW0603010RJNEAHP</td>
<td>Vishay</td>
</tr>
<tr>
<td>TVS</td>
<td>Bidirectional 400W Transient Suppressor</td>
<td>CDSOT23-SM712</td>
<td>Bourns</td>
</tr>
<tr>
<td>TBU1,TBU2</td>
<td>Bidirectional. 200mA Transient Blocking Unit</td>
<td>TBU-CA-065-200-WH</td>
<td>Bourns</td>
</tr>
<tr>
<td>MOV1,MOV2</td>
<td>200V, Metal-Oxide Varistor</td>
<td>MOV-10D201K</td>
<td>Bourns</td>
</tr>
</tbody>
</table>

Both circuits are designed for 10-kV ESD and 4-kV EFT transient protection. The left however provides surge protection of ≥ 500-V transients only, while the right protection circuits can withstand 5-kV surge transients.
9.2 Typical Application

9.2.1 Design Requirements
The following list outlines sample design requirements for the typical application example found in Figure 25:

- RS-485-compliant bus interface (needs differential signal amplitude of at least 1.5 V under fully-loaded conditions – essentially, maximum number of nodes connected and with dual 120-Ω termination).
- Galvanic isolation of both signal and power supply lines.
- Able to withstand ESD transients up to 10 kV (per IEC 61000-4-2) and EFTs up to 4 kV (per IEC 61000-4-4).
- Full control of data flow on bus in order to prevent contention (for half-duplex communication).

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools
Click here to create a custom design using the SN65HVD82 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (\(V_{\text{IN}}\)), output voltage (\(V_{\text{OUT}}\)), and output current (\(I_{\text{OUT}}\)) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance

Figure 25. Isolated Bus Node With Transient Protection
Typical Application (continued)

• Export customized schematic and layout into popular CAD formats
• Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.2.2 Isolated Bus Node Design

Many RS-485 networks use isolated bus nodes to prevent the creation of unintended ground loops and their disruptive impact on signal integrity. An isolated bus node typically includes a micro controller that connects to the bus transceiver via a multi-channel, digital isolator (Figure 25).

Power isolation is accomplished using the push-pull transformer driver SN6501 and a low-cost LDO, TPS76350. Signal isolation utilizes the quadruple digital isolator ISO7241. Notice that both enable inputs, EN1 and EN2, are pulled-up via 4.7-kΩ resistors to limit their input currents during transient events.

While the transient protection is similar to the one in Figure 24 (left circuit), an additional high-voltage capacitor is used to divert transient energy from the floating RS-485 common further towards Protective Earth (PE) ground. This is necessary as noise transients on the bus are usually referred to Earth potential.

R_VH refers to a high-voltage resistor, and in some applications even a varistor. This resistance is applied to prevent charging of the floating ground to dangerous potentials during normal operation.

Occasionally varistors are used instead of resistors in order to rapidly discharge C_HV, if it is expected that fast transients might charge C_HV to high-potentials.

Note that the PE island represents a copper island on the PCB for the provision of a short, thick Earth wire connecting this island to PE ground at the entrance of the power supply unit (PSU).

In equipment designs using a chassis, the PE connection is usually provided through the chassis itself. Typically the PE conductor is tied to the chassis at one end while the high-voltage components, C_HV and R_HV, are connecting to the chassis at the other end.

9.2.3 Application Curve

![Figure 26. SN65GVD82 D Input (Top), Differential Output (Middle), and R Output (Bottom), 250 kbps Operation, PRBS Data Pattern](image-url)
10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100-
nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple
present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and
inductance of the PCB power planes.

11 Layout

11.1 Layout Guidelines

11.1.1 Design and Layout Considerations For Transient Protection

On-chip IEC-ESD protection is good for laboratory and portable equipment but never sufficient for EFT and surge
transients occurring in industrial environments. Therefore robust and reliable bus node design requires the use of
external transient protection devices.

Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high-
frequency layout techniques must be applied during PCB design.

In order for your PCB design to be successful start with the design of the protection circuit in mind.

1. Place the protection circuitry close to the bus connector to prevent noise transients from penetrating your
   board.
2. Use Vcc and ground planes to provide low-inductance. Note that high-frequency currents follow the path of
   least inductance and not the path of least impedance.
3. Design the protection components into the direction of the signal path. Do not force the transients currents to
   divert from the signal path to reach the protection device.
4. Apply 100-nF to 220-nF bypass capacitors as close as possible to the Vcc-pins of transceiver, UART,
   controller ICs on the board.
5. Use at least two vias for Vcc and ground connections of bypass capacitors and protection devices to
   minimize effective via-inductance.
6. Use 1-kΩ to 10-kΩ pullup or pulldown resistors for enable lines to limit noise currents in these lines during
   transient events.
7. Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified
   maximum voltage of the transceiver bus terminals. These resistors limit the residual clamping current into the
   transceiver and prevent it from latching up.
8. While pure TVS protection is sufficient for surge transients up to 1kV, higher transients require metal-oxide
   varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient
   blocking units (TBUs) that limit transient current to some 200 mA.
11.2 Layout Example

Figure 27. SN65HVD82 Layout Example
12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.1.2 Custom Design With WEBENCH® Tools

Click here to create a custom design using the SN65HVD82 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ($V_{IN}$), output voltage ($V_{OUT}$), and output current ($I_{OUT}$) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

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12.2 Community Resources

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among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help
solve problems with fellow engineers.

Design Support TI's Design Support Quickly find helpful E2E forums along with design support tools and
contact information for technical support.

12.3 Trademarks

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12.4 Electrostatic Discharge Caution

⚠️ These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam
during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — TI Glossary.
This glossary lists and explains terms, acronyms, and definitions.
13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
### PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
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<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>HVD82</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines “RoHS” to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, “RoHS” products are suitable for use in specified lead-free processes. TI may reference these types of products as “Pb-Free”.
- **RoHS Exempt**: TI defines “RoHS Exempt” to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green**: TI defines “Green” to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <1000ppm threshold. Antimony trioxide based flame retardants must also meet the <1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION

### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

### REEL DIMENSIONS

- **Reel Diameter**
- **Reel Width (W1)**

### Quadrant Assignments for Pin 1 Orientation in Tape

- **Q1**: Pocket Quadrant
- **Q2**: Pocket Quadrant
- **Q3**: Pocket Quadrant
- **Q4**: Pocket Quadrant

*All dimensions are nominal*

<table>
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<tr>
<th>Device</th>
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<th>SPQ</th>
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<th>B0  (mm)</th>
<th>K0  (mm)</th>
<th>P1  (mm)</th>
<th>W   (mm)</th>
<th>Pin1 Quadrant</th>
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</table>

*All dimensions are nominal*
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
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