- **Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days**
- **Wide Range of Supply Voltages Over Specified Temperature Range:**
  - **0°C to 70°C . . . 3 V to 16 V**
  - **−40°C to 85°C . . . 4 V to 16 V**
  - **−55°C to 125°C . . . 5 V to 16 V**
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix and I-Suffix Types)**
- **Low Noise . . . 68 nV/√Hz Typically at f = 1 kHz**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typ**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-In Latch-Up Immunity**

description

The TLC27L1 operational amplifier combines a wide range of input offset-voltage grades with low offset-voltage drift and high input impedance. In addition, the TLC27L1 is a low-bias version of the TLC271 programmable amplifier. These devices use the Texas Instruments silicon-gate LinCMOS™ technology, which provides offset-voltage stability far exceeding the stability available with conventional metal-gate processes.

Three offset-voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC27L1 (10 mV) to the TLC27L1B (2 mV) low-offset version. The extremely high input impedance and low bias currents, in conjunction with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available in LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC27L1. The devices also exhibit low-voltage single-supply operation, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input-voltage range includes the negative rail.

The device inputs and output are designed to withstand −100-mA surge currents without sustaining latch-up.

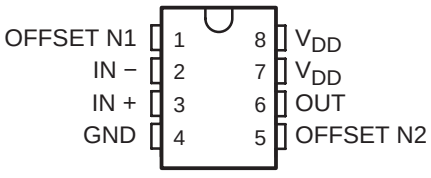
The TLC27L1 incorporates internal electrostatic-discharge (ESD) protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGE	
		SMALL OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	2 mV 5 mV 10 mV	TLC27L1BCD TLC27L1ACD TLC27L1CD	TLC27L1BCP TLC27L1ACP TLC27L1CP
−40°C to 85°C	2 mV 5 mV 10 mV	TLC27L1BID TLC27L1AID TLC27L1ID	TLC27L1BIP TLC27L1AIP TLC27L1IP
−55°C to 125°C	10 mV	TLC27L1MD	TLC27L1MP

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLC27L1BCDR).

D OR P PACKAGE
(TOP VIEW)



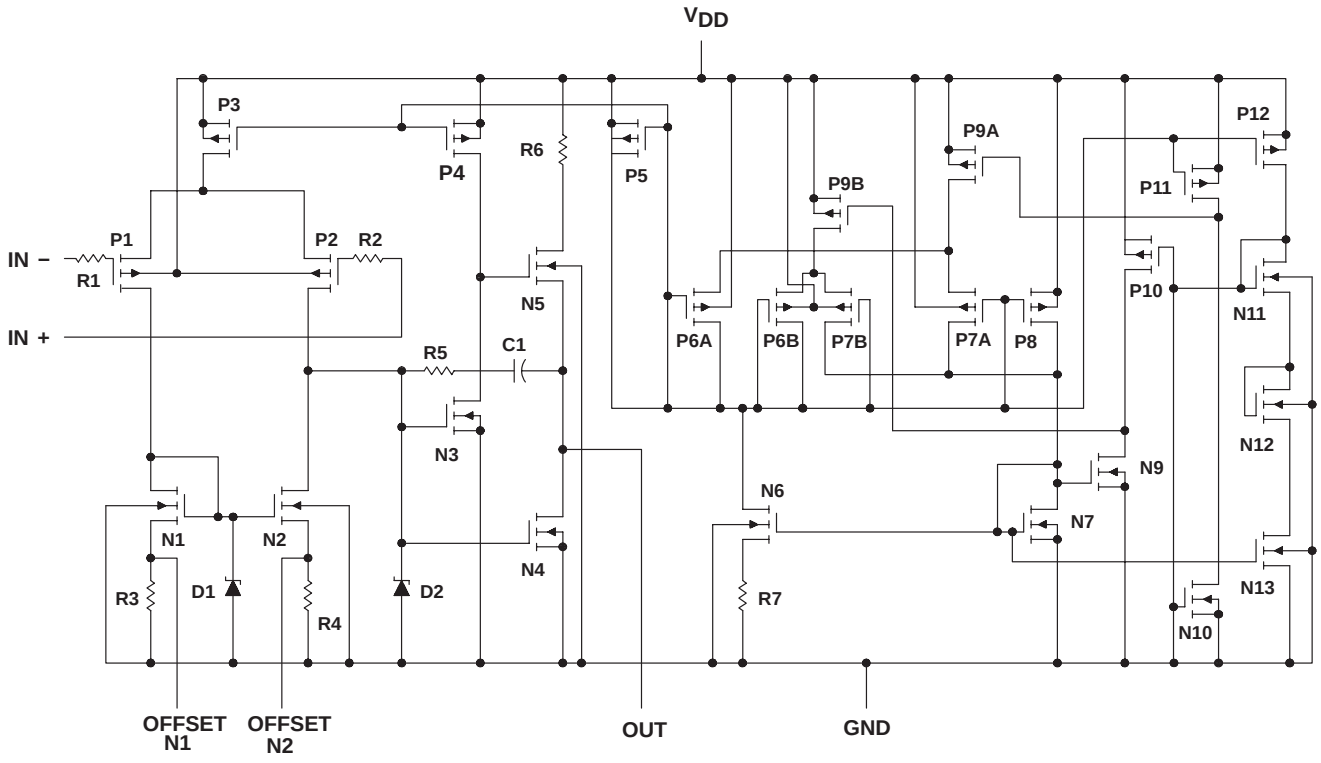
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LinCMOS is a trademark of Texas Instruments.

description (continued)

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

equivalent schematic



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Differential input voltage, V_{ID} (see Note 2) . . . . . $\pm V_{DD}$
Input voltage range, V_I (any input) . . . . . −0.3 V to V_{DD}
Input current, I_I . . . . . ±5 mA
Output current, I_O . . . . . ±30 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . . Unlimited
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: C suffix . . . . . 0°C to 70°C
I suffix . . . . . −40°C to 85°C
M suffix . . . . . −55°C to 125°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Case temperature for 60 seconds, T_C: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN−.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}		3	16	4	16	5	16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	−0.2	3.5	−0.2	3.5	0	3.5	V
	V_{DD} = 10 V	−0.2	8.5	−0.2	8.5	0	8.5	
Operating free-air temperature, T_A		0	70	−40	85	−55	125	°C

electrical characteristics at specified free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC27L1C, TLC27L1AC, TLC27L1BC						UNIT
					V_{DD} = 5 V			V_{DD} = 10 V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27L1C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_I = 1 MΩ	25°C		1.1	10		1.1	10	mV
				Full range			12			12	
		TLC27L1AC		25°C		0.9	5		0.9	5	
				Full range			6.5			6.5	
		TLC27L1BC		25°C		0.24	2		0.26	2	
				Full range			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.1			1		µV/°C
I_{IO}	Input offset current (see Note 4)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1	60		0.1	60	pA
				70°C		7	300		8	300	
I_{IB}	Input bias current (see Note 4)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.6	60		0.7	60	pA
				70°C		40	600		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8	8.9		V
				0°C	3	4.1		7.8	8.9		
				70°C	3	4.2		7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				0°C		0	50		0	50	
				70°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 1 MΩ, See Note 6	25°C	50	520		50	870		V/mV
				0°C	50	700		50	1030		
				70°C	50	380		50	660		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$min	25°C	65	94		65	97		dB
				0°C	60	95		60	97		
				70°C	60	95		60	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		70	97		dB
				0°C	60	97		60	97		
				70°C	60	98		60	98		
$I_{I(SEL)}$	Input current (BIAS SELECT)		$V_{I(SEL)} = V_{DD}$	25°C		65			95		nA
I_{DD}	Supply current		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$, No load	25°C		10	17		14	23	µA
				0°C		12	21		18	33	
				70°C		8	14		11	20	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

electrical characteristics at specified free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLC27L1I, TLC27L1AI, TLC27L1BI						UNIT
					V_{DD} = 5 V			V_{DD} = 10 V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27L1I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10		1.1	10	mV
				Full range			13			13	
		TLC27L1AI		25°C		0.9	5		0.9	5	
				Full range			7			7	
		TLC27L1BI		25°C		0.24	2		0.26	2	
				Full range			3.5			3.5	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.1			1		μV/°C
I_{IO}	Input offset current (see Note 4)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1	60		0.1	60	pA
				85°C		24	1000		26	1000	
I_{IB}	Input bias current (see Note 4)		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.6	60		0.7	60	pA
				85°C		200	2000		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3	4.1		8	8.9		V
				−40°C	3	4.1		7.8	8.9		
				85°C	3	4.2		7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				−40°C		0	50		0	50	
				85°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 1 MΩ See Note 6	25°C	50	520		50	870		V/mV
				−40°C	50	900		50	1550		
				85°C	50	330		50	585		
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$min	25°C	65	94		65	97		dB
				−40°C	60	95		60	97		
				85°C	60	95		60	98		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		70	97		dB
				−40°C	60	97		60	97		
				85°C	60	98		60	98		
$I_{I(SEL)}$	Input current (BIAS SELECT)		$V_{I(SEL)} = V_{DD}$	25°C		65			95		nA
I_{DD}	Supply current		$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$, No load	25°C		10	17		14	23	μA
				−40°C		16	27		25	43	
				85°C		17	13		10	18	

† Full range is −40 to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

electrical characteristics at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC27L1M						UNIT
				V_{DD} = 5 V			V_{DD} = 10 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10		1.1	10	mV
			Full range			12			12	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 125°C		1.4			1.4		µV/°C
I_{IO}	Input offset current (see Note 4)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1	60		0.1	60	pA
			125°C		1.4	15		1.8	15	nA
I_{IB}	Input bias current (see Note 4)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.6	60		0.7	60	pA
			125°C		9	35		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	0 to 4	−0.3 to 4.2		0 to 9	−0.3 to 9.2		V
			Full range	0 to 3.5			0 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L= 1 MΩ	25°C	3.2	4.1		8	8.9		V
			−55°C	3	4.1		7.8	8.8		
			125°C	3	4.2		7.8	9		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
			−55°C		0	50		0	50	
			125°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification	R_L= 1 MΩ, See Note 6	25°C	50	520		50	870		V/mV
			−55°C	25	1000		25	1775		
			125°C	25	200		25	380		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C	65	94		65	97		dB
			−55°C	60	95		60	97		
			125°C	60	85		60	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		70	97		dB
			−55°C	60	97		60	97		
			125°C	60	98		60	98		
$I_{I(SEL)}$	Input current (BIAS SELECT)	$V_{I(SEL)} = V_{DD}$	25°C		65			95		nA
I_{DD}	Supply current	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$, No load	25°C		10	17		14	23	µA
			−55°C		17	30		28	48	
			125°C		7	12		9	15	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC27L1C, TLC27L1AC, TLC27L1BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 33	$V_{I(PP)}$ = 1 V	25°C		0.03		V/μs
				0°C		0.04		
				70°C		0.03		
			$V_{I(PP)}$ = 2.5 V	25°C		0.03		
				0°C		0.03		
				70°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 34	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 1 MΩ,	C_L = 20 pF, See Figure 33	25°C		5		kHz
				0°C		6		
				70°C		4.5		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 35	C_L = 20 pF,	25°C		85		kHz
				0°C		100		
				70°C		65		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 35	25°C		34°		
				0°C		36°		
				70°C		30°		

operating characteristics at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC27L1C, TLC27L1AC, TLC27L1BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 33	$V_{I(PP)}$ = 1 V	25°C		0.05		V/μs
				0°C		0.05		
				70°C		0.04		
			$V_{I(PP)}$ = 5.5 V	25°C		0.04		
				0°C		0.05		
				70°C		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 34	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 1 MΩ,	C_L = 20 pF, See Figure 33	25°C		1		kHz
				0°C		1.3		
				70°C		0.9		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 35	C_L = 20 pF,	25°C		110		kHz
				0°C		125		
				70°C		90		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 35	25°C		38°		
				0°C		40°		
				70°C		34°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC27L1I, TLC27L1AI, TLC27L1BI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 33	$V_{I(PP)}$ = 1 V	25°C		0.03		V/μs
				–40°C		0.04		
				85°C		0.03		
			$V_{I(PP)}$ = 2.5 V	25°C		0.03		
				–40°C		0.04		
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 34	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 1 MΩ,	C_L = 20 pF, See Figure 33	25°C		5		kHz
				–40°C		7		
				85°C		4		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 35	C_L = 20 pF,	25°C		85		MHz
				–40°C		130		
				85°C		55		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 35	25°C		34°		
				–40°C		38°		
				85°C		28°		

operating characteristics at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC27L1C, TLC27L1AC, TLC27L1BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 33	$V_{I(PP)}$ = 1 V	25°C		0.05		V/μs
				–40°C		0.06		
				85°C		0.03		
			$V_{I(PP)}$ = 5.5 V	25°C		0.04		
				–40°C		0.05		
				85°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 34	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 1 MΩ,	C_L = 20 pF, See Figure 33	25°C		1		kHz
				–40°C		1.4		
				85°C		0.8		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 35	C_L = 20 pF,	25°C		110		MHz
				–40°C		155		
				85°C		80		
ϕ_m	Phase margin	V_I = 10 mV,I C_L = 20 pF,	f = B_1, See Figure 35	25°C		38°		
				–40°C		42°		
				85°C		32°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC27L1M			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 33	$V_{I(PP)}$ = 1 V	25°C		0.03		V/μs
				−55°C		0.04		
				125°C		0.02		
			$V_{I(PP)}$ = 2.5 V	25°C		0.03		
				−55°C		0.04		
				125°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 34	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 1 MΩ,	C_L = 20 pF, See Figure 33	25°C		5		kHz
				−55°C		8		
				125°C		3		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 35	C_L = 20 pF,	25°C		85		kHz
				−55°C		140		
				125°C		45		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 35	25°C		34°		
				−55°C		39°		
				125°C		25°		

operating characteristics at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC27L1M			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 33	$V_{I(PP)}$ = 1 V	25°C		0.05		V/μs
				−55°C		0.06		
				125°C		0.03		
			$V_{I(PP)}$ = 5.5 V	25°C		0.04		
				−55°C		0.06		
				125°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 34	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 1 MΩ,	C_L = 20 pF, See Figure 33	25°C		1		kHz
				−55°C		1.5		
				125°C		0.7		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 35	C_L = 20 pF,	25°C		110		kHz
				−55°C		165		
				125°C		70		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 35	25°C		38°		
				−55°C		43°		
				125°C		29°		

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	1, 2
α_{VIO}	Temperature coefficient	Distribution	3, 4
V_{OH}	High-level output voltage	vs High-level output current vs Supply voltage vs Free-air temperature	5, 6 7 8
V_{OL}	Low-level output voltage	vs Common-mode input voltage vs Differential input voltage vs Free-air temperature vs Low-level output current	9, 10 11 12 13, 14
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage vs Free-air temperature vs Frequency	15 16 27, 28
I_{IB}	Input bias current	vs Free-air temperature	17
I_{IO}	Input offset current	vs Free-air temperature	17
V_I	Maximum input voltage	vs Supply voltage	18
I_{DD}	Supply current	vs Supply voltage vs Free-air temperature	19 20
SR	Slew rate	vs Supply voltage vs Free-air temperature	21 22
	Bias-select current	vs Supply voltage	23
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	24
B_1	Unity-gain bandwidth	vs Free-air temperature vs Supply voltage	25 26
ϕ_m	Phase margin	vs Supply voltage vs Free-air temperature vs Capacitive load	29 30 31
V_n	Equivalent input noise voltage	vs Frequency	32
	Phase shift	vs Frequency	27, 28

TYPICAL CHARACTERISTICS†

**DISTRIBUTION OF TLC27L1
INPUT OFFSET VOLTAGE**

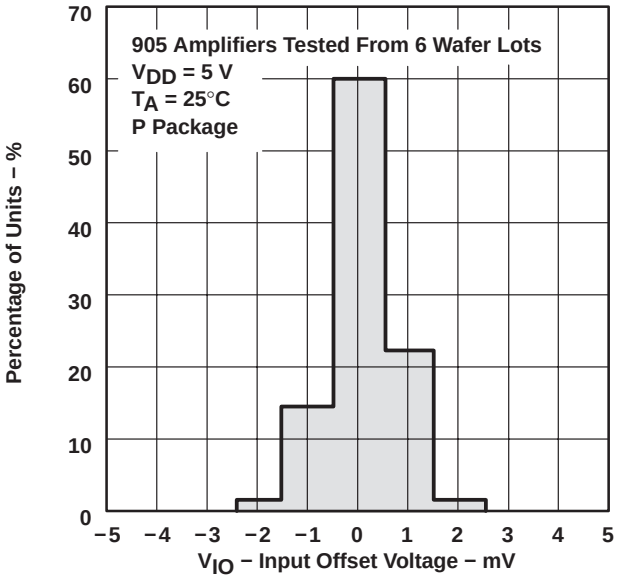


Figure 1

**DISTRIBUTION OF TLC27L1
INPUT OFFSET VOLTAGE**

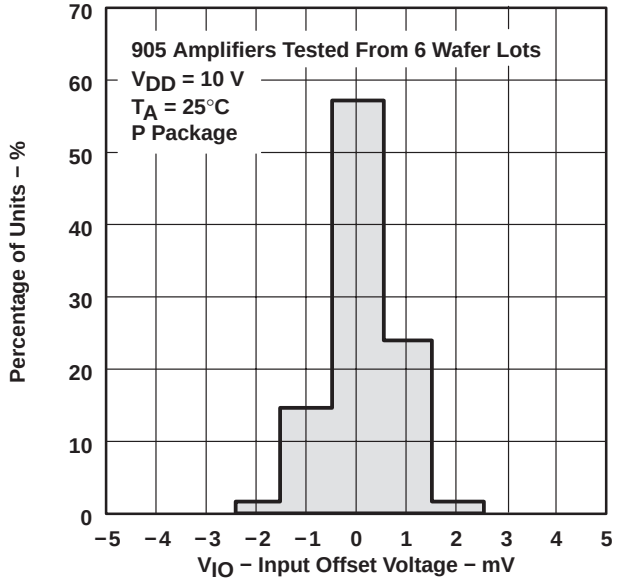


Figure 2

**DISTRIBUTION OF TLC27L1
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT**

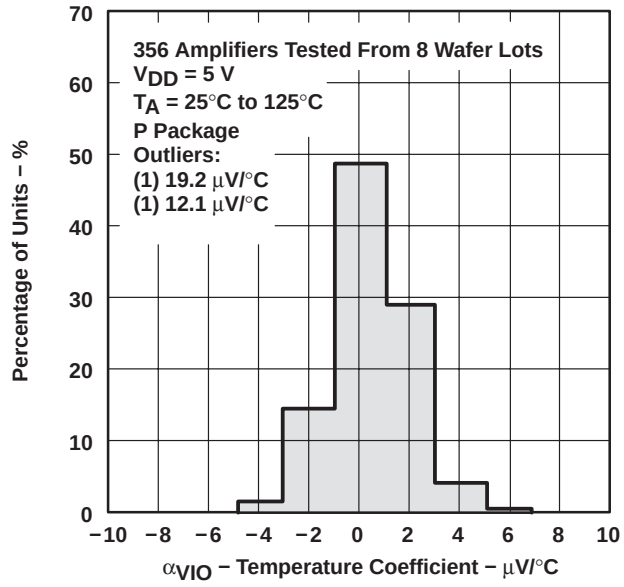


Figure 3

**DISTRIBUTION OF TLC27L1
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT**

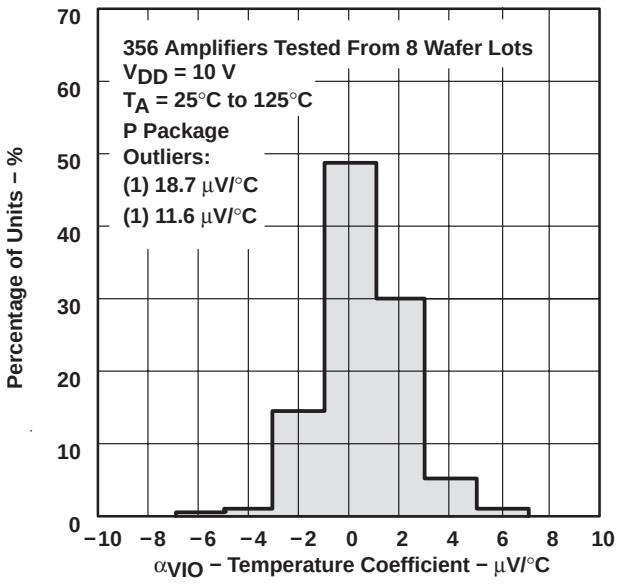


Figure 4

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

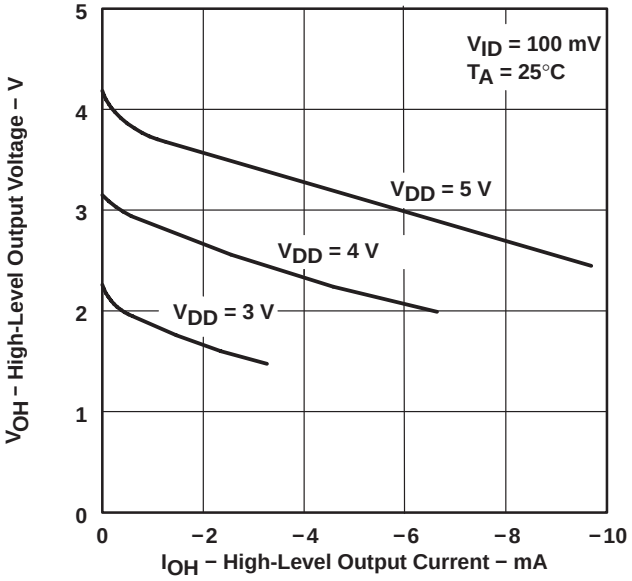


Figure 5

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

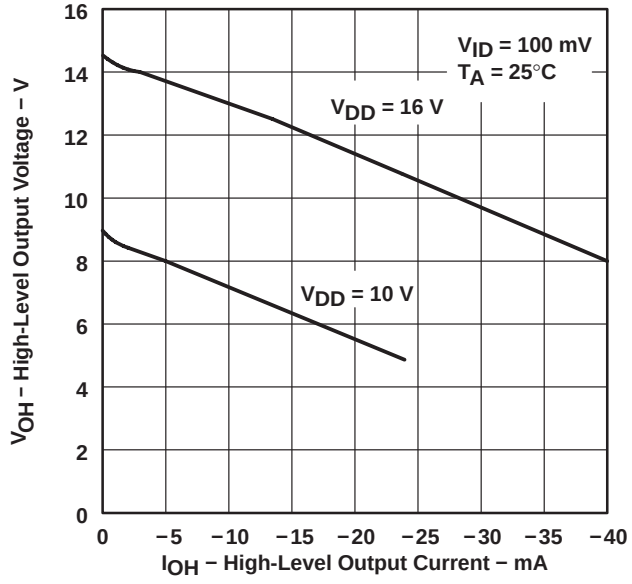


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

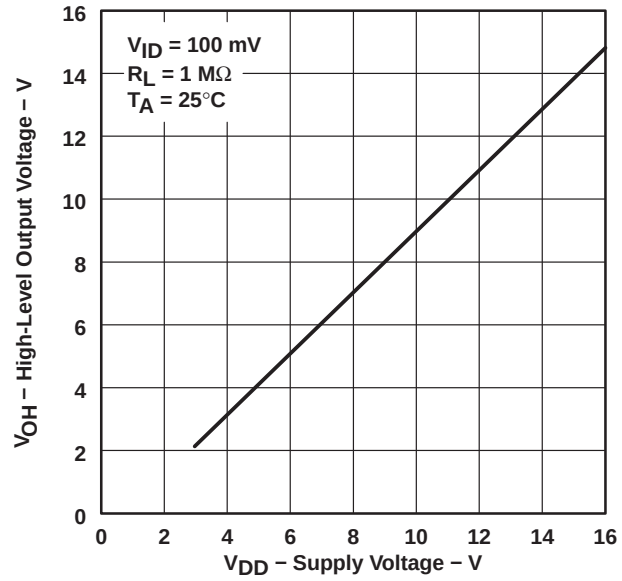


Figure 7

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

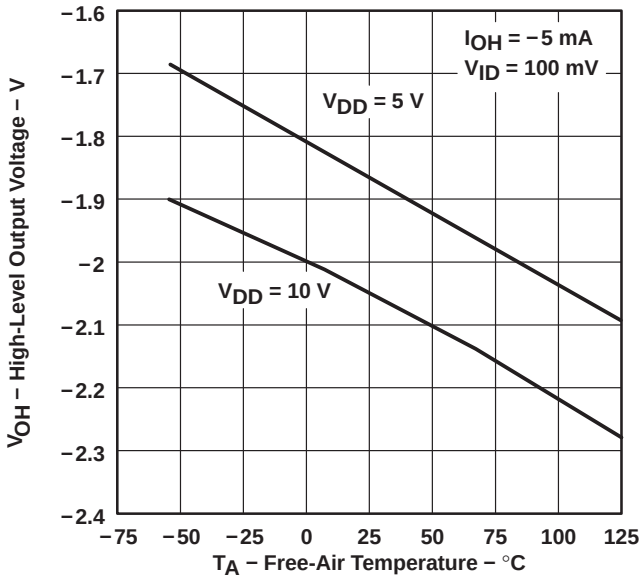


Figure 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

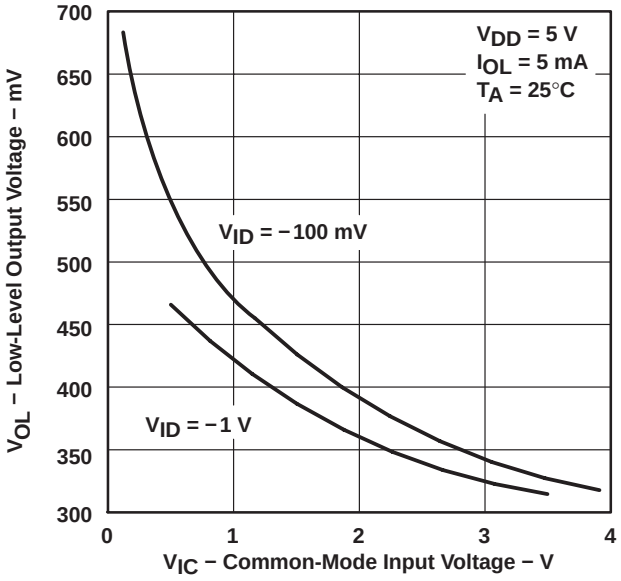


Figure 9

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

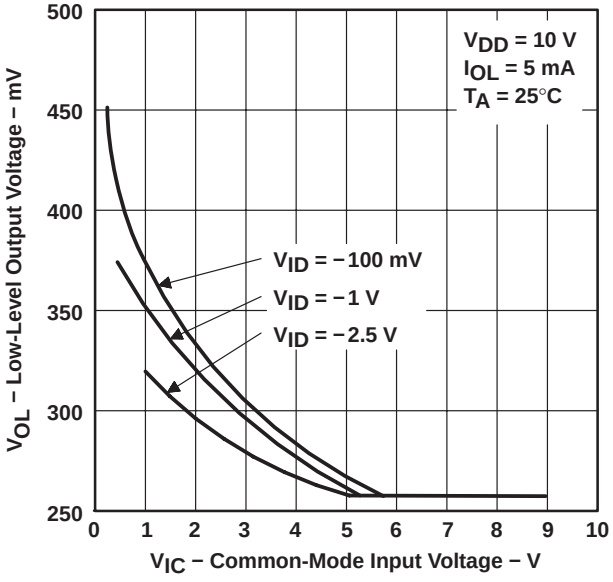


Figure 10

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

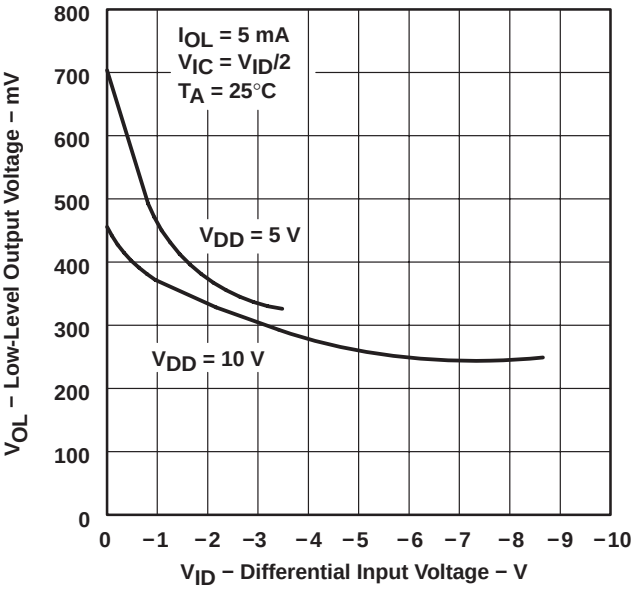


Figure 11

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

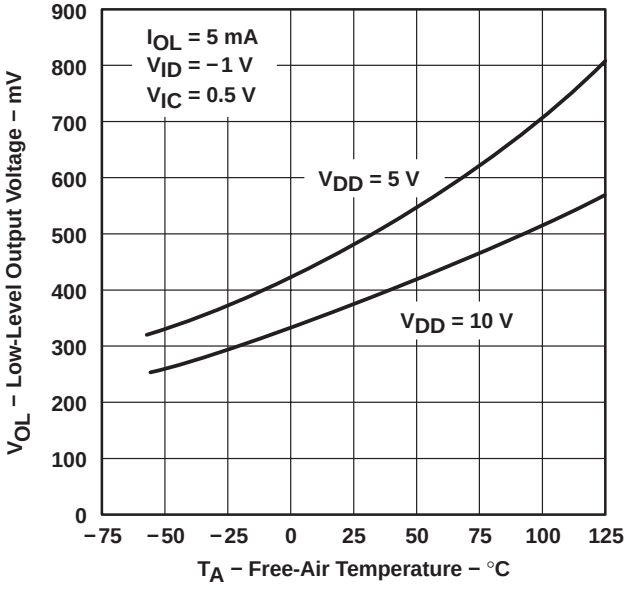


Figure 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

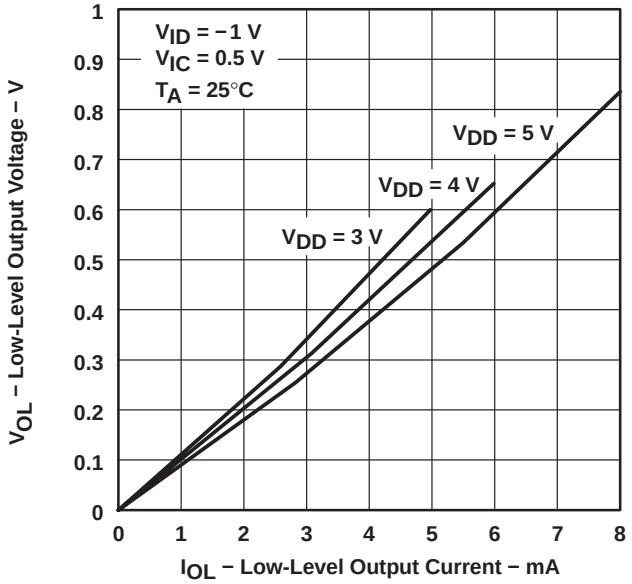


Figure 13

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

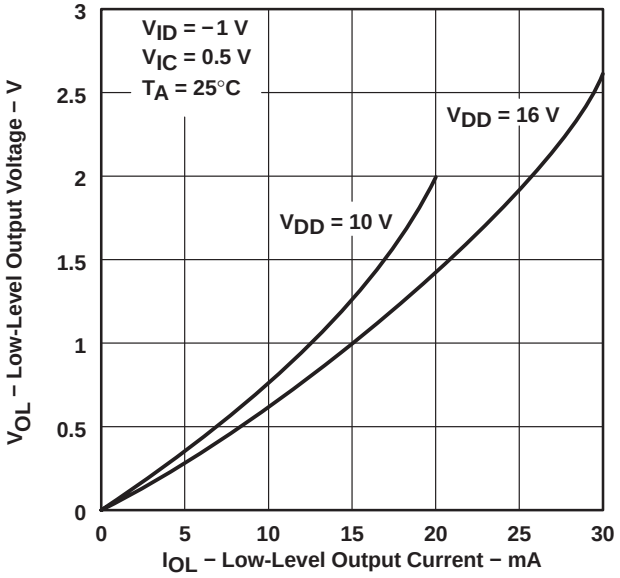


Figure 14

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

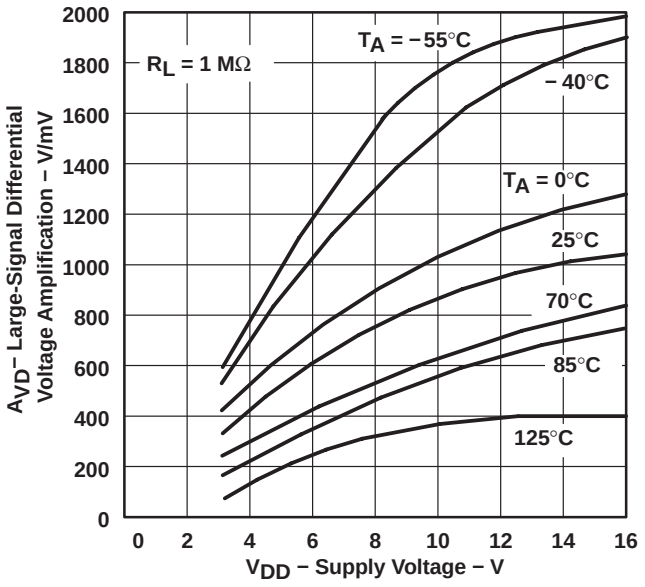


Figure 15

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

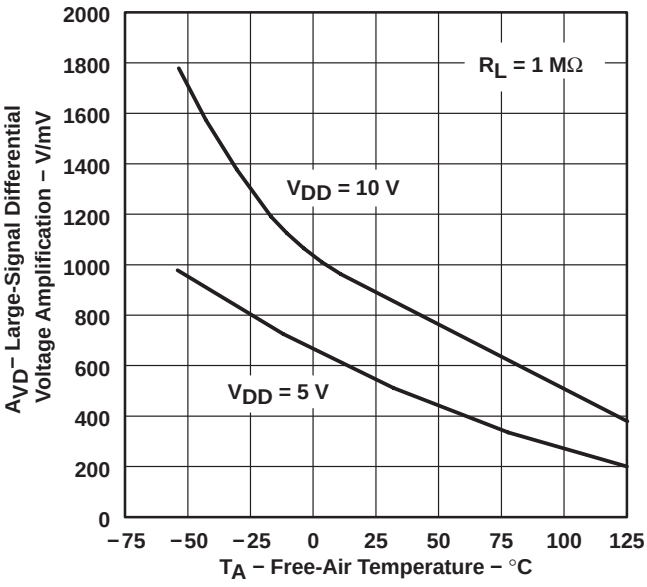
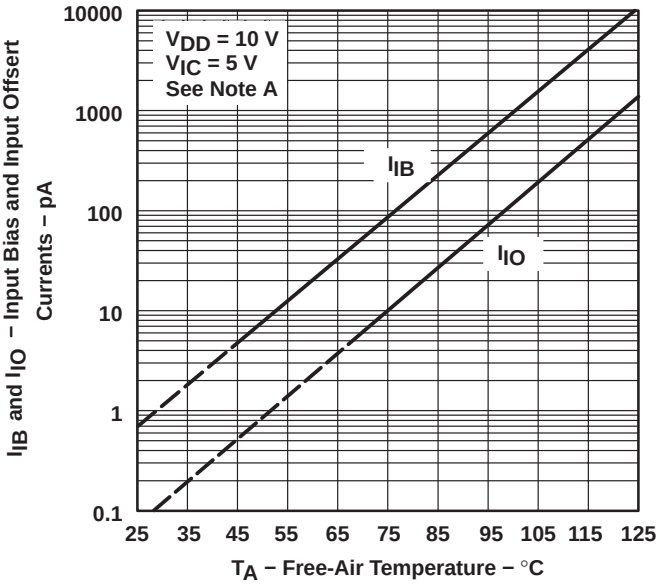


Figure 16

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS AND INPUT OFFSET CURRENTS vs FREE-AIR TEMPERATURE



NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 17

MAXIMUM INPUT VOLTAGE vs SUPPLY VOLTAGE

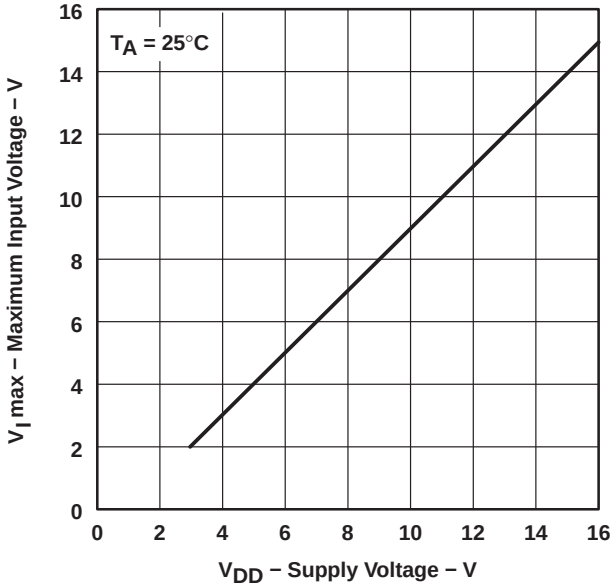


Figure 18

SUPPLY CURRENT vs SUPPLY VOLTAGE

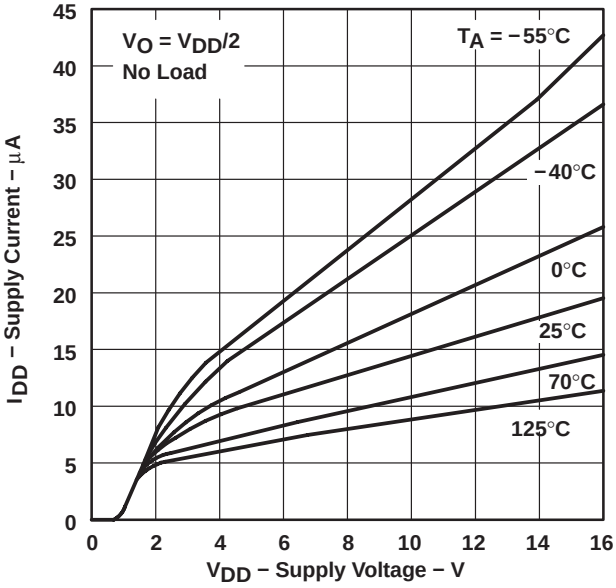


Figure 19

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

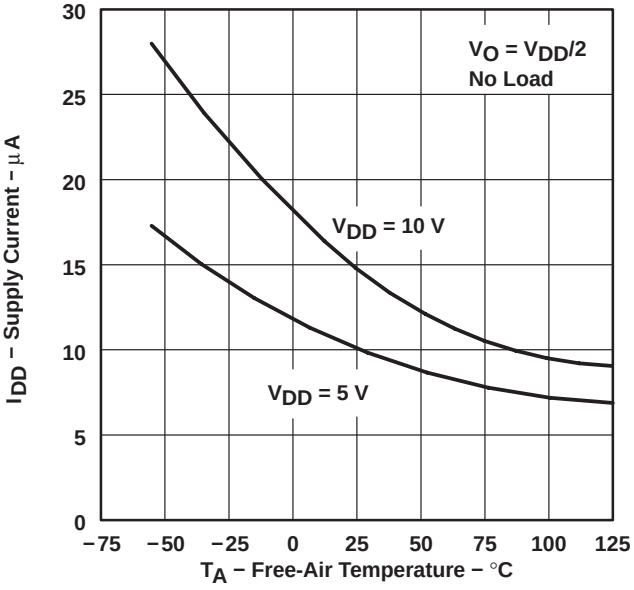


Figure 20

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SLEW RATE vs SUPPLY VOLTAGE

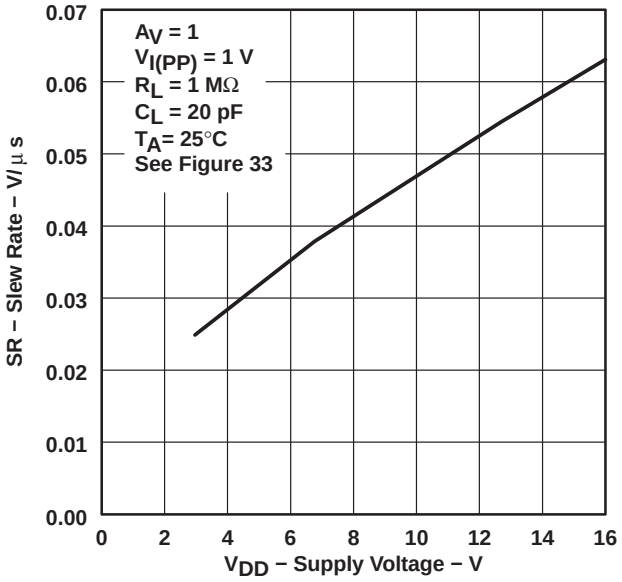


Figure 21

SLEW RATE vs FREE-AIR TEMPERATURE

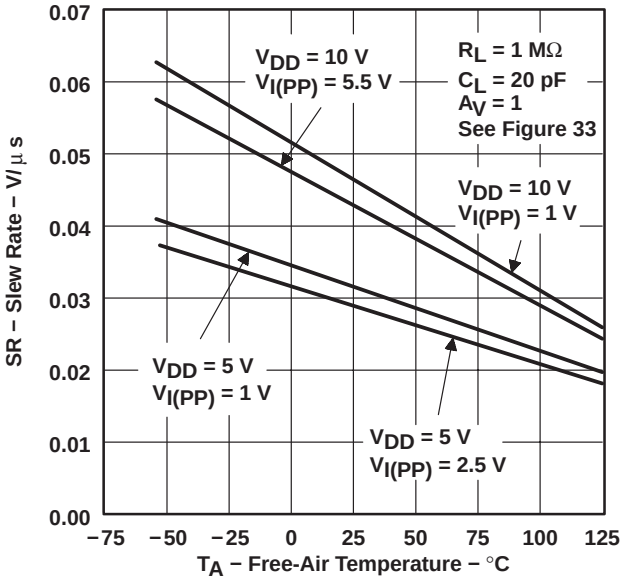


Figure 22

BIAS-SELECT CURRENT vs SUPPLY VOLTAGE

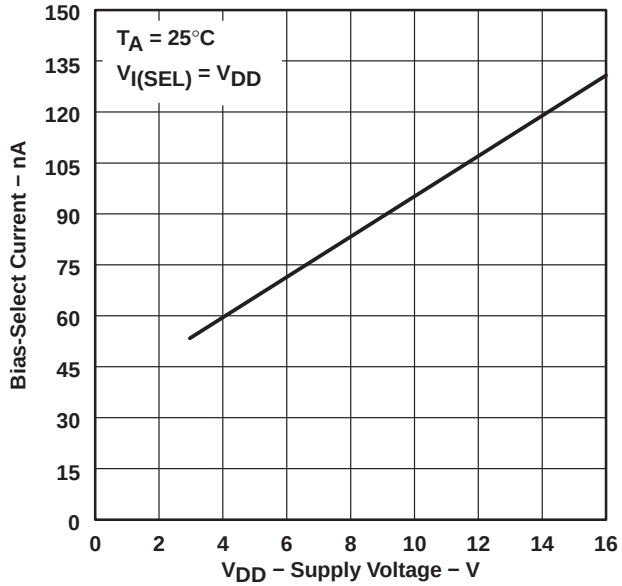


Figure 23

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

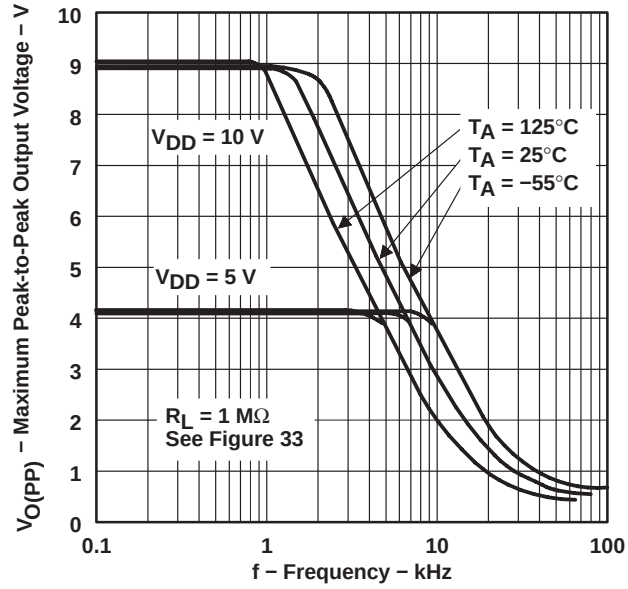


Figure 24

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH vs FREE-AIR TEMPERATURE

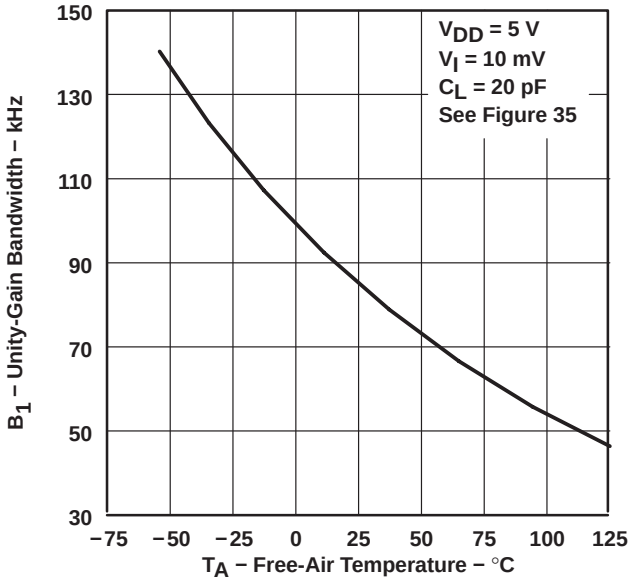


Figure 25

UNITY-GAIN BANDWIDTH vs SUPPLY VOLTAGE

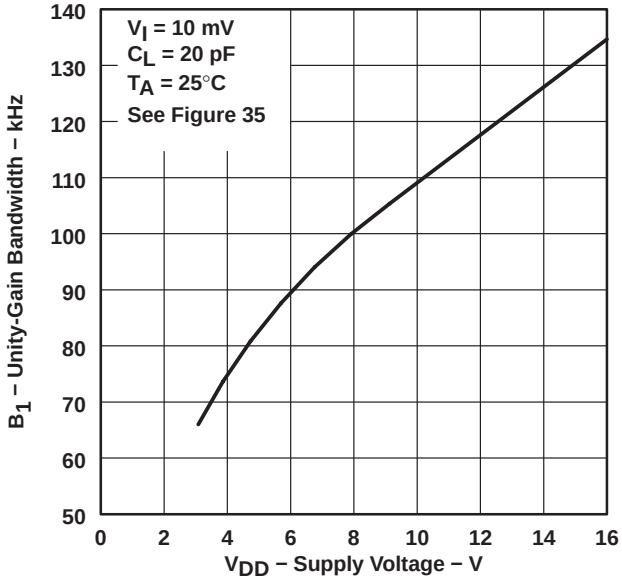


Figure 26

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

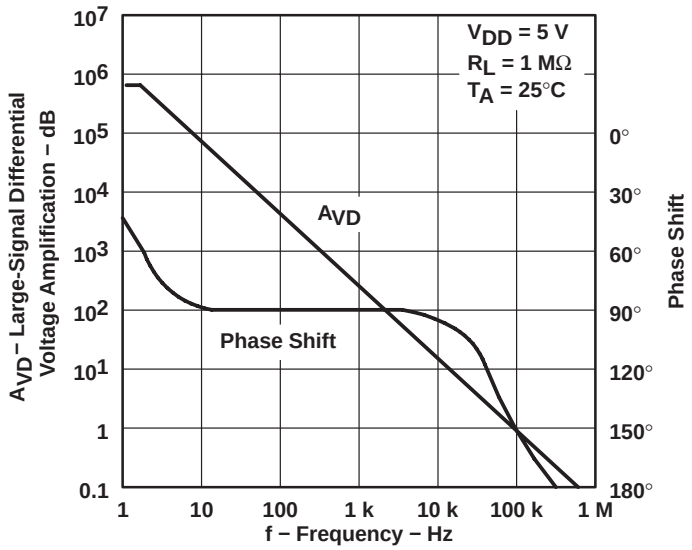


Figure 27

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

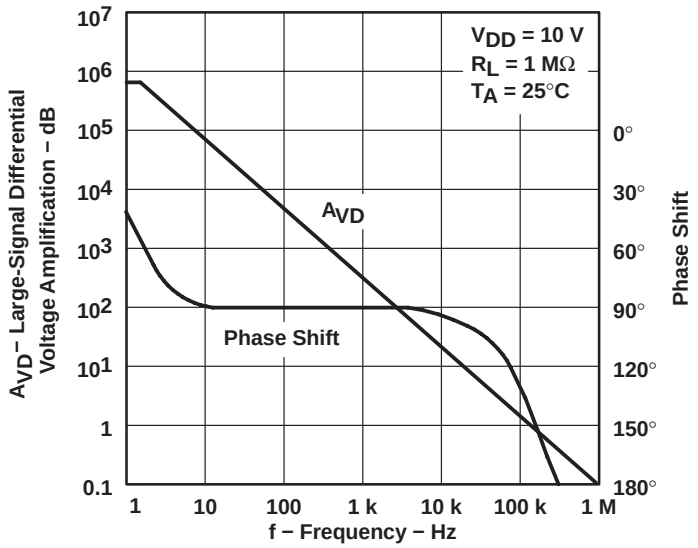


Figure 28

PHASE MARGIN vs SUPPLY VOLTAGE

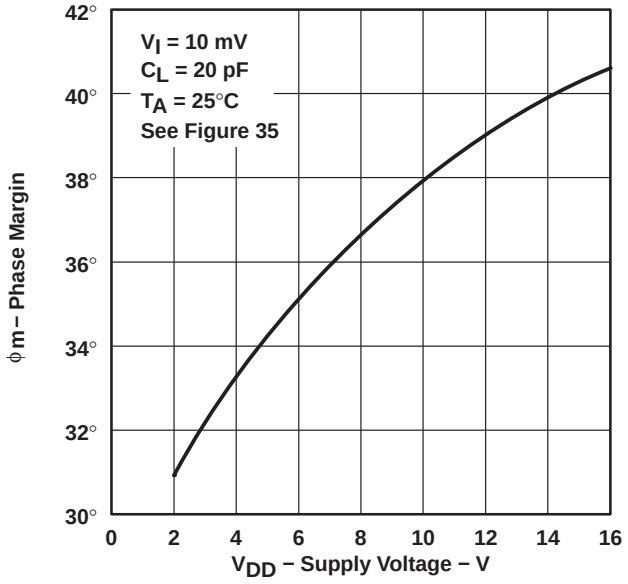


Figure 29

PHASE MARGIN vs FREE-AIR TEMPERATURE

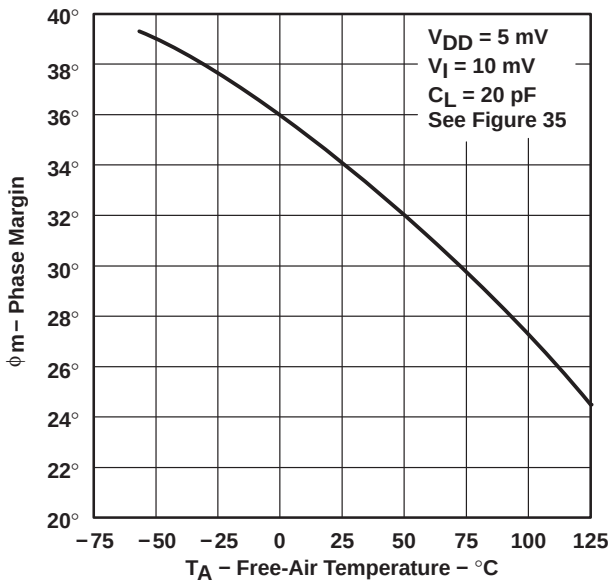


Figure 30

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

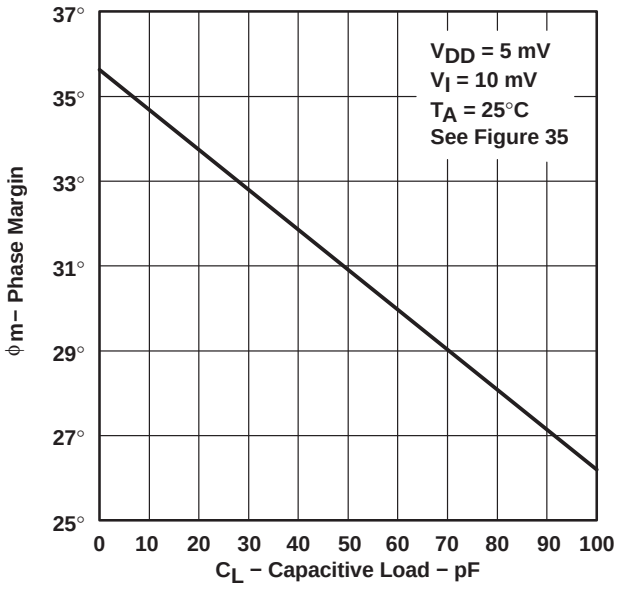


Figure 31

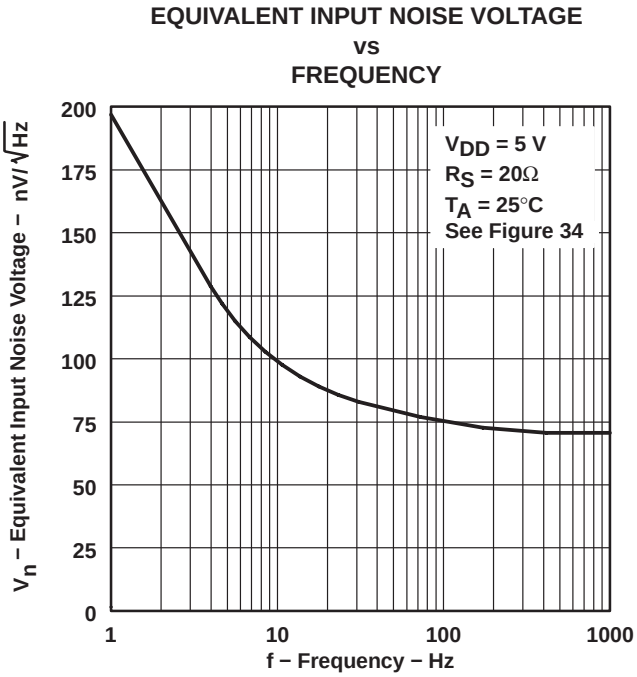


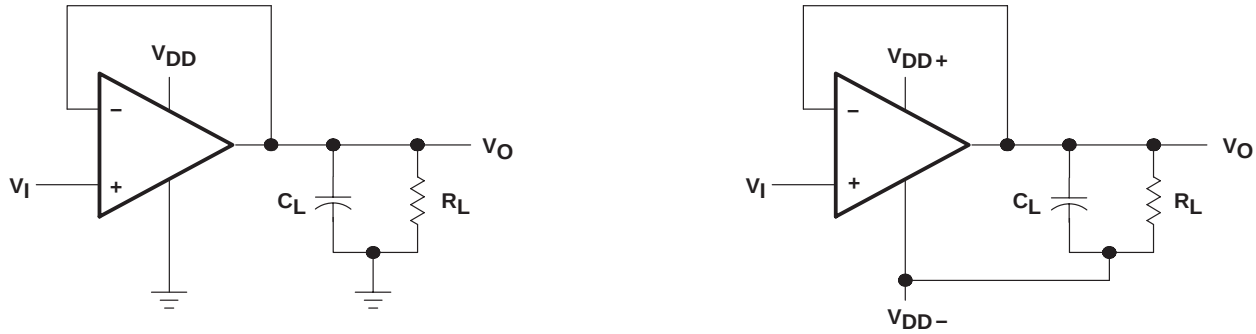
Figure 32

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLC27L1 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.



(a) SINGLE SUPPLY

(b) SPLIT SUPPLY

Figure 33. Unity-Gain Amplifier

PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits (continued)

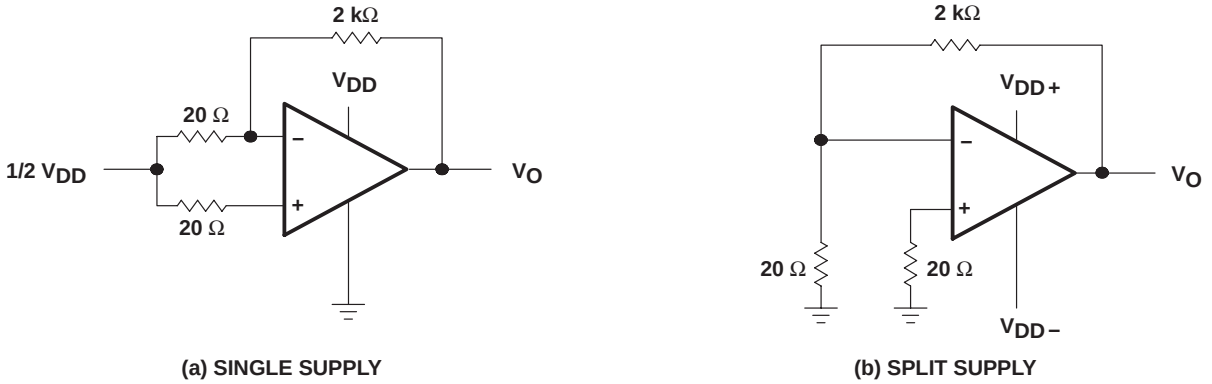


Figure 34. Noise-Test Circuit

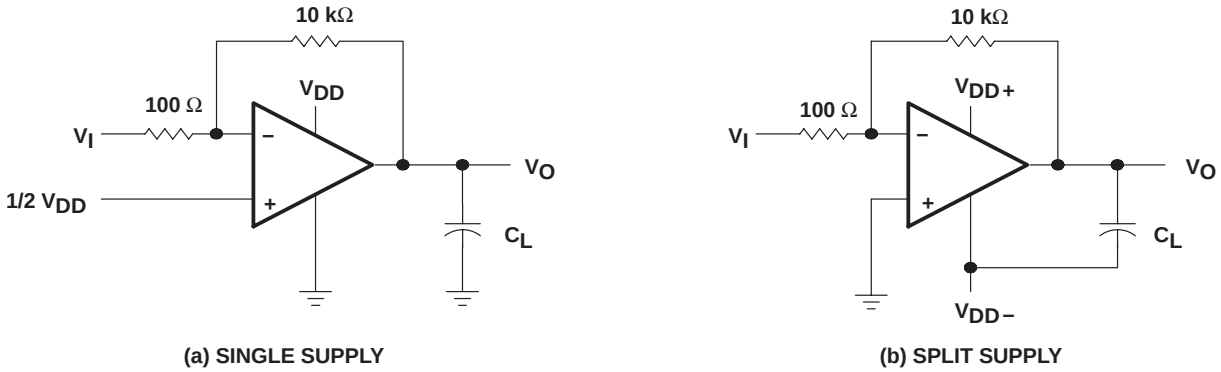


Figure 35. Gain-of-100 Inverting Amplifier

input bias current

Due to the high input impedance of the TLC27L1 operational amplifiers, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 36). Leakages that would otherwise flow to the inputs are shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias-current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

One word of caution: many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

PARAMETER MEASUREMENT INFORMATION

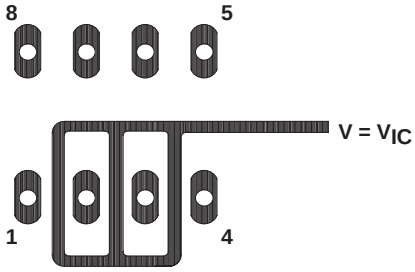


Figure 36. Isolation Metal Around Device Inputs (JG and P packages)

low-level output voltage

To obtain low-supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. When conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

input offset-voltage temperature coefficient

Erroneous readings often result from attempts to measure the temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset-voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance which can cause erroneous input offset-voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Since there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit in Figure 33. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 37). A square wave allows a more accurate determination of the point at which the maximum peak-to-peak output is reached.

PARAMETER MEASUREMENT INFORMATION

full-power response (continued)

(a) f = 100 Hz (b) B_{OM} > f > 100 Hz (c) f = B_{OM} (d) f > B_{OM}

Figure 37. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices, and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

APPLICATION INFORMATION

single-supply operation

While the TLC27L1 performs well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

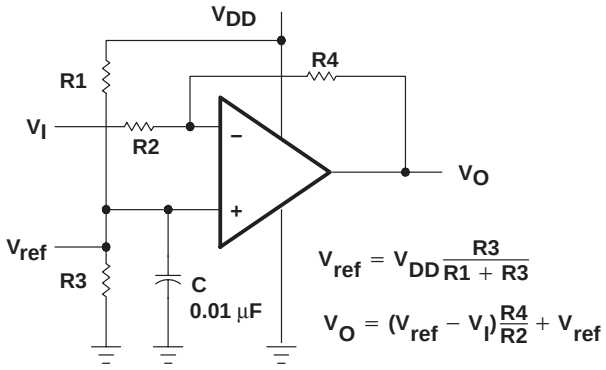


Figure 38. Inverting Amplifier With Voltage Reference

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low-input bias-current consumption of the TLC27L1 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC27L1 works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.

APPLICATION INFORMATION

single-supply operation (continued)

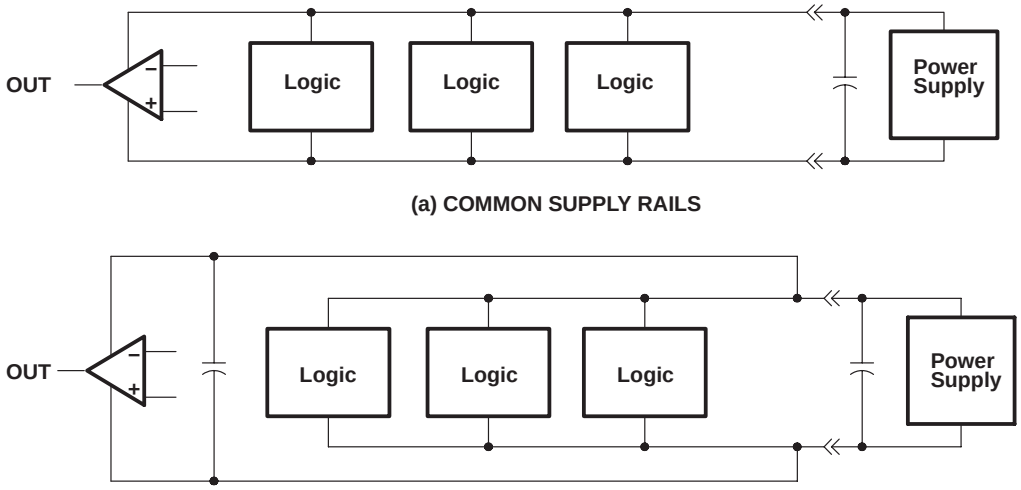


Figure 39. Common Versus Separate Supply Rails

input offset voltage nulling

The TLC27L1 offers external input-offset null control. Nulling of the input-offset voltage may be achieved by adjusting a 25-kΩ potentiometer connected between the offset null terminals with the wiper connected as shown in Figure 40. Total nulling may not be possible.

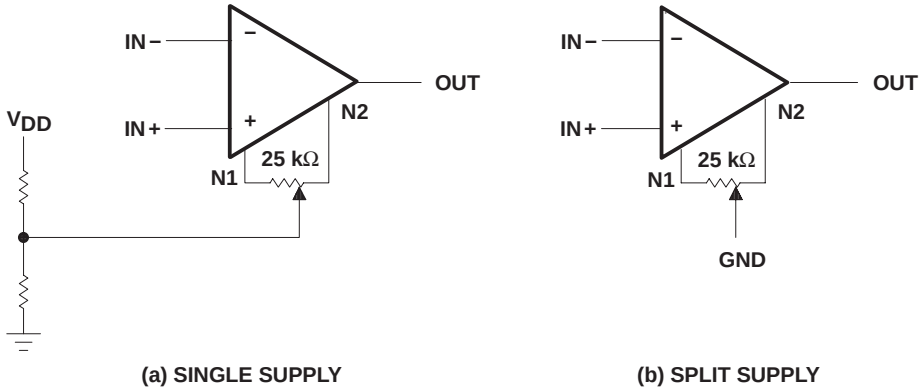


Figure 40. Input Offset-Voltage Null Circuit

input characteristics

The TLC27L1 is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at V_{DD} − 1 V at T_A = 25°C and at V_{DD} − 1.5 V at all other temperatures.

APPLICATION INFORMATION

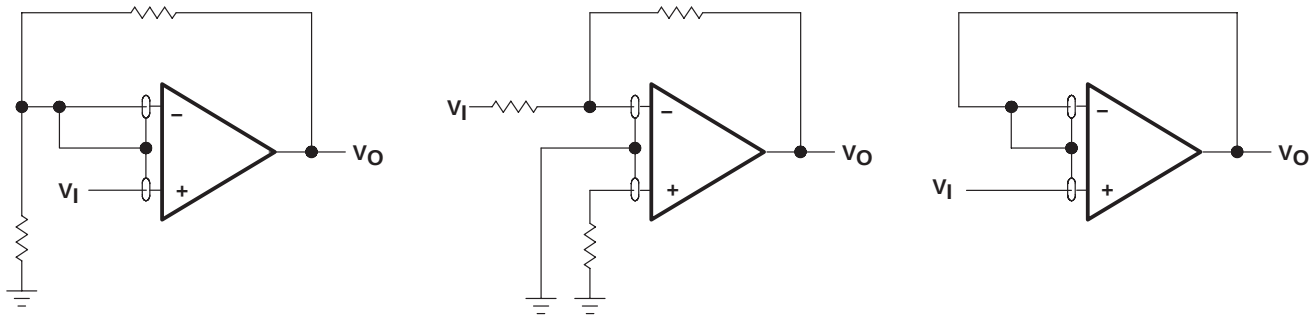
input characteristics (continued)

The use of the polysilicon-gate process and the careful input circuit design gives the TLC27L1 very good input offset-voltage drift characteristics relative to conventional metal-gate processes. Offset-voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset-voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias-current requirements, the TLC27L1 is well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias-current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 36 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 41).

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low-input bias-current requirements of the TLC27L1 results in a very-low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

Figure 41. Guard-Ring Schemes

APPLICATION INFORMATION

feedback

Operational amplifier circuits almost always employ feedback, and since feedback is the first prerequisite for oscillation, a little caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 42). The value of this capacitor is optimized empirically.

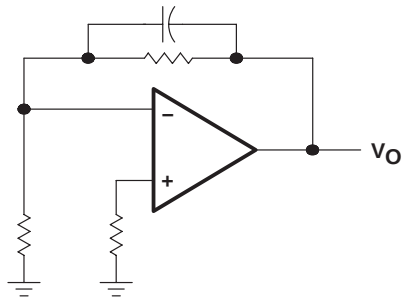


Figure 42. Compensation for Input Capacitance

electrostatic discharge protection

The TLC27L1 incorporates an internal ESD protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC27L1 inputs and output were designed to withstand −100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established when latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

APPLICATION INFORMATION

output characteristics

The output stage of the TLC27L1 is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage (see Figure 43).

All operating characteristics of the TLC27L1 were measured using a 20-pF load. The devices drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 44). In many cases, adding some compensation in the form of a series resistor in the feedback loop alleviates the problem.

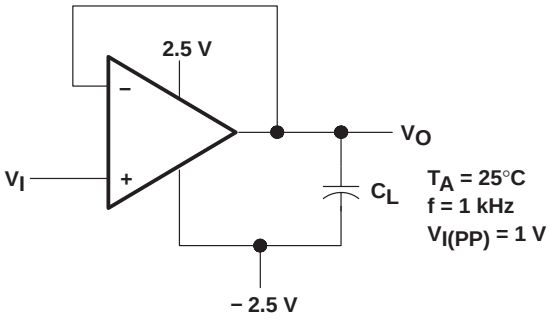
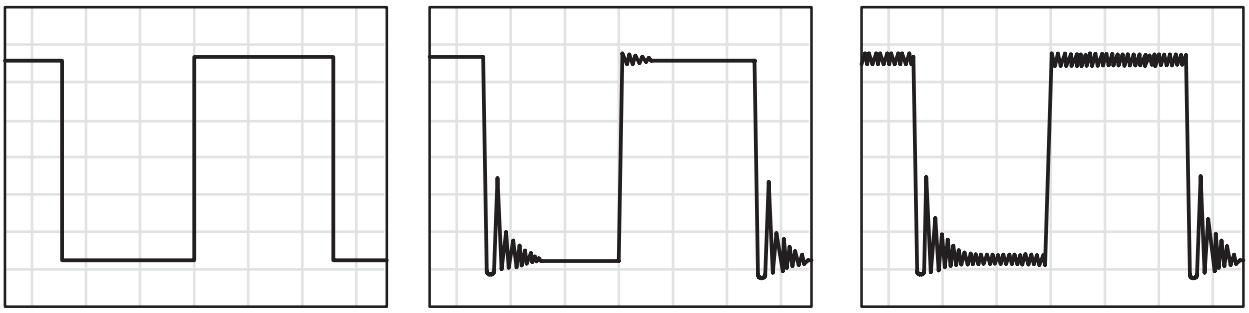


Figure 43. Test Circuit for Output Characteristics

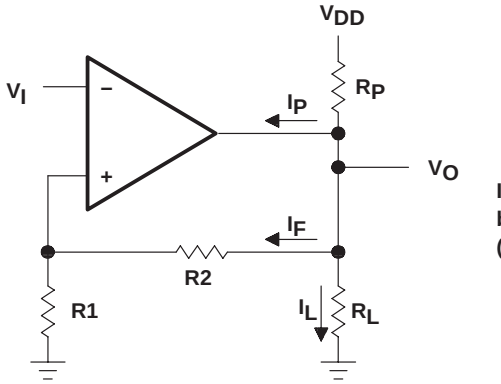


(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 260 pF, R_L = NO LOAD (c) C_L = 310 pF, R_L = NO LOAD

Figure 44. Effect of Capacitive Loads in Low-Bias Mode

Although the TLC27L1 possesses excellent high-level output voltage and current capability, methods are available for boosting this capability, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 45). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor, N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0 V at the output occurs. Secondly, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

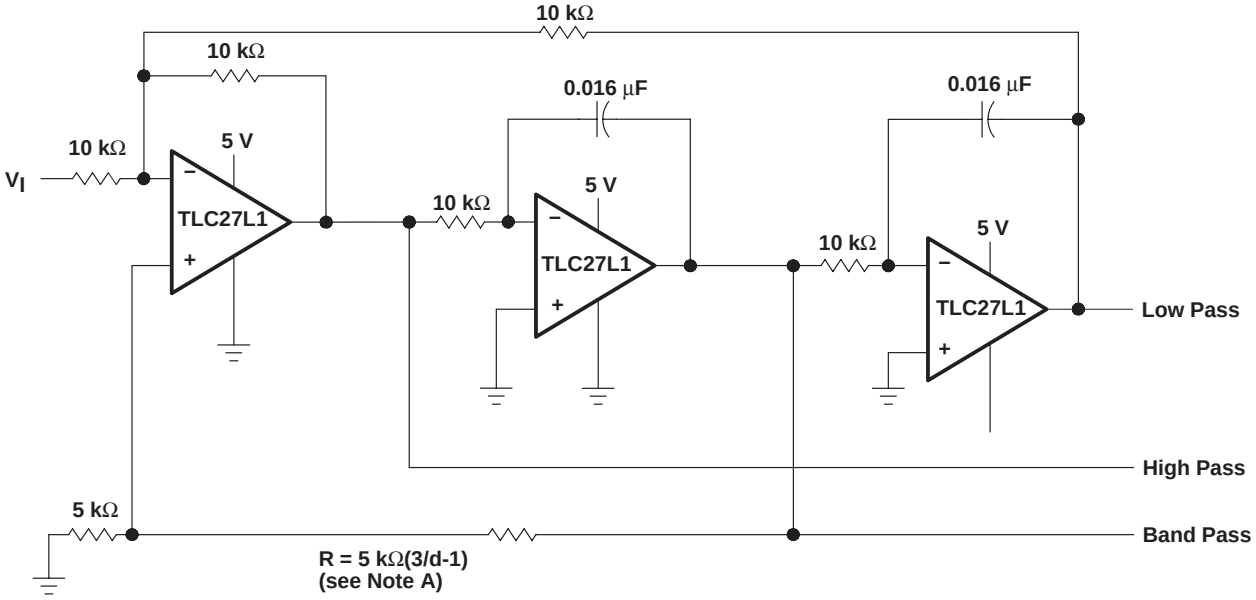
APPLICATION INFORMATION



$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pullup current required by the operational amplifier (typically 500 mA)

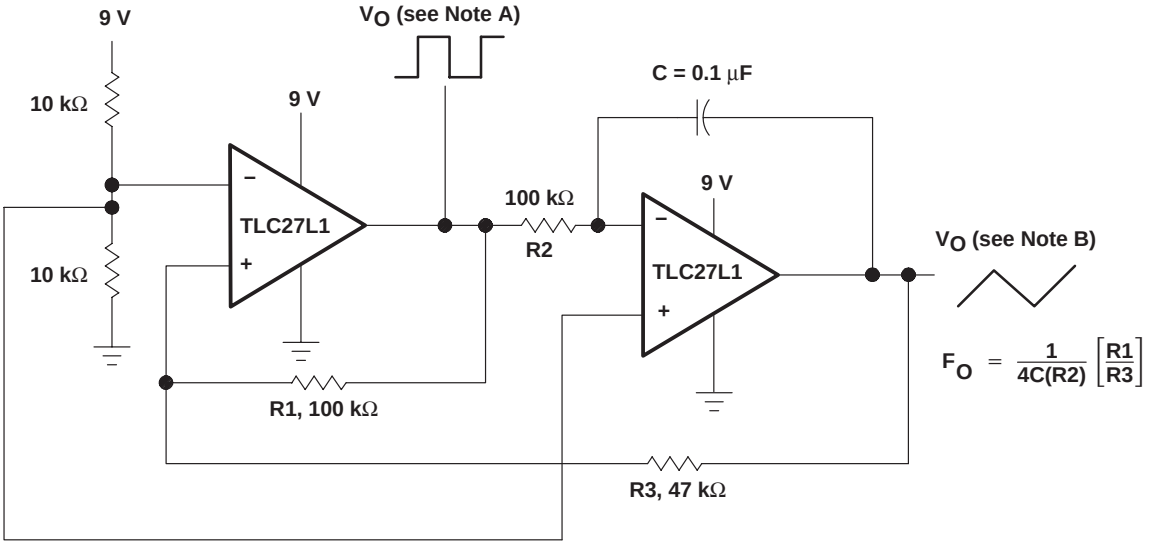
Figure 45. Resistive Pullup to Increase V_{OH}



NOTE A: d = damping factor, I/O

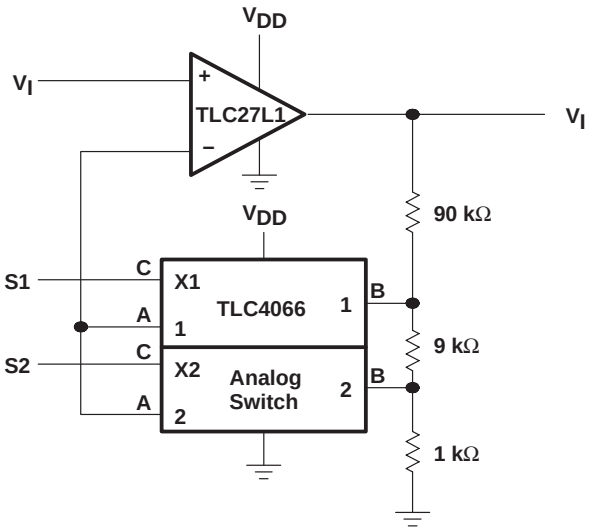
Figure 46. State-Variable Filter

APPLICATION INFORMATION



NOTES: A. $V_{O(PP)}$ = 8 V
B. $V_{O(PP)}$ = 4 V

Figure 47. Single-Supply Function Generator



Select	S_1	S_2
A_V	10	100

NOTE A: V_{DD} = 5 V to 12 V

Figure 48. Amplifier With Digital-Gain Selection

APPLICATION INFORMATION

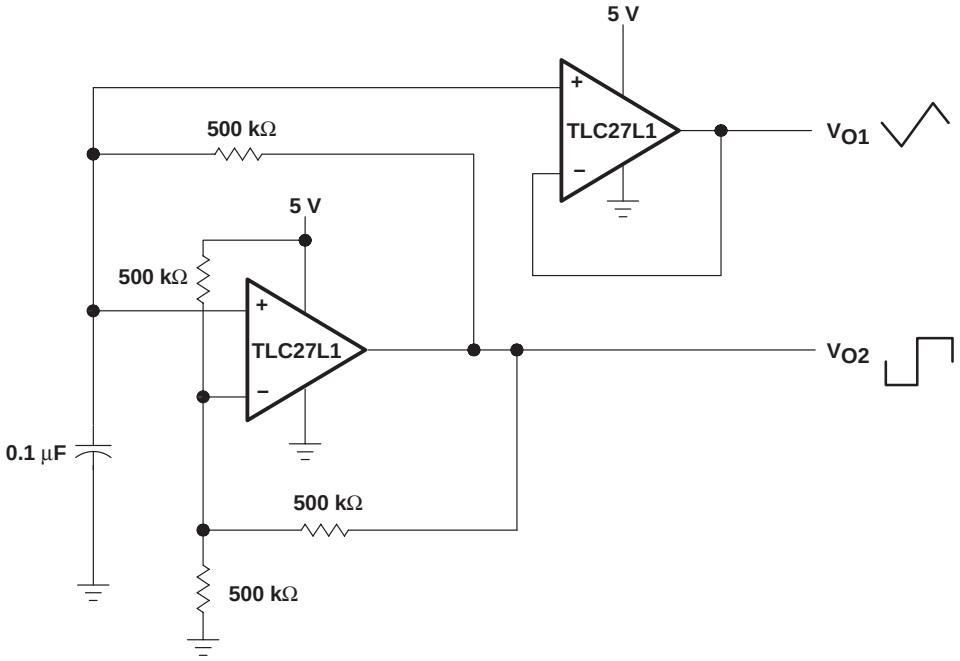
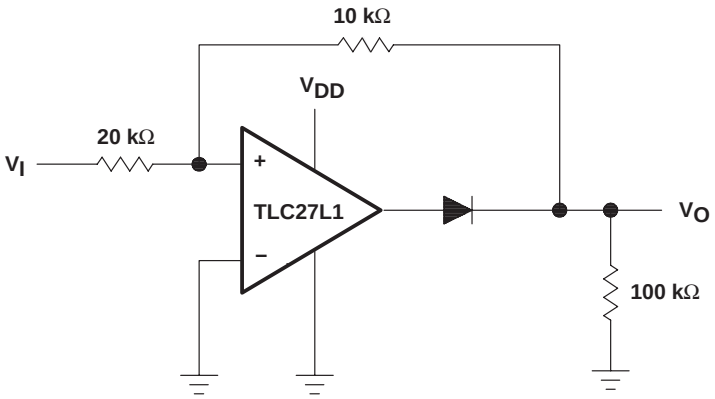


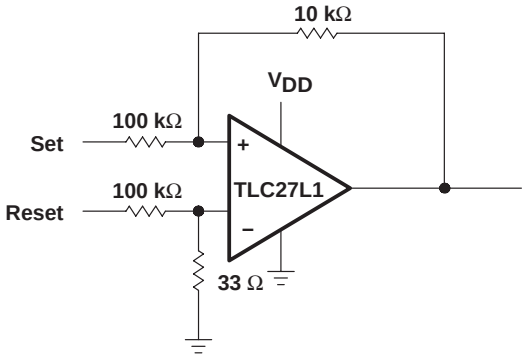
Figure 49. Multivibrator



NOTE A: V_{DD} = 5 V to 16 V

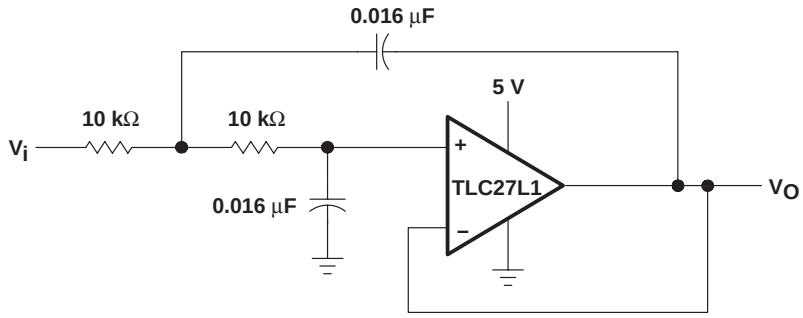
Figure 50. Full-Wave Rectifier

APPLICATION INFORMATION



NOTE A: V_{DD} = 5 V to 16 V

Figure 51. Set/Reset Flip-Flop



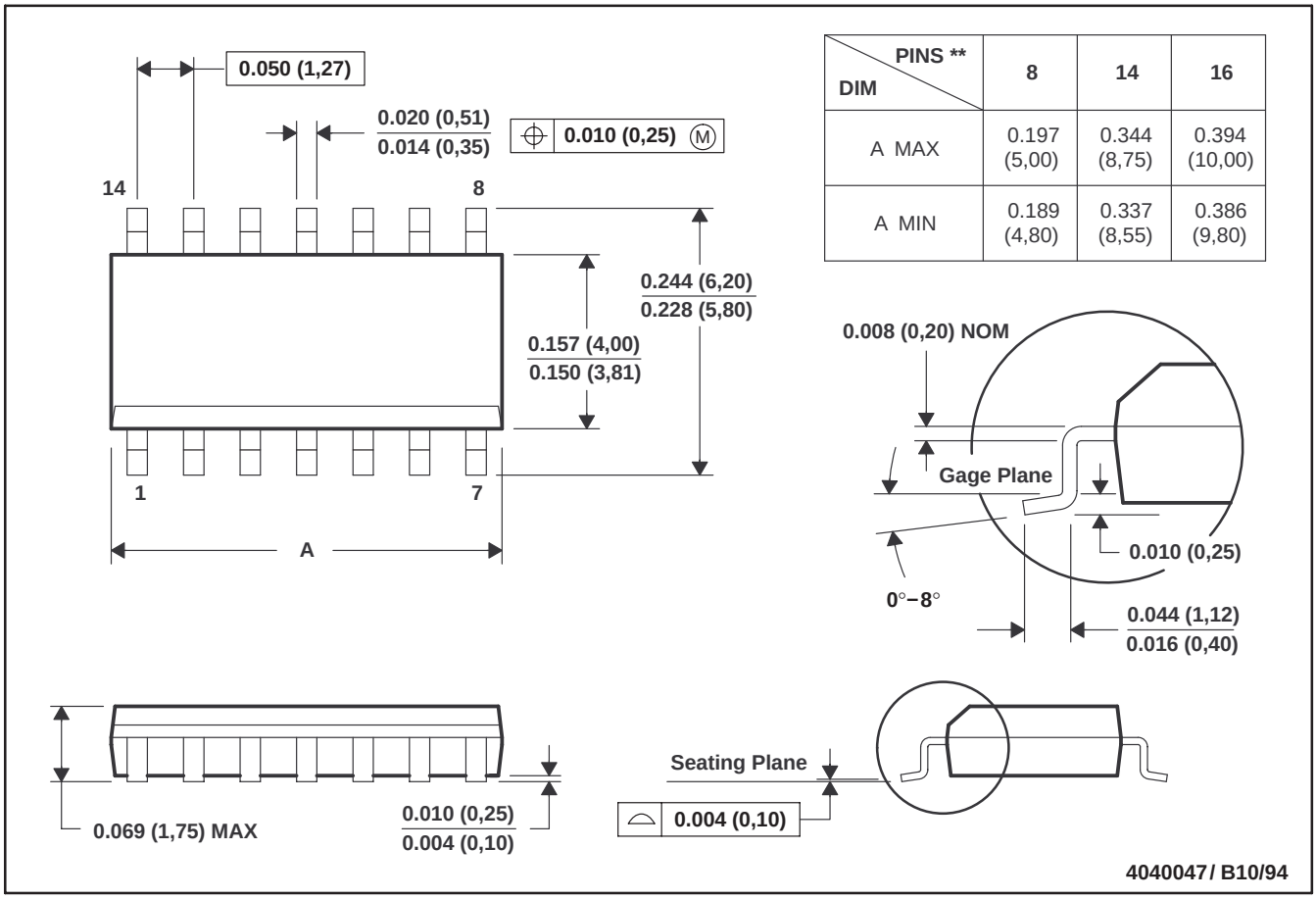
NOTE A: Normalized to F_C = 1 kHz and R_L = 10 kΩ

Figure 52. Two-Pole Low-Pass Butterworth Filter

MECHANICAL INFORMATION

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Four center pins are connected to die mount pad.
E. Falls within JEDEC MS-012

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC27L1ACP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC27L1AC	Samples
TLC27L1AID	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27L1AI	
TLC27L1BCD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	27L1BC	
TLC27L1CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	27L1C	Samples
TLC27L1CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	27L1C	Samples
TLC27L1CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC27L1CP	Samples
TLC27L1ID	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27L1I	
TLC27L1IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27L1I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

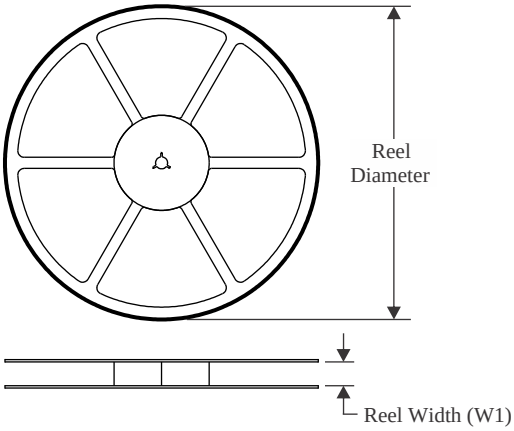
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

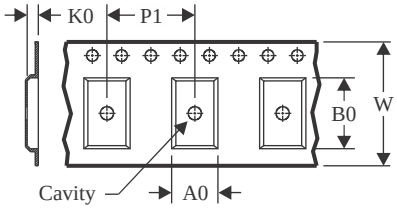
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

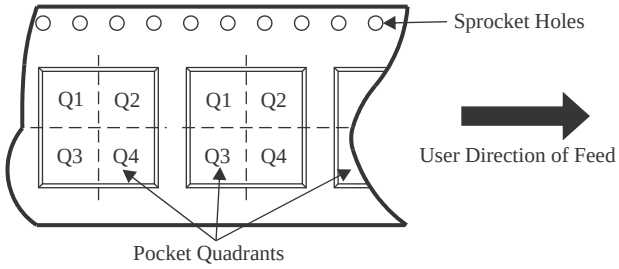


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

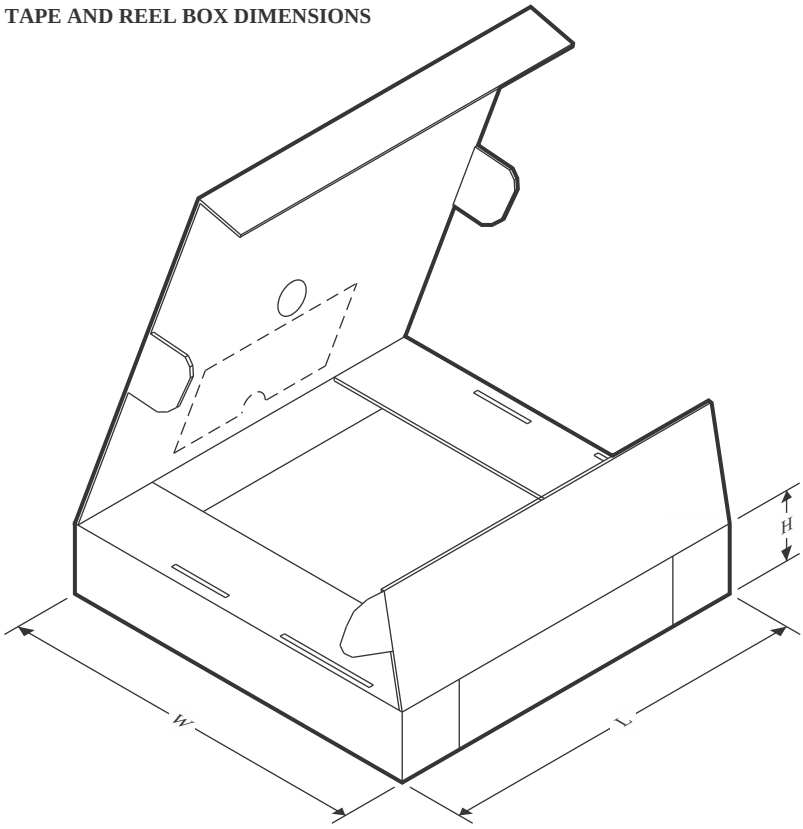
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC27L1CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC27L1IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

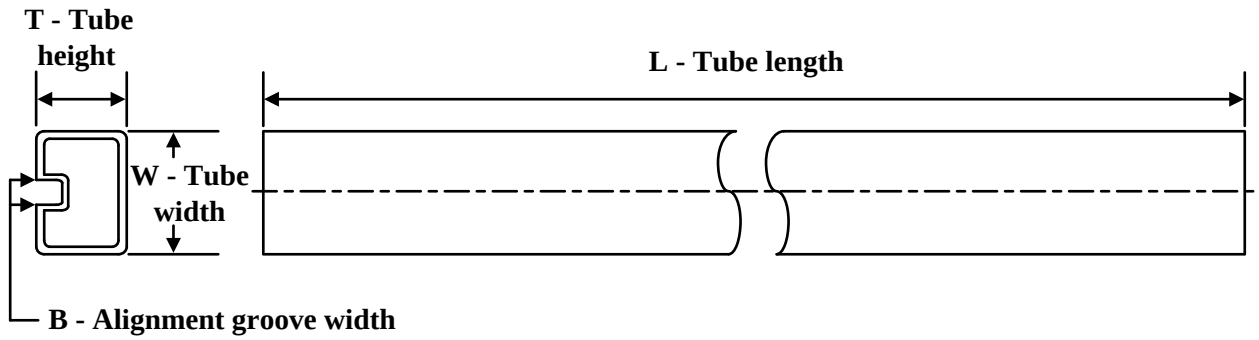
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC27L1CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC27L1IDR	SOIC	D	8	2500	340.5	338.1	20.6

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC27L1ACP	P	PDIP	8	50	506	13.97	11230	4.32
TLC27L1AID	D	SOIC	8	75	507	8	3940	4.32
TLC27L1AID	D	SOIC	8	75	505.46	6.76	3810	4
TLC27L1BCD	D	SOIC	8	75	507	8	3940	4.32
TLC27L1BCD	D	SOIC	8	75	505.46	6.76	3810	4
TLC27L1CD	D	SOIC	8	75	507	8	3940	4.32
TLC27L1CD	D	SOIC	8	75	505.46	6.76	3810	4
TLC27L1CP	P	PDIP	8	50	506	13.97	11230	4.32
TLC27L1ID	D	SOIC	8	75	507	8	3940	4.32

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265