Ultra Low Power Stereo Audio Codec With Integrated Headphone Amplifiers

Check for Samples: TLV320DAC3203

FEATURES

- **Stereo Audio DAC with 100dB SNR**
- **4.1mW Stereo 48ksps Playback**
- **PowerTune™**
- **Extensive Signal Processing Options**
- **Stereo Headphone Outputs**
- **Low Power Analog Bypass Mode**
- **Programmable PLL**
- **Integrated LDO**
- **4mm × 4mm QFN and 2.7mm × 2.7mm WCSP Package**

APPLICATIONS

- **Mobile Handsets**
- **Communication**
- **Portable Computing**

DESCRIPTION

The TLV320DAC3203 (sometimes referred to as the DAC3203) is a flexible, low-power, low-voltage stereo audio codec with programmable outputs, PowerTune capabilities, fixed predefined and parameterizable signal processing blocks, integrated PLL, integrated LDO and flexible digital interfaces. Extensive register-based control of power, input/output channel configuration, gains, effects, pin-multiplexing and clocks is included, allowing the device to be precisely targeted to its application.

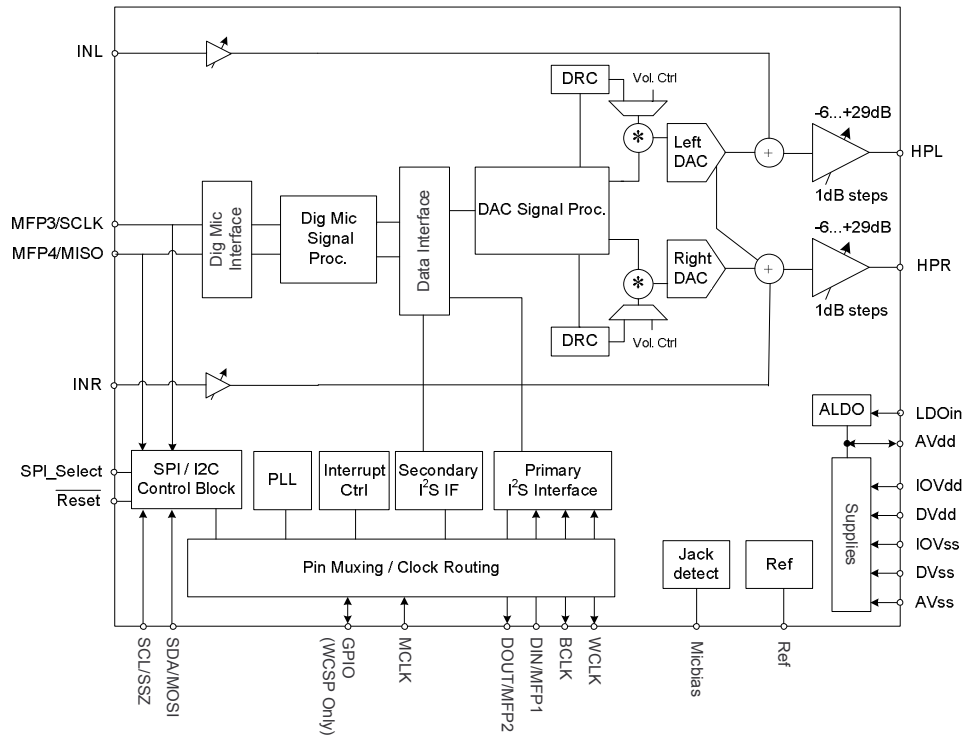

Figure 1. Simplified Block Diagram

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONTINUED)

Combined with the advanced PowerTune technology, the device can cover operations from 8kHz mono voice playback to stereo 192kHz DAC playback, making it ideal for portable battery-powered audio and telephony applications.

The playback path offers signal processing blocks for filtering and effects, true differential output signal, flexible mixing of DAC and analog input signals as well as programmable volume controls. The TLV320DAC3203 contains two high-power output drivers which can be configured in multiple ways, including stereo and mono BTL. The integrated PowerTune technology allows the device to be tuned to just the right power-performance trade-off. Mobile applications frequently have multiple use cases requiring very low-power operation while being used in a mobile environment. When used in a docked environment, power consumption typically is less of a concern and lowest possible noise is more important. With PowerTune the TLV320DAC3203 can address both cases.

The voltage supply range for the TLV320DAC3203 for analog is 1.5V–1.95V, and for digital it is 1.26V–1.95V. To ease system-level design, a low-dropout regulator (LDO) is integrated to generate the appropriate analog supply from input voltages ranging from 1.8V to 3.6V. Digital I/O voltages are supported in the range of 1.1V–3.6V.

The required internal clock of the TLV320DAC3203 can be derived from multiple sources, including the MCLK, BCLK, GPIO pins or the output of internal PLL, where the input to the PLL again can be derived from the MCLK, BCLK or GPIO pins. Although using the internal, fractional PLL ensures the availability of a suitable clock signal, it is not recommended for the lowest power settings. The PLL is highly programmable and can accept available input clocks in the range of 512kHz to 50MHz.

The device is available in the 4mm × 4mm QFN and 2.7mm × 2.7mm WCSP package.

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Package and Signal Descriptions

Packaging/Ordering Information

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	OPERATING TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TLV320DAC3203	S-XBGA-N25	YZK	–40°C to 85°C	TLV320DAC3203IYZKT	Tape and Reel, 250
				TLV320DAC3203IYZKR	Tape and Reel, 3000
	S-PVQFN-N24	RGE	–40°C to 85°C	TLV320DAC3203IRGET	Tape and Reel, 250
				TLV320DAC3203IRGER	Tape and Reel, 3000

Pin Assignments

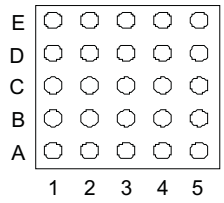

Figure 2. S-XBGA-N25 (YZK) Package, Bottom View

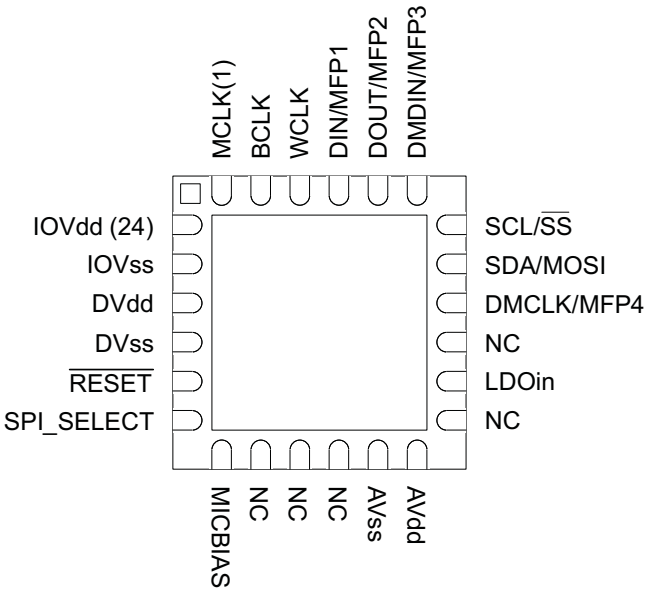

Figure 3. S-PVQFN-N24 (RGE) Package, Bottom View

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TERMINAL FUNCTIONS

TERMINAL		NAME	TYPE	DESCRIPTION
QFN PIN	WCSP BALL			
1	A1	MCLK	I	Master Clock Input
2	B2	BCLK	IO	Audio serial data bus (primary) bit clock
3	B3	WCLK	IO	Audio serial data bus (primary) word clock
4	A2	DIN/MFP1	I	Primary function Audio serial data bus data input Secondary function Digital Microphone Input General Purpose Input
5	A3	DOUT/MFP2	O	Primary Audio serial data bus data output Secondary General Purpose Output Clock Output INT1 Output INT2 Output Audio serial data bus (secondary) bit clock output Audio serial data bus (secondary) word clock output
6	A5	DMDIN/ MFP3/ SCLK	I	Primary (SPI_Select = 1) SPI serial clock Secondary: (SPI_Select = 0) Digital microphone input Headset detect input Audio serial data bus (secondary) bit clock input Audio serial data bus (secondary) DAC/common word clock input Audio serial data bus (secondary) ADC word clock input Audio serial data bus (secondary) data input General Purpose Input
7	A4	SCL/ $\overline{SS}$	I	I^2C interface serial clock (SPI_Select = 0) SPI interface mode chip-select signal (SPI_Select = 1)
8	B4	SDA/ MOSI	I	I^2C interface mode serial data input (SPI_Select = 0) SPI interface mode serial data input (SPI_Select = 1)
9	B5	DMCLK/ MFP4/ MISO	O	Primary (SPI_Select = 1) Serial data output Secondary (SPI_Select = 0) Multifunction pin #4 (MFP4) options are only available using I^2C Digital microphone clock output General purpose output CLKOUT output INT1 output INT2 output Audio serial data bus (primary) ADC word clock output Audio serial data bus (secondary) data output Audio serial data bus (secondary) bit clock output Audio serial data bus (secondary) word clock output
10	C5	HPR	O	Right high-power output driver
11	D5	LDOIN/ HPVDD	Power	LDO Input supply and Headphone Power supply 1.9V– 3.6V
12	D4	HPL	O	Left high power output driver

(1) For multiple BGA Balls assigned to the same pin-name, it is ***necessary*** to connect them on the PCB.
(2) For multiple BGA Balls assigned to the same pin-name, it is *recommended* to connect them on the PCB.

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TERMINAL FUNCTIONS (continued)

TERMINAL		NAME	TYPE	DESCRIPTION
QFN PIN	WCSP BALL			
13	D3	AVDD	Power	Analog voltage supply 1.5V–1.95V Input when A-LDO disabled, Filtering output when A-LDO enabled
14	E4	AVSS	Ground	Analog ground supply
15	E5	INL	I	Left Analog Bypass Input
16	E3	INR	I	Right Analog Bypass Input
17	E2	REF	O	Reference voltage output for filtering
18	D2	MICBIAS	O	Microphone bias voltage output
19	E1	SPI_ SELECT	I	Control mode select pin (1 = SPI, 0 = I2C)
20	C2	$\overline{\text{RESET}}$	I	Reset (active low)
21	D1	DVSS	Ground	Digital Ground and Chip-substrate
22	C1	DVDD	Power	Digital voltage supply 1.26V–1.95V
23	B1	IOVSS	Ground	I/O ground supply
24	C3	IOVDD	Power	I/O voltage supply 1.1V – 3.6V
n/a	C4	GPIO/MFP5	I	Primary General Purpose digital IO Secondary CLKOUT Output INT1 Output INT2 Output Audio serial data bus ADC word clock output Audio serial data bus (secondary) bit clock output Audio serial data bus (secondary) word clock output Digital microphone clock output

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Electrical Characteristics

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE	UNIT
AVdd to AVss		–0.3 to 2.2	V
DVdd to DVss		–0.3 to 2.2	V
IOVDD to IOVSS		–0.3 to 3.9	V
LDOIN to AVss		–0.3 to	V
Digital Input voltage		to IOVDD + 0.3	V
Analog input voltage		to AVdd + 0.3	V
Operating temperature range		–40 to 85	°C
Storage temperature range			°C
Junction temperature (T_J Max)		105	°C
S-XBGA NanoFree package (YZK)	Power dissipation	(T_J Max – T_A) / θ_{JA}	W
	θ_{JA} Thermal impedance	48	C/W

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
LDOIN (1)	Power Supply Voltage Range	Referenced to AVss (2)	1.9		3.6	V
AVdd			1.5	1.8	1.95	
IOVDD		Referenced to IOVSS (2)	1.1		3.6	
DVdd		Referenced to DVss (2)	1.65	1.8	1.95	
DVdd (3)			1.26	1.8	1.95	
	PLL Input Frequency	Clock divider uses fractional divide (D > 0), P=1, D_{Vdd} ≥ 1.65V (See table in SLAU434, *Maximum TLV320DAC3203 Clock Frequencies*)	10		20	MHz
		Clock divider uses integer divide (D = 0), P=1, D_{Vdd} ≥ 1.65V (Refer to table in SLAU434, *Maximum TLV320DAC3203 Clock Frequencies*)	0.512		20	MHz
MCLK	Master Clock Frequency	MCLK; Master Clock Frequency; D_{Vdd} ≥ 1.65V			50	MHz
SCL	SCL Clock Frequency				400	kHz
HPL, HPR	Stereo headphone output load resistance	Single-ended configuration	14.4	16		Ω
	Headphone output load resistance	Differential configuration	24.4	32		Ω
C_{Lout}	Digital output load capacitance			10		pF
C_{ref}	Reference decoupling capacitor			1		µF

(1) Minimum spec applies if LDO is used. Minimum is 1.5V if LDO is not enabled. Using the LDO below 1.9V degrades LDO performance.
(2) All grounds on board are tied together, so they should not differ in voltage by more than 0.2V max, for any combination of ground signals.
(3) At DVdd values lower than 1.65V, the PLL does not function. Please see table in SLAU434, *Maximum TLV320DAC3203 Clock Frequencies* for details on maximum clock frequencies.

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Electrical Characteristics, Bypass Outputs

At 25°C, AVdd, DVdd, IOVDD = 1.8V, LDO_in = 1.8V, AVdd LDO disabled, f_s (Audio) = 48kHz, Cref = 10µF on REF PIN, PLL disabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG BYPASS TO HEADPHONE AMPLIFIER, DIRECT MODE						
	Device Setup	Load = 16Ω (single-ended), 50pF; Input and Output CM = 0.9V; Headphone Output on LDOIN Supply; INL routed to HPL and INR routed to HPR; Channel Gain = 0dB				
	Gain Error			±0.4		dB
	Noise, A-weighted(1)	Idle Channel, INL and INR ac-shorted to ground		3		μV_{RMS}
THD	Total Harmonic Distortion	446mVrms, 1-kHz input signal		–82		dB

(1) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values

Electrical Characteristics, Microphone Interface

At 25°C, AVdd, DVdd, IOVDD = 1.8V, LDO_in = 1.8V, AVdd LDO disabled, Cref = 10µF on REF PIN, PLL disabled unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
MICROPHONE BIAS					
Bias voltage	Bias voltage CM=0.9V, LDOin = 3.3V, no load				
	Micbias Mode 0, Connect to AVdd or LDOin		1.25		V
	Micbias Mode 1, Connect to LDOin		1.7		V
	Micbias Mode 2, Connect to LDOin		2.5		V
	Micbias Mode 3, Connect to AVdd		AVdd		V
	Micbias Mode 3, Connect to LDOin		LDOin		V
	CM = 0.75V, LDOin = 3.3V				
	Micbias Mode 0, Connect to AVdd or LDOin		1.04		V
	Micbias Mode 1, Connect to AVdd or LDOin		1.42		V
	Micbias Mode 2, Connect to LDOin		2.08		V
	Micbias Mode 3, Connect to AVdd		AVdd		V
	Micbias Mode 3, Connect to LDOin		LDOin		V
Output Noise	CM = 0.9V, Micbias Mode 2, A-weighted, 20Hz to 20kHz bandwidth, Current load = 0mA.		10		μV_{RMS}
Current Sourcing	Micbias Mode 2, Connect to LDOin		3		mA
Inline Resistance	Micbias Mode 3, Connect to AVdd		160		Ω
	Micbias Mode 3, Connect to LDOin		110		

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Electrical Characteristics, Audio Outputs

At 25°C, AVdd, DVdd, IOVDD = 1.8V, LDO_in = 1.8V, AVdd LDO disabled, f_s (Audio) = 48kHz, Cref = 10 µF on REF PIN, PLL disabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio DAC – Stereo Single-Ended Headphone Output						
	Device Setup	Load = 16Ω (single-ended), 50pF Headphone Output on AVdd Supply, Input & Output CM = 0.9V, DOSR = 128, MCLK = 256* f_s, Channel Gain = 0dB word length = 16 bits; Processing Block = PRB_P1 Power Tune = PTM_P3				
	Full scale output voltage (0dB)			0.5		V_{RMS}
SNR	Signal-to-noise ratio, A-weighted (1) (2)	All zeros fed to DAC input, modulator in excited state	88	100		dB
DR	Dynamic range, A-weighted (1) (2)	–60dB 1kHz input full-scale signal, Word Length = 20 bits, Power Tune = PTM_P4		99		dB
THD+N	Total Harmonic Distortion plus Noise	–3dB full-scale, 1-kHz input signal		–80	–70	dB
	DAC Gain Error	0dB, 1kHz input full scale signal		±0.1		dB
	DAC Mute Attenuation	Mute		127		dB
	DAC channel separation	–1dB, 1kHz signal, between left and right HP out		92		dB
	DAC PSRR	100mVpp, 1kHz signal applied to AVdd		70		dB
		100mVpp, 217Hz signal applied to AVdd		75		dB
	Power Delivered	R_L=16Ω, Output Stage on AVdd = 1.8V THDN < 1%, Input CM=0.9V, Output CM=0.9V, Channel Gain = 2dB		13		mW
		R_L= 16Ω Output Stage on LDOIN = 3.3V, THDN < 1% Input CM = 0.9V, Output CM = 1.65V, Channel Gain = 8dB		47		
Audio DAC – Stereo Single-Ended Headphone Output						
	Device Setup	Load = 16Ω (single-ended), 50pF, Headphone Output on AVdd Supply, Input & Output CM = 0.75V; AVdd = 1.5V, DOSR = 128, MCLK = 256* f_s, Channel Gain = –2dB, word length = 20-bits; Processing Block = PRB_P1, Power Tune = PTM_P4				
	Full scale output voltage (0dB)			0.375		V_{RMS}
SNR	Signal-to-noise ratio, A-weighted (1) (2)	All zeros fed to DAC input, modulator in excited state		99		dB
DR	Dynamic range, A-weighted (1) (2)	-60dB 1 kHz input full-scale signal		98		dB
THD+N	Total Harmonic Distortion plus Noise	–3dB full-scale, 1-kHz input signal		–84		dB
Audio DAC – Mono Differential Headphone Output						
	Device Setup	Load = 32 Ω (differential), 50pF, Headphone Output on LDOIN Supply Input CM = 0.75V, Output CM = 1.5V, AVdd=1.8V, LDOIN = 3.0V, DOSR = 128 MCLK = 256* f_s, Channel (headphone driver) Gain = 5dB for full scale output signal, word length = 16-bits, Processing Block = PRB_P1, Power Tune = PTM_P3				

(1) Ratio of output level with 1-kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.

(2) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values

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Electrical Characteristics, Audio Outputs (continued)

At 25°C, AVdd, DVdd, IOVDD = 1.8V, LDO_in = 1.8V, AVdd LDO disabled, f_s (Audio) = 48kHz, Cref = 10 µF on REF PIN, PLL disabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Full scale output voltage (0dB)			1778		mV_{RMS}
SNR	Signal-to-noise ratio, A-weighted (1) (2)	All zeros fed to DAC input, modulator in excited state		101		dB
DR	Dynamic range, A-weighted (1) (2)	–60dB 1kHz input full-scale signal		98		dB
THD	Total Harmonic Distortion	–3dB full-scale, 1-kHz input signal		–82		dB
	Power Delivered	R_L = 32Ω, Output Stage on LDOIN = 3.3V, THDN < 1%, Input CM = 0.9V, Output CM = 1.65V, Channel Gain = 8dB		125		mW
		R_L = 32Ω Output Stage on LDOIN = 3.0V, THDN < 1% Input CM = 0.9V, Output CM = 1.5V, Channel Gain = 8dB		103		mW

Electrical Characteristics, LDO

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOW DROPOUT REGULATOR (AVdd)					
Output Voltage	LDOMode = 1, LDOin > 1.95V, I_O = 15mA		1.63		V
	LDOMode = 0, LDOin > 2.0V, I_O = 15mA		1.68		
	LDOMode = 2, LDOin > 2.05V, I_O = 15mA		1.73		
Output Voltage Accuracy			±2		%
Load Regulation	Load current range 0 to 50mA		26		mV
Line Regulation	Input Supply Range 1.9V to 3.6V		3		mV
Decoupling Capacitor		1			µF
Bias Current			50		µA

Electrical Characteristics, Misc.

At 25°C, AVdd, DVdd, IOVDD = 1.8V, LDO_in = 3.3V, AVdd LDO disabled, f_s (Audio) = 48kHz, Cref = 10 µF on REF PIN, PLL disabled unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE					
Reference Voltage Settings	CMMode = 0 (0.9V)		0.9		V
	CMMode = 1 (0.75V)		0.75		
Reference Noise	CM=0.9V, A-weighted, 20Hz to 20kHz bandwidth, C_{ref} = 10µF		1		$µV_{RfcMS}$
Decoupling Capacitor		1	10		µF
Bias Current			120		µA
Shutdown Current					
Device Setup	Coarse AVdd supply turned off, LDO_select held at ground, No external digital input is toggled				
I_{DVdd}			1.4		µA
I_{AVdd}			1		
I_{LDOin}			1		
I_{IOVDD}			<0.1		

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Electrical Characteristics, Logic Levels

At 25°C, AV_{DD}, DV_{DD}, IOV_{DD} = 1.8V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC FAMILY				**CMOS**		
V_{IH}	Logic Level	I_{IH} = 5 µA, IOV_{DD} > 1.6V	0.7 × IOV_{DD}			V
		I_{IH} = 5µA, 1.2V ≤ IOV_{DD} <1.6V	0.9 × IOV_{DD}			V
		I_{IH} = 5µA, IOV_{DD} < 1.2V	IOV_{DD}			V
V_{IL}		I_{IL} = 5 µA, IOV_{DD} > 1.6V	–0.3		0.3 × IOV_{DD}	V
		I_{IL} = 5µA, 1.2V ≤ IOV_{DD} <1.6V			0.1 × IOV_{DD}	V
		I_{IL} = 5µA, IOV_{DD} < 1.2V			0	V
V_{OH}		I_{OH} = 2 TTL loads	0.8 × IOV_{DD}			V
V_{OL}		I_{OL} = 2 TTL loads			0.1 × IOV_{DD}	V
	Capacitive Load			10		pF

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Interface Timing

Typical Timing Characteristics — Audio Data Serial Interface Timing (I^2S)

All specifications at 25°C, DVdd = 1.8V

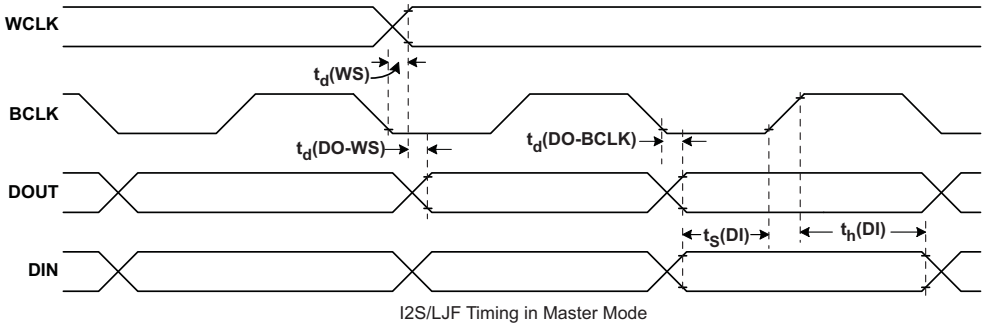

Figure 4. I^2S/LJF/RJF Timing in Master Mode

Table 1. I^2S/LJF/RJF Timing in Master Mode (see Figure 4)

PARAMETER		IOVDD=1.8V		IOVDD=3.3V		UNITS
		MIN	MAX	MIN	MAX	
t_d(WS)	WCLK delay		30		20	ns
t_d (DO-WS)	WCLK to DOUT delay (For LJF Mode only)		50		25	ns
t_d (DO-BCLK)	BCLK to DOUT delay		50		25	ns
t_s(DI)	DIN setup	8		8		ns
t_h(DI)	DIN hold	8		8		ns
t_r	Rise time		24		12	ns
t_f	Fall time		24		15	ns

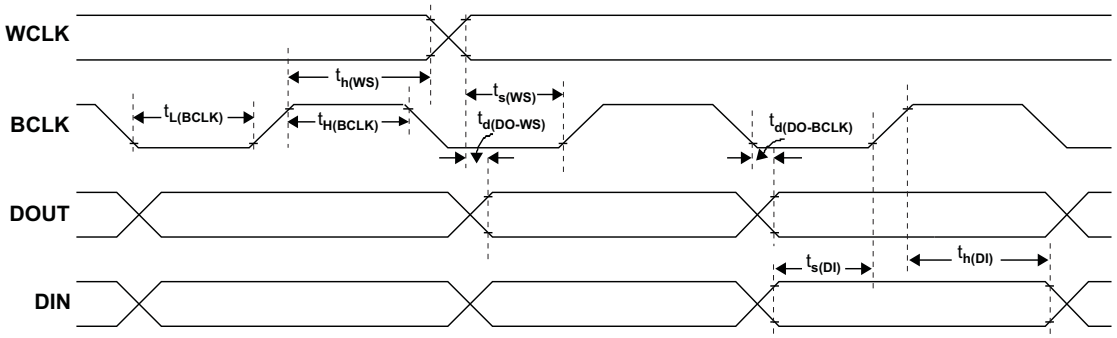

Figure 5. I^2S/LJF/RJF Timing in Slave Mode

Table 2. I^2S/LJF/RJF Timing in Slave Mode (see Figure 5)

PARAMETER		IOVDD=1.8V		IOVDD=3.3V		UNITS
		MIN	MAX	MIN	MAX	
t_H (BCLK)	BCLK high period	35		35		ns
t_L (BCLK)	BCLK low period	35		35		
t_s (WS)	WCLK setup	8		8		
t_h (WS)	WCLK hold	8		8		
t_d (DO-WS)	WCLK to DOUT delay (For LJF mode only)		50		25	
t_d (DO-BCLK)	BCLK to DOUT delay		50		25	
t_s(DI)	DIN setup	8		8		
t_h(DI)	DIN hold	8		8		
t_r	Rise time		4		4	
t_f	Fall time		4		4	

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Typical DSP Timing Characteristics

All specifications at 25°C, DVdd = 1.8V

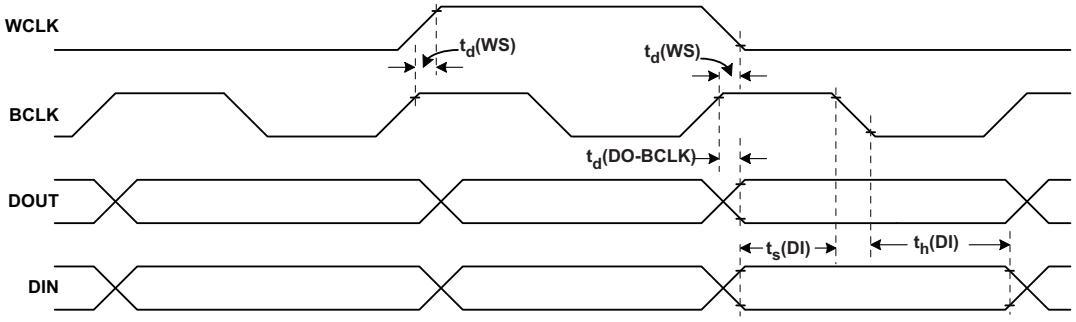

Figure 6. DSP Timing in Master Mode

Table 3. DSP Timing in Master Mode (see Figure 6)

PARAMETER		IOVDD=1.8V		IOVDD=3.3V		UNITS
		MIN	MAX	MIN	MAX	
t_d (WS)	WCLK delay		30		20	ns
t_d (DO-BCLK)	BCLK to DOUT delay		40		20	ns
t_s(DI)	DIN setup	8		8		ns
t_h(DI)	DIN hold	8		8		ns
t_r	Rise time		24		12	ns
t_f	Fall time		24		12	ns

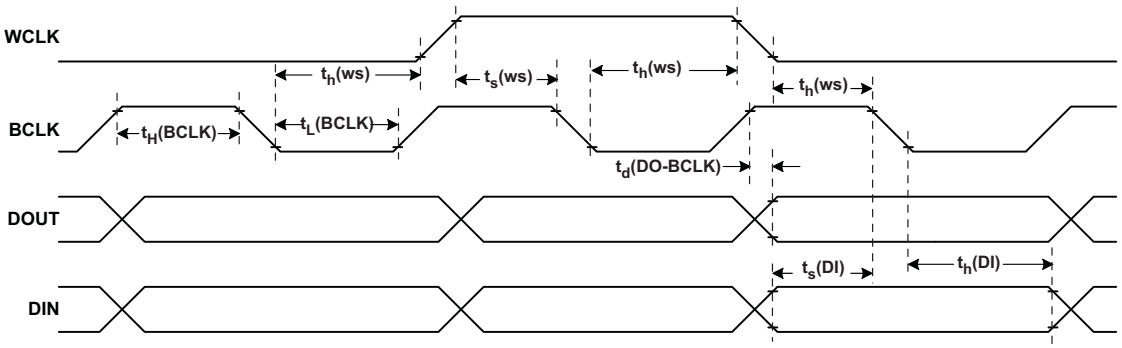

Figure 7. DSP Timing in Slave Mode

Table 4. DSP Timing in Slave Mode (see Figure 7)

PARAMETER		IOVDD=1.8V		IOVDD=3.3V		UNITS
		MIN	MAX	MIN	MAX	
t_H (BCLK)	BCLK high period	35		35		ns
t_L (BCLK)	BCLK low period	35		35		ns
t_s(WS)	WCLK setup	8		8		ns
t_h(WS)	WCLK hold	8		8		ns
t_d (DO-BCLK)	BCLK to DOUT delay		40		22	ns
t_s(DI)	DIN setup	8		8		ns
t_h(DI)	DIN hold	8		8		ns
t_r	Rise time		4		4	ns
t_f	Fall time		4		4	ns

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I²C Interface Timing

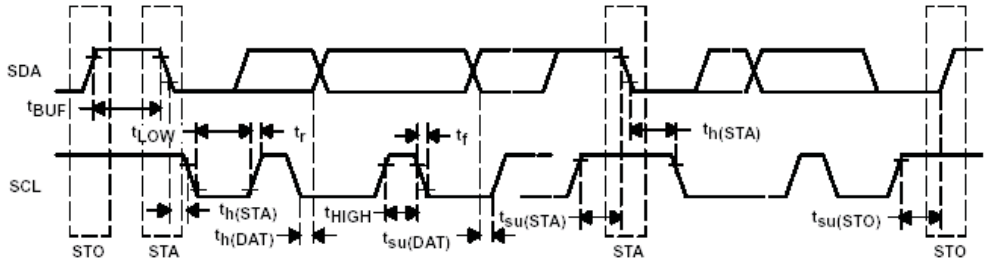

Figure 8.

Table 5. I²C Interface Timing

PARAMETER		TEST CONDITION	Standard-Mode			Fast-Mode			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{SCL}	SCL clock frequency		0		100	0		400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.		4.0			0.8			µs
t_{LOW}	LOW period of the SCL clock		4.7			1.3			µs
t_{HIGH}	HIGH period of the SCL clock		4.0			0.6			µs
$t_{SU;STA}$	Setup time for a repeated START condition		4.7			0.8			µs
$t_{HD;DAT}$	Data hold time: For I2C bus devices		0		3.45	0		0.9	µs
$t_{SU;DAT}$	Data set-up time		250			100			ns
t_r	SDA and SCL Rise Time				1000	$20+0.1C_b$		300	ns
t_f	SDA and SCL Fall Time				300	$20+0.1C_b$		300	ns
$t_{SU;STO}$	Set-up time for STOP condition		4.0			0.8			µs
t_{BUF}	Bus free time between a STOP and START condition		4.7			1.3			µs
C_b	Capacitive load for each bus line				400			400	pF

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SPI Interface Timing

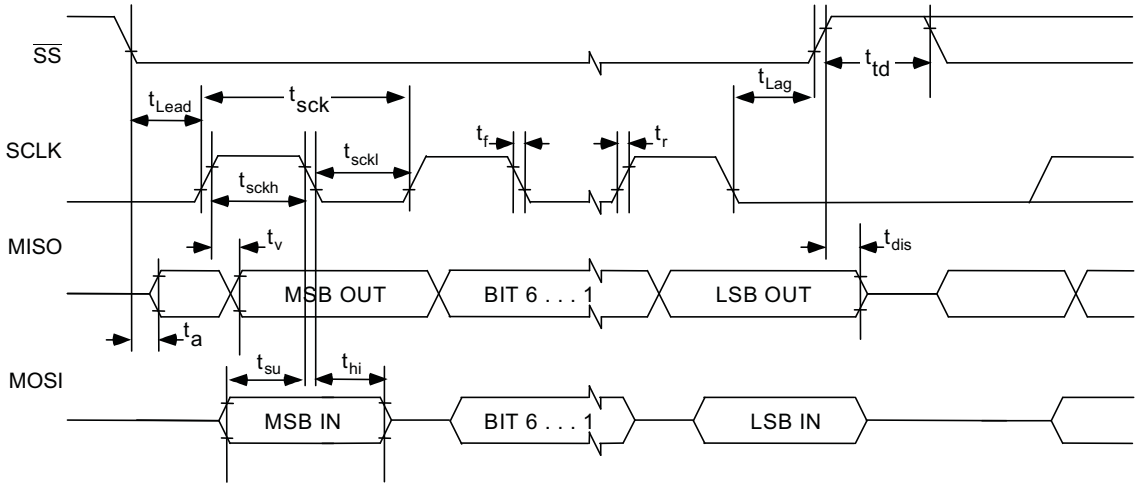

Figure 9. SPI Interface Timing Diagram

Timing Requirements (See Figure 9)

At 25°C, DVdd = 1.8V

Table 6. SPI Interface Timing

PARAMETER		TEST CONDITION	IOVDD=1.8V			IOVDD=3.3V			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{sck}	SCLK Period		100			50			ns
t_{sckh}	SCLK Pulse width High		50			25			ns
t_{sckl}	SCLK Pulse width Low		50			25			ns
t_{lead}	Enable Lead Time		30			20			ns
t_{lag}	Enable Lag Time		30			20			ns
$t_{d;seqxfr}$	Sequential Transfer Delay		40			20			ns
t_a	Slave DOUT access time				40			20	ns
t_{dis}	Slave DOUT disable time				40			25	ns
t_{su}	DIN data setup time		15			10			ns
$t_{h;DIN}$	DIN data hold time		15			10			ns
$t_{v;DOUT}$	DOUT data valid time				45			25	ns
t_r	SCLK Rise Time				4			4	ns
t_f	SCLK Fall Time				4			4	ns

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Typical Characteristics

Device Power Consumption

Device power consumption largely depends on PowerTune configuration. For information on device power consumption, see the *TLV320DAC3203 Application Reference Guide*, literature number SLAU434.

Typical Performance

TOTAL HARMONIC DISTORTION vs HEADPHONE OUTPUT POWER

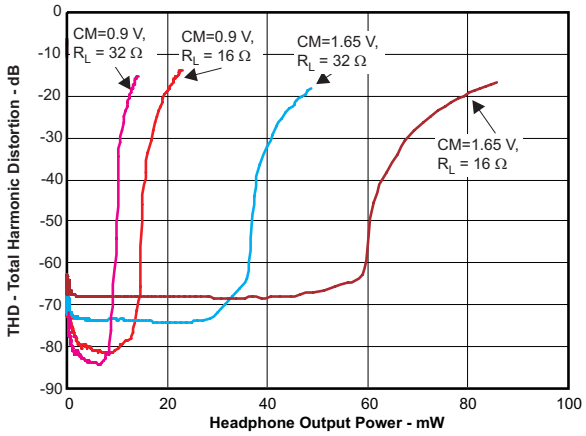

Figure 10.

TOTAL HARMONIC DISTORTION vs HEADPHONE OUTPUT POWER

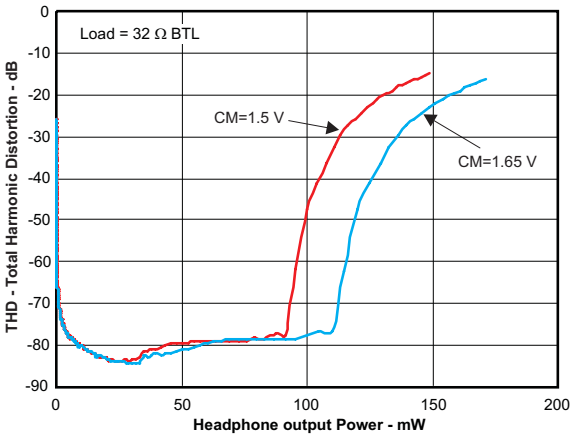

Figure 11.

HEADPHONE SNR AND SE OUTPUT POWER vs OUTPUT COMMON MODE SETTING

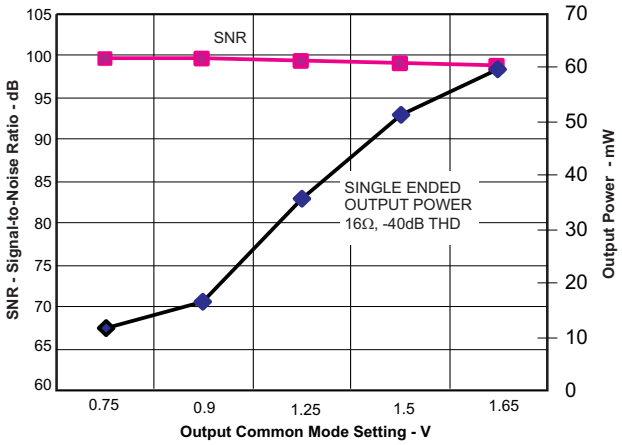

Figure 12.

LDO DROPOUT VOLTAGE vs LOAD CURRENT

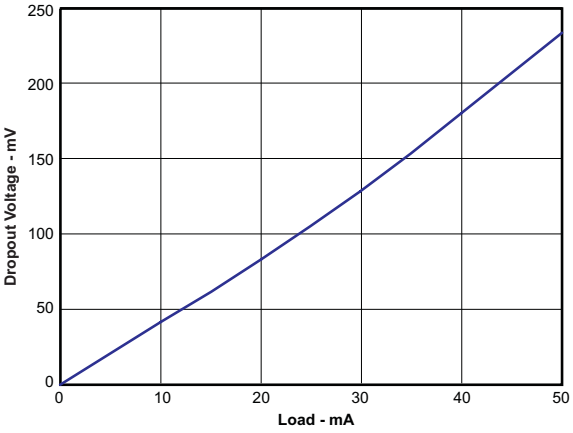

Figure 13.

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LDO LOAD RESPONSE

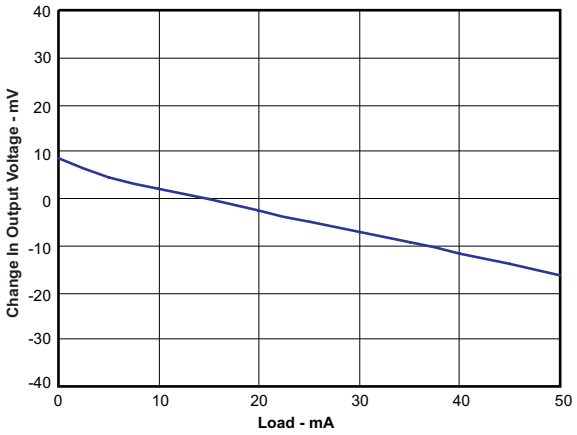

Figure 14.

MICBIAS MODE 2, CM = 0.9V, LDOIN OP STAGE
vs
MICBIAS LOAD CURRENT

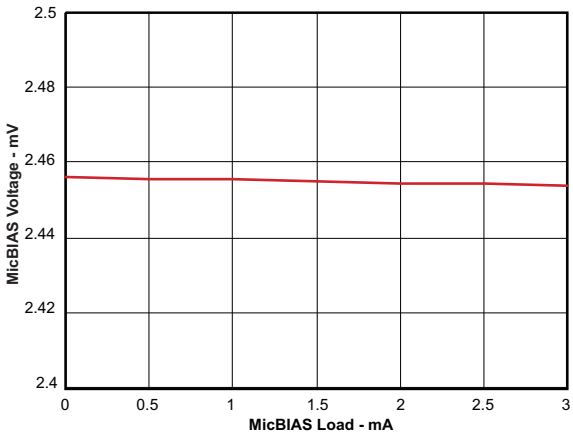

Figure 15.

FFT

DAC TO HEADPHONE FFT @ -3dBFS

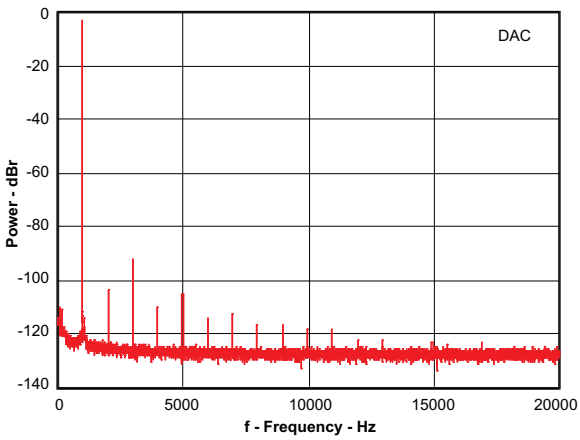

Figure 16.

ANALOG BYPASS TO HEADPHONE FFT @ -3dB BELOW 0.5Vrms

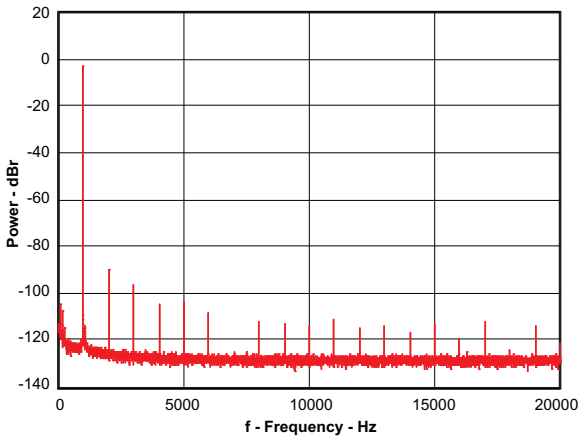

Figure 17.

Typical Circuit Configuration

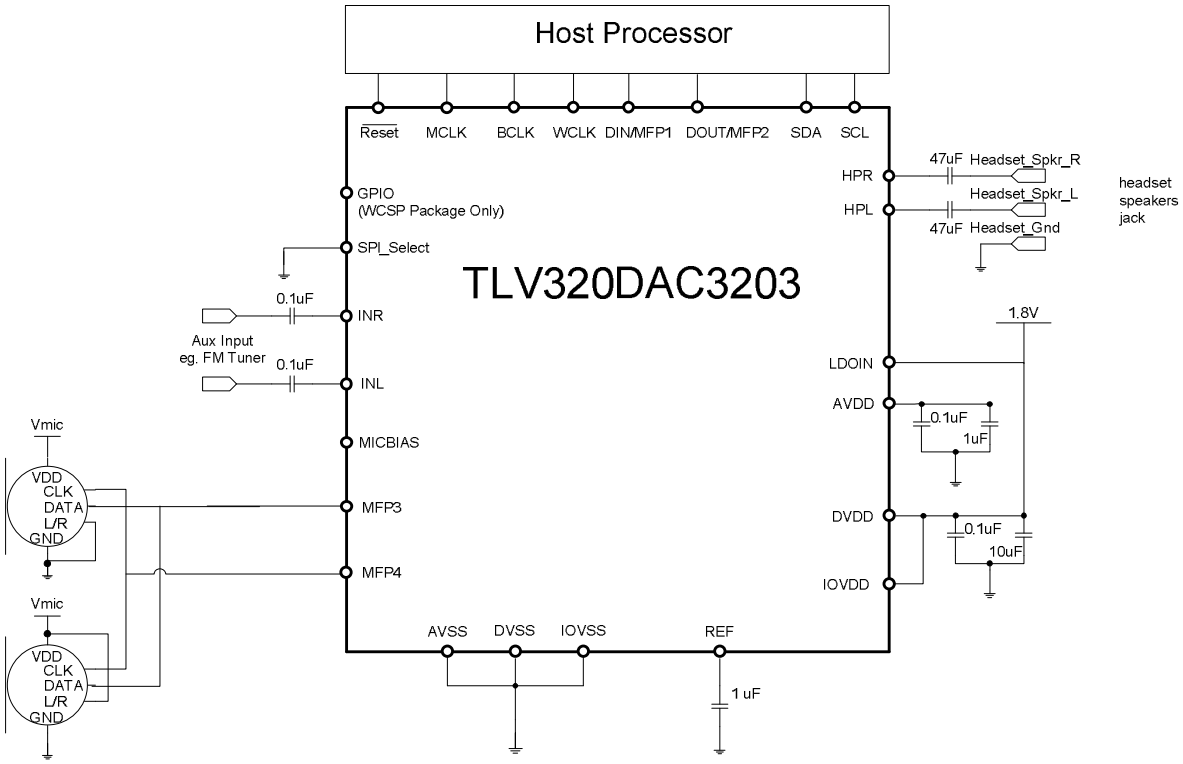

Figure 18. Typical Circuit Configuration

Application Overview

The TLV320DAC3203 offers a wide range of configuration options. Figure 1 shows the basic functional blocks of the device.

Device Connections

Digital Pins

Only a small number of digital pins are dedicated to a single function; whenever possible, the digital pins have a default function, and also can be reprogrammed to cover alternative functions for various applications.

The fixed-function pins are Reset and the SPI_Select pin, which are HW control pins. Depending on the state of SPI_Select, the two control-bus pins SCL/SS and SDA/MOSI are configured for either I^2C or SPI protocol.

Other digital IO pins can be configured for various functions via register control. An overview of available functionality is given in Multifunction Pins.

Analog Pins

Analog functions can also be configured to a large degree. For minimum power consumption, analog blocks are powered down by default. The blocks can be powered up with fine granularity according to the application needs.

Multifunction Pins

Table 7 shows the possible allocation of pins for specific functions. The PLL input, for example, can be programmed to be any of 4 pins (MCLK, BCLK, DIN, GPIO).

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Table 7. Multifunction Pin Assignments

		1	2	3	4	5	6	7	8
	Pin Function	**MCLK**	**BCLK**	**WCLK**	**DIN MFP1**	**DOUT MFP2**	**MFP3/ SCLK**	**MFP4/ MISO**	**GPIO MFP5**
A	PLL Input	S(1)	S(2)		E				S(3)
B	Codec Clock Input	S(1) ,D(4)	S(2)						S(3)
C	I^2S BCLK input		S(2),D						
D	I^2S BCLK output		E(5)						
E	I^2S WCLK input			E, D					
F	I^2S WCLK output			E					
G	I^2S ADC word clock input						E		E
H	I^2S ADC WCLK out							E	E
I	I^2S DIN				E, D				
J	I^2S DOUT					E, D			
K	General Purpose Output I					E			
K	General Purpose Output II							E	
K	General Purpose Output III								E
L	General Purpose Input I				E				
L	General Purpose Input II						E		
L	General Purpose Input III								E
M	INT1 output					E		E	E
N	INT2 output					E		E	E
Q	Secondary I^2S BCLK input						E		E
R	Secondary I^2S WCLK in						E		E
S	Secondary I^2S DIN						E		E
T	Secondary I^2S DOUT							E	
U	Secondary I^2S BCLK OUT					E		E	E
V	Secondary I^2S WCLK OUT					E		E	E
X	Aux Clock Output					E		E	E

(1) S(1): The MCLK pin can be used to drive the PLL and Codec Clock inputs **simultaneously**
(2) S(2): The BCLK pin can be used to drive the PLL and Codec Clock and audio interface bit clock inputs **simultaneously**
(3) S(3): The GPIO/MFP5 pin can be used to drive the PLL and Codec Clock inputs simultaneously
(4) D: Default Function
(5) E: The pin is **exclusively** used for this function, no other function can be implemented with the same pin (e.g. if GPIO/MFP5 has been allocated for General Purpose Output, it cannot be used as the INT1 output at the same time)

Analog Audio I/O

The analog I/O path of the TLV320DAC3203 offers a variety of options for signal conditioning and routing:

- 2 headphone amplifier outputs
- Analog gain setting
- Single ended and differential modes

Analog Low Power Bypass

The TLV320DAC3203 offers an analog-bypass mode. An analog signal can be routed from the analog input pin to the output amplifier. Neither the digital-input processing blocks nor the DAC resources are required for such operation; this supports low-power operation during analog-bypass mode.

In analog low-power bypass mode, line-level signals can be routed directly from the analog inputs INL to the left headphone amplifier (HPL) and INR to HPR.

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Headphone Outputs

The stereo headphone drivers on pins HPL and HPR can drive loads with impedances down to 16Ω in single-ended AC-coupled headphone configurations, or loads down to 32Ω in differential mode, where a speaker is connected between HPL and HPR. In single-ended drive configuration these drivers can drive up to 15mW power into each headphone channel while operating from 1.8V analog supplies. While running from the AVdd supply, the output common-mode of the headphone driver is set by the common-mode setting of analog inputs to allow maximum utilization of the analog supply range while simultaneously providing a higher output-voltage swing. In cases when higher output-voltage swing is required, the headphone amplifiers can run directly from the higher supply voltage on LDOIN input (up to 3.6V). To use the higher supply voltage for higher output signal swing, the output common-mode can be adjusted to either 1.25V, 1.5V or 1.65V. When the common-mode voltage is configured at 1.65V and LDOIN supply is 3.3V, the headphones can each deliver up to 40mW power into a 16Ω load.

The headphone drivers are capable of driving a mixed combination of DAC signal and bypass from analog input INL and INR. The analog input signals can be attenuated up to 72dB before routing. The level of the DAC signal can be controlled using the digital volume control of the DAC. To control the output-voltage swing of headphone drivers, the digital volume control provides a range of –6.0dB to +29.0dB (6) in steps of 1dB. These level controls are not meant to be used as dynamic volume control, but more to set output levels during initial device configuration. Refer to for recommendations for using headphone volume control for achieving 0dB gain through the DAC channel with various configurations.

Digital Microphone Inteface

The TLV320DAC3203 includes a stereo decimation filter for digital microphone inputs. The stereo recording path can be powered up one channel at a time, to support the case where only mono record capability is required.

The digital microphone input path of the TLV320DAC3203 features a large set of options for signal conditioning as well as signal routing:

- Stereo decimation filters (PDM input)
- Fine gain adjustment of digital channels with 0.1 dB step size
- Digital volume control with a range of -12 to +20dB
- Mute function

In addition to the standard set of stereo decimation filter features the TLV320DAC3203 also offers the following special functions:

- Channel-to-channel phase adjustment
- Adaptive filter mode

ADC Processing Blocks — Overview

The TLV320DAC3203 includes a built-in digital decimation filter to process the oversampled data from the PDM input to generate digital data at Nyquist sampling rate with high dynamic range. The decimation filter can be chosen from three different types, depending on the required frequency response, group delay and sampling rate.

Processing Blocks

The TLV320DAC3203 offers a range of processing blocks which implement various signal processing capabilities along with decimation filtering. These processing blocks give users the choice of how much and what type of signal processing they may use and which decimation filter is applied.

Table 8 gives an overview of the available processing blocks and their properties.

The signal processing blocks available are:

- First-order IIR
- Scalable number of biquad filters
- Variable-tap FIR filter

(6) If the device must be placed into 'mute' from the –6.0dB setting, set the device at a gain of –5.0dB first, then place the device into mute.

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The processing blocks are tuned for common cases and can achieve high anti-alias filtering or low-group delay in combination with various signal processing effects such as audio effects and frequency shaping. The available first order IIR, BiQuad and FIR filters have fully user-programmable coefficients. The Resource Class Column (RC) gives an approximate indication of power consumption.

Table 8. Processing Blocks

Processing Blocks	Channel	Decimation Filter	1st Order IIR Available	Number BiQuads	FIR	Required AOSR Value	Resource Class
PRB_R1(1)	Stereo	A	Yes	0	No	128,64	6
PRB_R2	Stereo	A	Yes	5	No	128,64	8
PRB_R3	Stereo	A	Yes	0	25-Tap	128,64	8
PRB_R4	Right	A	Yes	0	No	128,64	3
PRB_R5	Right	A	Yes	5	No	128,64	4
PRB_R6	Right	A	Yes	0	25-Tap	128,64	4
PRB_R7	Stereo	B	Yes	0	No	64	3
PRB_R8	Stereo	B	Yes	3	No	64	4
PRB_R9	Stereo	B	Yes	0	20-Tap	64	4
PRB_R10	Right	B	Yes	0	No	64	2
PRB_R11	Right	B	Yes	3	No	64	2
PRB_R12	Right	B	Yes	0	20-Tap	64	2
PRB_R13	Stereo	C	Yes	0	No	32	3
PRB_R14	Stereo	C	Yes	5	No	32	4
PRB_R15	Stereo	C	Yes	0	25-Tap	32	4
PRB_R16	Right	C	Yes	0	No	32	2
PRB_R17	Right	C	Yes	5	No	32	2
PRB_R18	Right	C	Yes	0	25-Tap	32	2

(1) Default

For more detailed information see the *TLV320DAC3203 Application Reference Guide*

DAC

The TLV320DAC3203 includes a stereo audio DAC supporting data rates from 8kHz to 192kHz. Each channel of the stereo audio DAC consists of a signal-processing engine with fixed processing blocks, a digital interpolation filter, multi-bit digital delta-sigma modulator, and an analog reconstruction filter. The DAC is designed to provide enhanced performance at low sampling rates through increased oversampling and image filtering, thereby keeping quantization noise generated within the delta-sigma modulator and signal images strongly suppressed within the audio band to beyond 20kHz. To handle multiple input rates and optimize performance, the TLV320DAC3203 allows the system designer to program the oversampling rates over a wide range from 1 to 1024. The system designer can choose higher oversampling ratios for lower input data rates and lower oversampling ratios for higher input data rates.

The TLV320DAC3203 DAC channel includes a built-in digital interpolation filter to generate oversampled data for the sigma-delta modulator. The interpolation filter can be chosen from three different types depending on required frequency response, group delay and sampling rate.

The DAC path of the TLV320DAC3203 features many options for signal conditioning and signal routing:

- Digital volume control with a range of -63.5 to +24dB
- Mute function
- Dynamic range compression (DRC)

In addition to the standard set of DAC features the TLV320DAC3203 also offers the following special features:

- Built in sine wave generation (beep generator)
- Digital auto mute
- Adaptive filter mode

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DAC Processing Blocks — Overview

The TLV320DAC3203 implements signal processing capabilities and interpolation filtering via processing blocks. These fixed processing blocks give users the choice of how much and what type of signal processing they may use and which interpolation filter is applied.

Table 9 gives an overview over all available processing blocks of the DAC channel and their properties.

The signal processing blocks available are:

- First-order IIR
- Scalable number of biquad filters
- 3D – Effect
- Beep Generator

The processing blocks are tuned for typical cases and can achieve high image rejection or low group delay in combination with various signal processing effects such as audio effects and frequency shaping. The available first-order IIR and biquad filters have fully user-programmable coefficients. The Resource Class Column (RC) gives an approximate indication of power consumption.

Table 9. Overview – DAC Predefined Processing Blocks

Processing Block No.	Interpolation Filter	Channel	1st Order IIR Available	Num. of Biquads	DRC	3D	Beep Generator	Resource Class
PRB_P1(1)	A	Stereo	No	3	No	No	No	8
PRB_P2	A	Stereo	Yes	6	Yes	No	No	12
PRB_P3	A	Stereo	Yes	6	No	No	No	10
PRB_P4	A	Left	No	3	No	No	No	4
PRB_P5	A	Left	Yes	6	Yes	No	No	6
PRB_P6	A	Left	Yes	6	No	No	No	6
PRB_P7	B	Stereo	Yes	0	No	No	No	6
PRB_P8	B	Stereo	No	4	Yes	No	No	8
PRB_P9	B	Stereo	No	4	No	No	No	8
PRB_P10	B	Stereo	Yes	6	Yes	No	No	10
PRB_P11	B	Stereo	Yes	6	No	No	No	8
PRB_P12	B	Left	Yes	0	No	No	No	3
PRB_P13	B	Left	No	4	Yes	No	No	4
PRB_P14	B	Left	No	4	No	No	No	4
PRB_P15	B	Left	Yes	6	Yes	No	No	6
PRB_P16	B	Left	Yes	6	No	No	No	4
PRB_P17	C	Stereo	Yes	0	No	No	No	3
PRB_P18	C	Stereo	Yes	4	Yes	No	No	6
PRB_P19	C	Stereo	Yes	4	No	No	No	4
PRB_P20	C	Left	Yes	0	No	No	No	2
PRB_P21	C	Left	Yes	4	Yes	No	No	3
PRB_P22	C	Left	Yes	4	No	No	No	2
PRB_P23	A	Stereo	No	2	No	Yes	No	8
PRB_P24	A	Stereo	Yes	5	Yes	Yes	No	12
PRB_P25	A	Stereo	Yes	5	Yes	Yes	Yes	12

(1) Default

For more detailed information see the *TLV320DAC3203 Application Reference Guide*.

Powertune

The TLV320DAC3203 features PowerTune, a mechanism to balance power-versus-performance trade-offs at the time of device configuration. The device can be tuned to minimize power dissipation, to maximize performance, or to an operating point between the two extremes to best fit the application.

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For more detailed information see the *TLV320DAC3203 Application Reference Guide*.

Digital Audio I/O Interface

Audio data is transferred between the host processor and the TLV320DAC3203 via the digital audio data serial interface, or audio bus. The audio bus on this device is very flexible, including left or right-justified data options, support for I^2S or PCM protocols, programmable data length options, a TDM mode for multichannel operation, very flexible master/slave configurability for each bus clock line, and the ability to communicate with multiple devices within a system directly.

The audio bus of the TLV320DAC3203 can be configured for left or right-justified, I^2S, DSP, or TDM modes of operation, where communication with standard PCM interfaces is supported within the TDM mode. These modes are all MSB-first, with data width programmable as 16, 20, 24, or 32 bits by configuring Page 0, Register 27, D(5:4). In addition, the word clock and bit clock can be independently configured in either Master or Slave mode, for flexible connectivity to a wide variety of processors. The word clock is used to define the beginning of a frame, and may be programmed as either a pulse or a square-wave signal. The frequency of this clock corresponds to the DAC sampling frequency.

The bit clock is used to clock in and clock out the digital audio data across the serial bus. When in Master mode, this signal can be programmed to generate variable clock pulses by controlling the bit-clock divider in Page 0, Register 30. The number of bit-clock pulses in a frame may need adjustment to accommodate various word-lengths as well as to support the case when multiple TLV320DAC3203s may share the same audio bus.

The TLV320DAC3203 also includes a feature to offset the position of start of data transfer with respect to the word-clock. This offset can be controlled in terms of number of bit-clocks and can be programmed in Page 0, Register 28.

The TLV320DAC3203 also has the feature of inverting the polarity of the bit-clock used for transferring the audio data as compared to the default clock polarity used. This feature can be used independently of the mode of audio interface chosen. This can be configured via Page 0, Register 29, D(3).

The TLV320DAC3203 includes the programmability to program at what bit clock in a frame does audio data begin. This enables time-division multiplexing (TDM), enabling use of multiple codecs on a single audio bus. When the audio serial data bus is powered down while configured in master mode, the pins associated with the interface are put into a hi-Z output condition.

By default when the word-clocks and bit-clocks are generated by the TLV320DAC3203, these clocks are active only when the DAC is powered up within the device. This is done to save power. However, it also supports a feature when both the word clocks and bit-clocks can be active even when the DAC in the device is powered down. This is useful when using the TDM mode with multiple codecs on the same bus, or when word-clock or bit-clocks are used in the system as general-purpose clocks.

Clock Generation and PLL

The TLV320DAC3203 supports a wide range of options for generating clocks for the DAC as well as interface and other control blocks. The clocks for the DAC require a source reference clock. This clock can be provided on a variety of device pins such as MCLK, BCLK, or GPIO pins. The CODEC_CLKIN can then be routed through highly-flexible clock dividers to generate the various clocks required for the DAC sections. In the event that the desired audio clocks cannot be generated from the reference clocks on MCLK, BCLK, or GPIO, the TLV320DAC3203 also provides the option of using the on-chip PLL, which supports a wide range of fractional multiplication values to generate the required clocks. Starting from CODEC_CLKIN the TLV320DAC3203 provides several programmable clock dividers to help achieve a variety of sampling rates for the DAC.

For more detailed information see the *TLV320DAC3203 Application Reference Guide*.

Control Interfaces

The TLV320DAC3203 control interface supports SPI or I^2C communication protocols, with the protocol selectable using the SPI_SELECT pin. For SPI, SPI_SELECT should be tied high; for I^2C, SPI_SELECT should be tied low. It is not recommended to change the state of SPI_SELECT during device operation.

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I²C Control

The TLV320DAC3203 supports the I²C control protocol, and will respond to the I²C address of 0011000. I²C is a two-wire, open-drain interface supporting multiple devices and masters on a single bus. Devices on the I²C bus only drive the bus lines LOW by connecting them to ground; they never drive the bus lines HIGH. Instead, the bus wires are pulled HIGH by pullup resistors, so the bus wires are HIGH when no device is driving them LOW. This way, two devices cannot conflict; if two devices drive the bus simultaneously, there is no driver contention.

SPI Control

In the SPI control mode, the TLV320DAC3203 uses the pins SCL/$\overline{SS}$ as $\overline{SS}$, SCLK as SCLK, MISO as MISO, SDA/MOSI as MOSI; a standard SPI port with clock polarity setting of 0 (typical microprocessor SPI control bit CPOL = 0). The SPI port allows full-duplex, synchronous, serial communication between a host processor (the master) and peripheral devices (slaves). The SPI master (in this case, the host processor) generates the synchronizing clock (driven onto SCLK) and initiates transmissions. The SPI slave devices (such as the TLV320DAC3203) depend on a master to start and synchronize transmissions. A transmission begins when initiated by an SPI master. The byte from the SPI master begins shifting in on the slave MOSI pin under the control of the master serial clock (driven onto SCLK). As the byte shifts in on the MOSI pin, a byte shifts out on the MISO pin to the master shift register.

For more detailed information see the *TLV320DAC3203 Application Reference Guide*.

Power Supply

For more detailed information see the *TLV320DAC3203 Application Reference Guide*.

Device Special Functions

The following special functions are available to support advanced system requirements:

- Headset detection
- Interrupt generation
- Flexible pin multiplexing

For more detailed information see the *TLV320DAC3203 Application Reference Guide*.

Register Map Summary

Table 10. Summary of Register Map

Decimal		Hex		DESCRIPTION
PAGE NO.	REG. NO.	PAGE NO.	REG. NO.	
0	0	0x00	0x00	Page Select Register
0	1	0x00	0x01	Software Reset Register
0	2	0x00	0x02	Reserved Register
0	3	0x00	0x03	Reserved Register
0	4	0x00	0x04	Clock Setting Register 1, Multiplexers
0	5	0x00	0x05	Clock Setting Register 2, PLL P&R Values
0	6	0x00	0x06	Clock Setting Register 3, PLL J Values
0	7	0x00	0x07	Clock Setting Register 4, PLL D Values (MSB)
0	8	0x00	0x08	Clock Setting Register 5, PLL D Values (LSB)
0	9-10	0x00	0x09-0x0A	Reserved Register
0	11	0x00	0x0B	Clock Setting Register 6, NDAC Values
0	12	0x00	0x0C	Clock Setting Register 7, MDAC Values
0	13	0x00	0x0D	DAC OSR Setting Register 1, MSB Value
0	14	0x00	0x0E	DAC OSR Setting Register 2, LSB Value
0	15-17	0x00	0x0F-0x11	Reserved Register
0	18	0x00	0x12	Clock Setting Register 8, NADC Values
0	19	0x00	0x13	Clock Setting Register 9, MADC Values

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Table 10. Summary of Register Map (continued)

Decimal		Hex		DESCRIPTION
PAGE NO.	REG. NO.	PAGE NO.	REG. NO.	
0	20-24	0x00	0x14-0x18	Reserved Register
0	25	0x00	0x19	Clock Setting Register 10, Multiplexers
0	26	0x00	0x1A	Clock Setting Register 11, CLKOUT M divider value
0	27	0x00	0x1B	Audio Interface Setting Register 1
0	28	0x00	0x1C	Audio Interface Setting Register 2, Data offset setting
0	29	0x00	0x1D	Audio Interface Setting Register 3
0	30	0x00	0x1E	Clock Setting Register 12, BCLK N Divider
0	31	0x00	0x1F	Audio Interface Setting Register 4, Secondary Audio Interface
0	32	0x00	0x20	Audio Interface Setting Register 5
0	33	0x00	0x21	Audio Interface Setting Register 6
0	34	0x00	0x22	Digital Interface Misc. Setting Register
0	35-36	0x00	0x23-0x24	Reserved Register
0	37	0x00	0x25	DAC Flag Register 1
0	38	0x00	0x26	DAC Flag Register 2
0	39-41	0x00	0x27-0x29	Reserved Register
0	42	0x00	0x2A	Sticky Flag Register 1
0	43	0x00	0x2B	Interrupt Flag Register 1
0	44	0x00	0x2C	Sticky Flag Register 2
0	45	0x00	0x2D	Sticky Flag Register 3
0	46	0x00	0x2E	Interrupt Flag Register 2
0	47	0x00	0x2F	Interrupt Flag Register 3
0	48	0x00	0x30	INT1 Interrupt Control Register
0	49	0x00	0x31	INT2 Interrupt Control Register
0	50-51	0x00	0x32-0x33	Reserved Register
0	52	0x00	0x34	GPIO/MFP5 Control Register (YZK Package only)
0	53	0x00	0x35	MFP2 Function Control Register
0	54	0x00	0x36	DIN/MFP1 Function Control Register
0	55	0x00	0x37	MISO/MFP4 Function Control Register
0	56	0x00	0x38	SCLK/MFP3 Function Control Register
0	57-59	0x00	0x39-0x3B	Reserved Registers
0	60	0x00	0x3C	DAC Signal Processing Block Control Register
0	61-62	0x00	0x3D-0x3E	Reserved Register
0	63	0x00	0x3F	DAC Channel Setup Register 1
0	64	0x00	0x40	DAC Channel Setup Register 2
0	65	0x00	0x41	Left DAC Channel Digital Volume Control Register
0	66	0x00	0x42	Right DAC Channel Digital Volume Control Register
0	67	0x00	0x43	Headset Detection Configuration Register
0	68	0x00	0x44	DRC Control Register 1
0	69	0x00	0x45	DRC Control Register 2
0	70	0x00	0x46	DRC Control Register 3
0	71	0x00	0x47	Beep Generator Register 1
0	72	0x00	0x48	Beep Generator Register 2
0	73	0x00	0x49	Beep Generator Register 3
0	74	0x00	0x4A	Beep Generator Register 4
0	75	0x00	0x4B	Beep Generator Register 5
0	76	0x00	0x4C	Beep Generator Register 6

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Table 10. Summary of Register Map (continued)

Decimal		Hex		DESCRIPTION
PAGE NO.	REG. NO.	PAGE NO.	REG. NO.	
0	77	0x00	0x4D	Beep Generator Register 7
0	78	0x00	0x4E	Beep Generator Register 8
0	79	0x00	0x4F	Beep Generator Register 9
0	80-127	0x00	0x50-0x7F	Reserved Register
1	0	0x01	0x00	Page Select Register
1	1	0x01	0x01	Power Configuration Register
1	2	0x01	0x02	LDO Control Register
1	3	0x01	0x03	Playback Configuration Register 1
1	4	0x01	0x04	Playback Configuration Register 2
1	5-8	0x01	0x05-0x08	Reserved Register
1	9	0x01	0x09	Output Driver Power Control Register
1	10	0x01	0x0A	Common Mode Control Register
1	11	0x01	0x0B	Over Current Protection Configuration Register
1	12	0x01	0x0C	HPL Routing Selection Register
1	13	0x01	0x0D	HPR Routing Selection Register
1	14-15	0x01	0x0E-0x0F	Reserved Register
1	16	0x01	0x10	HPL Driver Gain Setting Register
1	17	0x01	0x11	HPR Driver Gain Setting Register
1	18-19	0x01	0x12-0x13	Reserved Register
1	20	0x01	0x14	Headphone Driver Startup Control Register
1	21	0x01	0x15	Reserved Register
1	22	0x01	0x16	INL to HPL Volume Control Register
1	23	0x01	0x17	INR to HPR Volume Control Register
1	24-50	0x01	0x18-0x32	Reserved Register
1	51	0x01	0x33	MICBIAS Configuration Register
1	52-57	0x01	0x34-0x39	Reserved Register
1	58	0x01	0x3A	Analog Input Settings
1	59-62	0x01	0x3B-0x3E	Reserved Register
1	63	0x01	0x3F	DAC Analog Gain Control Flag Register
1	64-122	0x01	0x40-0x7A	Reserved Register
1	123	0x01	0x7B	Reference Power-up Configuration Register
1	124	0x01	0x7C	Reserved Register
1	125	0x01	0x7D	Offset Callibration Register
1	126-127	0x01	0x7E-0x7F	Reserved Register
8	0-127	0x08	0x00-0x7F	Reserved Register
9-16	0-127	0x09-0x10	0x00-0x7F	Reserved Register
26-34	0-127	0x1A-0x22	0x00-0x7F	Reserved Register
44	0	0x2C	0x00	Page Select Register
44	1	0x2C	0x01	DAC Adaptive Filter Configuration Register
44	2-7	0x2C	0x02-0x07	Reserved
44	8-127	0x2C	0x08-0x7F	DAC Coefficients Buffer-A C(0:29)
45-52	0	0x2D-0x34	0x00	Page Select Register
45-52	1-7	0x2D-0x34	0x01-0x07	Reserved.
45-52	8-127	0x2D-0x34	0x08-0x7F	DAC Coefficients Buffer-A C(30:255)
62-70	0	0x3E-0x46	0x00	Page Select Register
62-70	1-7	0x3E-0x46	0x01-0x07	Reserved.

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Table 10. Summary of Register Map (continued)

Decimal		Hex		DESCRIPTION
PAGE NO.	REG. NO.	PAGE NO.	REG. NO.	
62-70	8-127	0x3E-0x46	0x08-0x7F	DAC Coefficients Buffer-B C(0:255)
80-114	0-127	0x50-0x72	0x00-0x7F	Reserved Register
152-186	0-127	0x98-0xBA	0x00-0x7F	Reserved Register

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV320DAC3203IRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	DAC 3203I	Samples
TLV320DAC3203IRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	DAC 3203I	Samples
TLV320DAC3203IYZKR	ACTIVE	DSBGA	YZK	25	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	DAC3203I	Samples
TLV320DAC3203IYZKT	ACTIVE	DSBGA	YZK	25	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	DAC3203I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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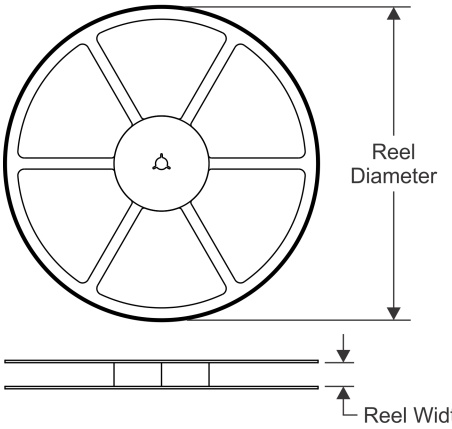
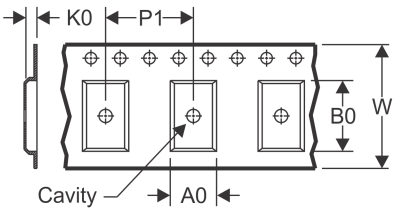
TAPE AND REEL INFORMATION

REEL DIMENSIONS

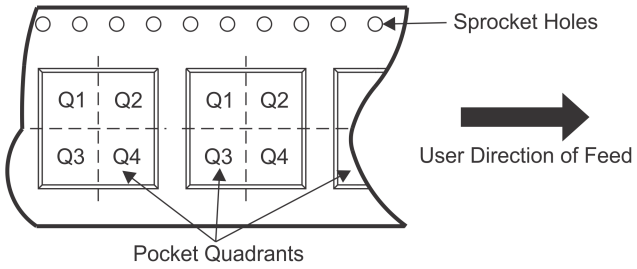


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

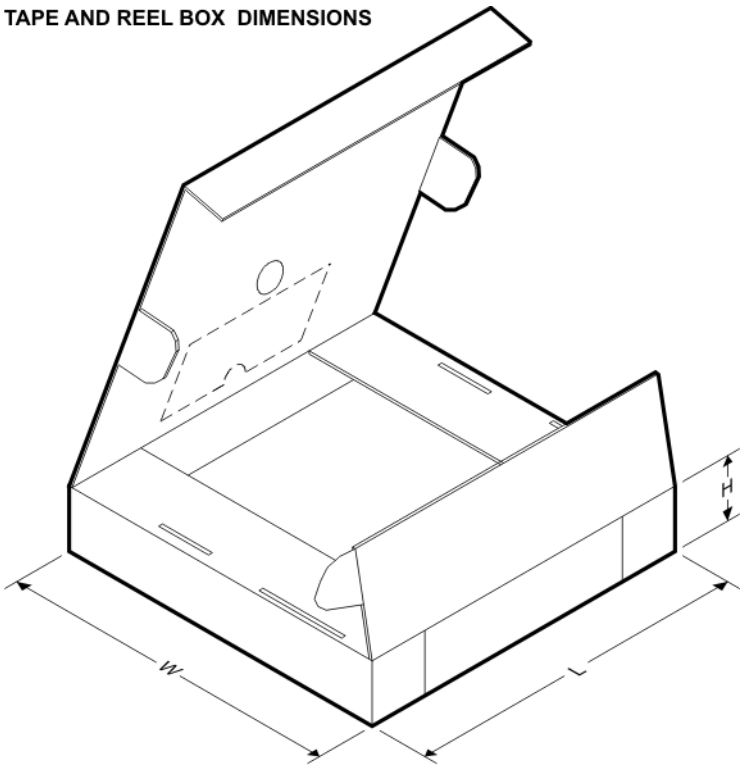
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV320DAC3203IRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV320DAC3203IRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV320DAC3203IRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV320DAC3203IYZKR	DSBGA	YZK	25	3000	180.0	8.4	2.75	2.75	0.81	4.0	8.0	Q1
TLV320DAC3203IYZKT	DSBGA	YZK	25	250	180.0	8.4	2.75	2.75	0.81	4.0	8.0	Q1

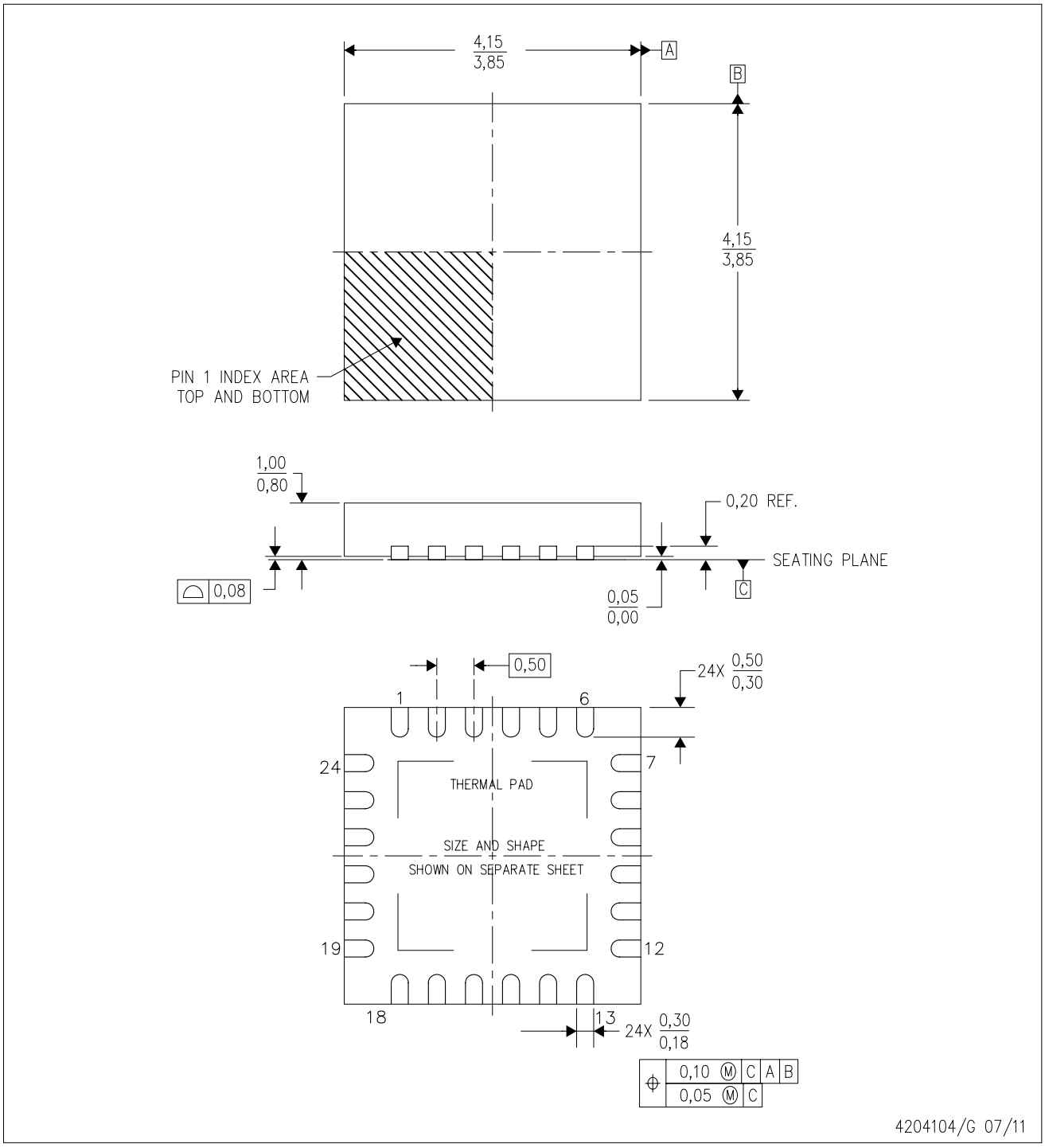
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV320DAC3203IRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TLV320DAC3203IRGET	VQFN	RGE	24	250	210.0	185.0	35.0
TLV320DAC3203IRGET	VQFN	RGE	24	250	210.0	185.0	35.0
TLV320DAC3203IYZKR	DSBGA	YZK	25	3000	182.0	182.0	20.0
TLV320DAC3203IYZKT	DSBGA	YZK	25	250	182.0	182.0	20.0

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

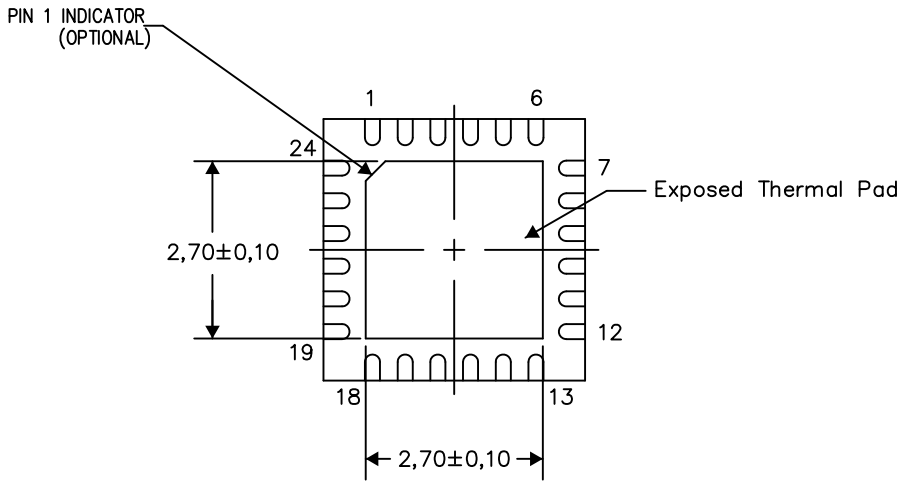
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



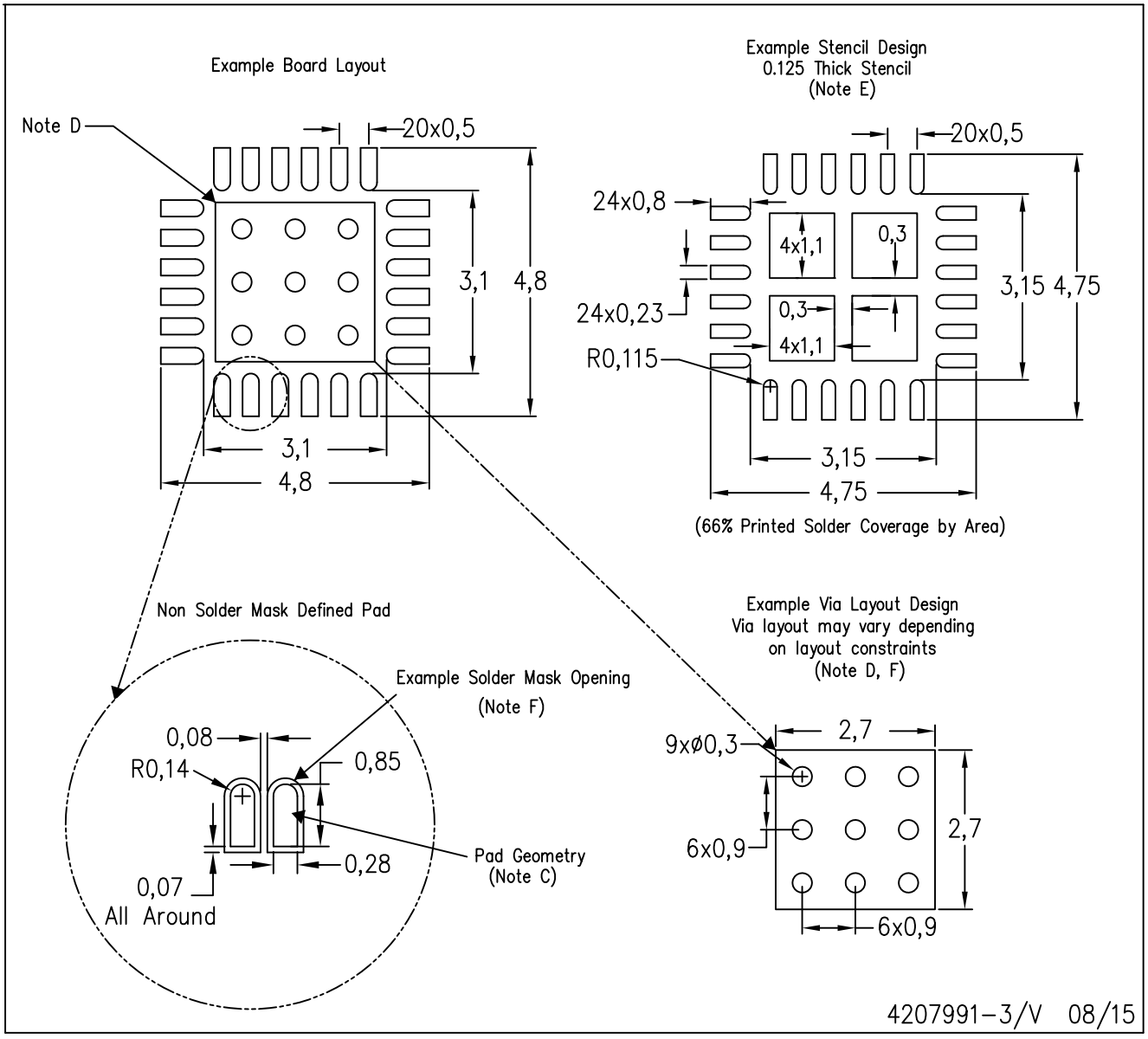
Bottom View

Exposed Thermal Pad Dimensions

4206344–5/AK 08/15

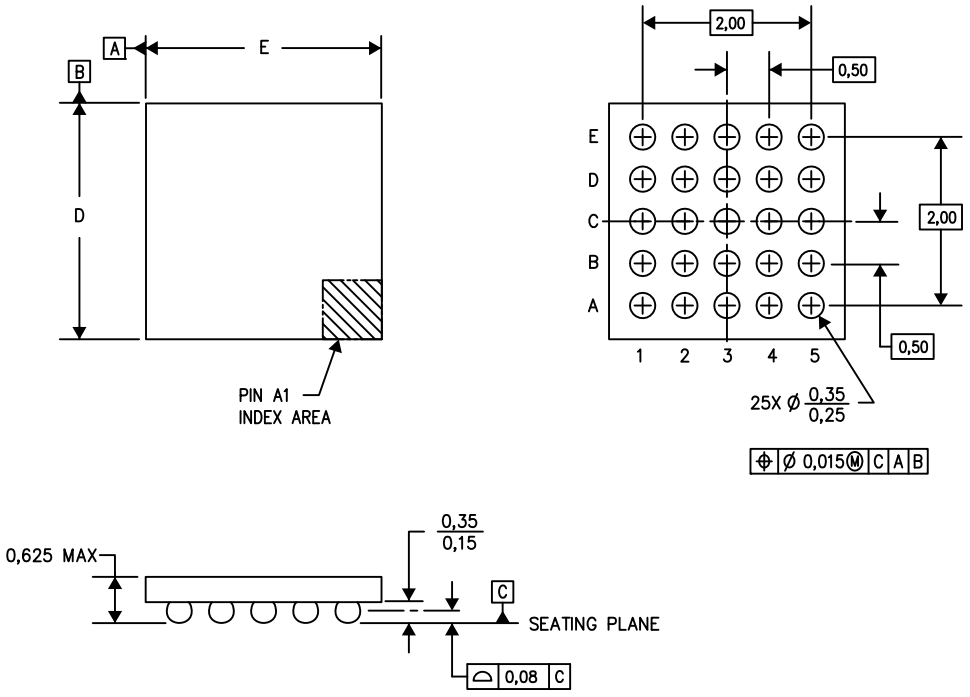
NOTES: A. All linear dimensions are in millimeters

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

YZK (S–XBGA–N25) DIE–SIZE BALL GRID ARRAY



D: Max = 2.67 mm, Min = 2.61 mm

E: Max = 2.67 mm, Min = 2.61 mm

4205062–3/F 07/13

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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