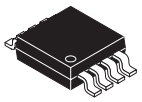


SLUS562A − JUNE 2003 − REVISED SEPTEMBER 2003

−48-V HOT SWAP CONTROLLER FOR REDUNDANT-SUPPLY SYSTEMS

FEATURES

- **Wide Input Supply Range: −36 V to −80 V**
- **Transient Rating to −100 V**
- **Improved Transient Response**
- **Enable Input (EN)**
- **Programmable Current Limit**
- **Programmable Current Slew Rate**
- **Fault Timer to Eliminate Nuisance Trips**
- **Open-Drain Power Good Output ($\overline{PG}$)**
- **8-Pin MSOP Package**

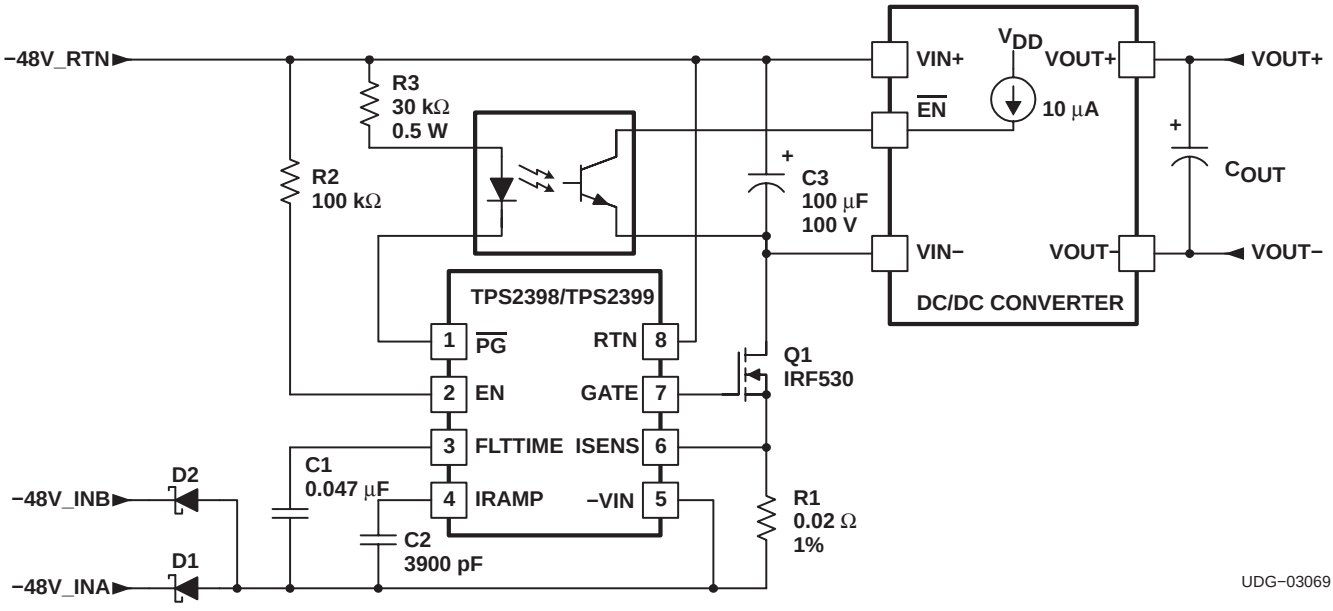
APPLICATIONS

- **−48-V Distributed Power Systems**
- **Redundant Negative Voltage Supplies**
- **Central Office Switching**

DESCRIPTION

The TPS2398 and TPS2399 integrated circuits are hot swap power managers optimized for use in nominal −48-V systems. For redundant-supply systems, they incorporate an improved circuit breaker response that provides rapid protection from short circuits, while still enabling plug-ins to tolerate large transients that can be generated by the sudden switchover to a higher voltage supply. They are designed for supply voltage ranges up to −80 V, and are rated to withstand spikes to −100 V. In conjunction with an external N-channel FET and sense resistor, they can be used to enable live insertion of plug-in cards and modules in powered systems. Both devices provide load current slew rate and peak magnitude limiting, easily programmed by sense resistor value and a single-external capacitor.

APPLICATION DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DESCRIPTION (continued)

They also provide single-line fault reporting, electrical isolation of faulty cards, and protection against nuisance overcurrent trips. The TPS2398 latches off in response to current faults, while the TPS2399 periodically retries the load in the event of a fault.

ABSOLUTE MAXIMUM RATINGS (See Note 1)

	TPS2398/1	UNIT
Input voltage range, all pins except RTN, EN, $\overline{PG}$(2)	−0.3 V to 15	V
Input voltage range, RTN(2)	−0.3 V to 100	V
Input voltage range, EN(2)(3)	−0.3 V to 100	V
Output voltage range, $\overline{PG}$(2)(4)	−0.3 V to 100	V
Continuous output current, $\overline{PG}$	10	mA
Continuous total power dissipation	see Dissipation Rating Table	
Operating junction temperature range, T_J	−55°C to 125°C	°C
Storage temperature range, T_{stg}	−65°C to 150°C	°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds	260°C	°C

NOTES 1: Stresses beyond those listed under ”absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under ”recommended operating conditions” is not implied. Exposure to absolute−maximum−rated conditions for extended periods may affect device reliability.
2: All voltages are with respect to −VIN (unless otherwise noted).
3: With 100-kΩ minimum input series resistance, −0.3 V to 15 V with low impedance.
4: With 10-kΩ minimum series resistance, −0.3 V to 80 V with low impedance.

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

	MIN	UNIT
Human Body Model (HBM)	1.5	kV
Charged Device Model (CDM)	1.5	kV

RECOMMENDED OPERATING CONDITIONS†

	MIN	NOM	MAX	UNIT
Nominal input supply, −VIN to RTN	−80		−36	V
Operating junction temperature range	−40		85	°C

† All voltages are with respect to −VIN (unless otherwise noted)

DISSIPATION RATING TABLE

PACKAGE	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
MSOP-8	420 mW	4.3 mW/°C	160 mW

AVAILABLE OPTIONS

OPERATING T_A	FAULT OPERATION	PACKAGED DEVICES MSOP (DGK)
−40°C to 85°C	Latch off	TPS2398DGK
	Periodically retry	TPS2399DGK

ELECTRICAL CHARACTERISTICS

$V_{I(-VIN)}$ = −48 V with respect to RTN, $V_{I(EN)}$ = 2.8 V, $V_{I(ISENS)}$ = 0, all outputs unloaded, T_A = −40°C to 85°C (unless otherwise noted)(1)(2)

input supply

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Supply current, RTN	$V_{I(RTN)}$ = 48 V		700	1000	µA
I_{CC2}	Supply current, RTN	$V_{I(RTN)}$ = 80 V		1000	1500	µA
V_{UVLO_L}	UVLO threshold, input voltage rising	To GATE pull-up, referenced to RTN	−36	−30	−25	V
V_{HYS}	UVLO hysteresis		1.8	2.3	3.0	V

enable input (EN)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{TH}	Threshold voltage, input voltage rising	To GATE pull-up	1.3	1.4	1.5	V
V_{HYS_EN}	EN hysteresis		22	60	90	mV
I_{IH}	High-level input current	$V_{I(EN)}$ = 5 V	−2	1	2	µA

linear current amplifier (LCA)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output, GATE	$V_{I(ISENS)}$ = 0 V	11	14	17	V
I_{SINK}	Output sink current	$V_{I(ISENS)}$ = 80 mV, $V_{O(GATE)}$ = 5V, Fault mode	50	100		mA
I_I	Input current, ISENS	0 V < $V_{I(ISENS)}$ < 0.2 V	−1		1	µA
V_{REF_K}	Reference clamp voltage	$V_{O(IRAMP)}$ = open	33	40	46	mV
V_{IO}	Input offset voltage	$V_{O(IRAMP)}$ = 2 V	−7		6	mV

ramp generator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SRC1}	IRAMP source current, slow turn-on rate	$V_{O(IRAMP)}$ = 0.25 V	−850	−600	−400	nA
I_{SRC2}	IRAMP source current, normal rate	$V_{O(IRAMP)}$ = 1 V, 3 V	−11	−10	−9	µA
V_{OL}	Low-level output voltage	$V_{I(EN)}$ = 0 V			5	mV
A_V	Voltage gain, relative to ISENS	$V_{O(IRAMP)}$ = 1 V, 3 V	9.5	10.0	10.5	mV/V

overload comparator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{TH_OL}	Current overload threshold, ISENS		80	100	120	mV
t_{DLY}	Glitch filter delay time	$V_{I(ISENS)}$ = 200 mV	2	4	7	µs

fault timer

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage		V_I(EN) = 0 V			5	mV
I_{CHG}	Charging current, current limit mode		$V_{I(ISENS)}$ = 80 mV, $V_{O(FLTTIME)}$ = 2 V	−55	−50	−45	µA
V_{FLT}	Fault threshold voltage			3.75	4.00	4.25	V
I_{DSG}	Discharge current, retry mode	TPS2399	$V_{I(ISENS)}$ = 80 mV, $V_{O(FLTTIME)}$ = 2 V		0.38	0.75	µA
D	Output duty cycle	TPS2399			1	1.5	%
I_{RST}	Discharge current, timer reset mode		$V_{O(FLTTIME)}$ = 2 V,$V_{I(ISENS)}$ = 0 V		1		mA

NOTES 1: All voltages are with respect to the −VIN terminal unless otherwise stated.
2: Currents are positive into and negative out of the specified terminal.

ELECTRICAL CHARACTERISTICS (continued)

$V_{I(-VIN)}$ = −48 V with respect to RTN, $V_{I(EN)}$ = 2.8 V, $V_{I(ISENS)}$ = 0, all outputs unloaded, T_A = −40°C to 85°C (unless otherwise noted)(1)(2)

$\overline{PG}$ output

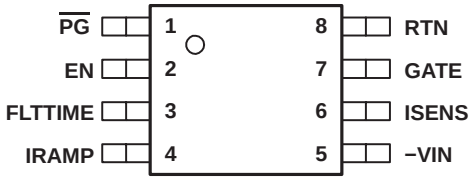
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OH}	High-level output (leakage) current	$V_{I(EN)}$ = 0 V, $V_{O(\overline{PG})}$ = 65 V			10	μA
$R_{DS(ON)}$	Driver ON resistance	$V_{I(\overline{ISENS})}$ = 80 mV, $V_{O(FLTTIME)}$ = 5V, $I_{O(PG)}$ = 1 mA		35	80	Ω

NOTES 1: All voltages are with respect to the −VIN terminal unless otherwise stated.
2: Currents are positive into and negative out of the specified terminal.

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
EN	2	I	Enable input to turn on/off power to the load.
$\overline{PG}$	1	O	Open-drain, active-low indication of a load power good condition.
FLTTIME	3	I/O	Connection for user-programming of the fault timeout period.
GATE	7	O	Gate drive for external N-channel FET.
IRAMP	4	I/O	Programming input for setting the inrush current slew rate.
ISENS	6	I	Current sense input.
RTN	8	I	Positive supply input for the TPS2398 and TPS2399.
−VIN	5	I	Negative supply input and reference pin for the TPS2398 and TPS2399.

DGK PACKAGE
(TOP VIEW)



DETAILED PIN DESCRIPTIONS

EN: Enable input to turn on/off power to the load. The EN pin is referenced to the −VIN potential of the circuit. When this input is pulled high (above the nominal 1.4-V threshold) the device enables the GATE output, and begins the ramp of current to the load. When this input is low, the linear current amplifier (LCA) is disabled, and a large pull-down device is applied to the FET gate, disabling power to the load.

FLTTIME: Connection for user-programming of the fault timeout period. An external capacitor connected from FLTTIME to −VIN establishes the timeout period to declare a fault condition. This timeout protects against indefinite current sourcing into a faulted load, and also provides a filter against nuisance trips from momentary current spikes or surges. The TPS2398 and TPS2399 define a fault condition as voltage at the ISENS pin at or greater than the 40-mV fault threshold. When a fault condition exists, the timer is active. The devices manage fault timing by charging the external capacitor to the 4-V fault threshold, then subsequently discharging it to reset the timer (TPS2398), or discharging it at approximately 1% the charge rate to establish the duty cycle for retrying the load (TPS2399). Whenever the internal fault latch is set (timer expired), the pass FET is rapidly turned off, and the $\overline{\text{PG}}$ output is deasserted.

GATE: Gate drive for external N-channel FET. When enabled, and the input supply is above the UVLO threshold, the gate drive is enabled and the device begins charging an external capacitor connected to the IRAMP pin. This pin voltage is used to develop the reference voltage at the non-inverting input of the internal LCA. The inverting input is connected to the current sense node, ISENS. The LCA acts to slew the pass FET gate to force the ISENS voltage to track the reference. The reference is internally clamped at 40 mV, so the maximum current that can be sourced to the load is determined by the sense resistor value as IMAX $\leq$ 40 mV/R_{SENSE}. Once the load voltage has ramped up to the input dc potential, and current demand drops off, the LCA drives the GATE output to about 14 V to fully enhance the pass FET, completing the low-impedance supply return path for the load.

IRAMP: Programming input for setting the inrush current slew rate. An external capacitor connected between this pin and −VIN establishes the load current slew rate whenever power to the load is enabled. The device charges the external capacitor to establish the reference input to the LCA. The closed-loop control of the LCA and pass FET acts to maintain the current sense voltage at ISENS at the reference potential. Since the sense voltage is developed as the drop across a resistor, the charging current ramp rate is set by the voltage ramp rate at the IRAMP pin. When the output is disabled via the EN input or due to a load fault, the capacitor is discharged and held low to initialize for the next turn-on.

ISENS: Current sense input. An external low value resistor connected between this pin and −VIN is used to feed back current magnitude information to the TPS2398/99. There are two internal device thresholds associated with the voltage at the ISENS pin. During charging of the load's input capacitance, or during other periods of excessive demand, the HSPM acts to limit this voltage to 40 mV. Whenever the LCA is in current regulation mode, the capacitor at FLTTIME is charged to activate the timer. If, when the LCA is driving to its supply rail, a fast-acting fault such as a short-circuit, causes the ISENS voltage to exceed 100 mV (the overload threshold), the GATE pin is pulled low rapidly, bypassing the fault timer.

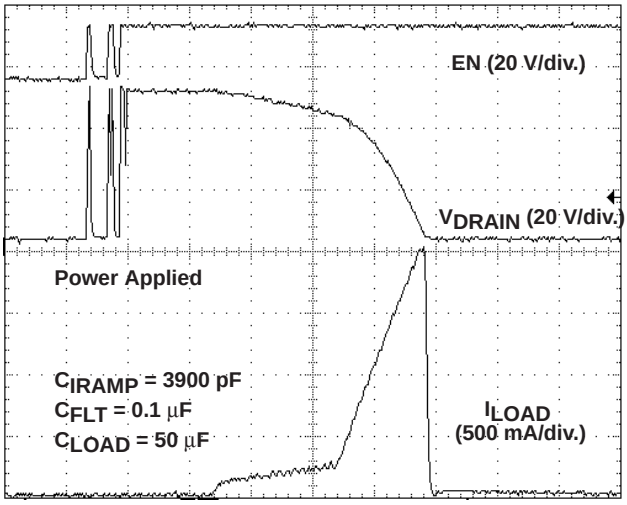
$\overline{\text{PG}}$: Open-drain, active-low indication of load power good. A power good status is declared when the output is enabled, the GATE pin voltage has ramped to at least 7 V, and the voltage on the IRAMP pin exceeds approximately 5 V. This last condition assures that full programmed sourcing current is available prior to declaring power good, even with very slow current ramp rates. This additional protection prevents potential discharging of the module input bulk capacitance during load turn-on.

RTN: Positive supply input for the TPS2398/99. For negative voltage systems, the supply pin connects directly to the return node of the input power bus. Internal regulators step down the input voltage to generate the various supply levels used by the TPS2398 and TPS2399.

−VIN: Negative supply input and reference pin for the TPS2398/99. This pin connects directly to the input supply negative rail. The input and output pins and all internal circuitry are referenced to this pin, so it is essentially the GND or VSS pin of the device.

TYPICAL CHARACTERISTICS

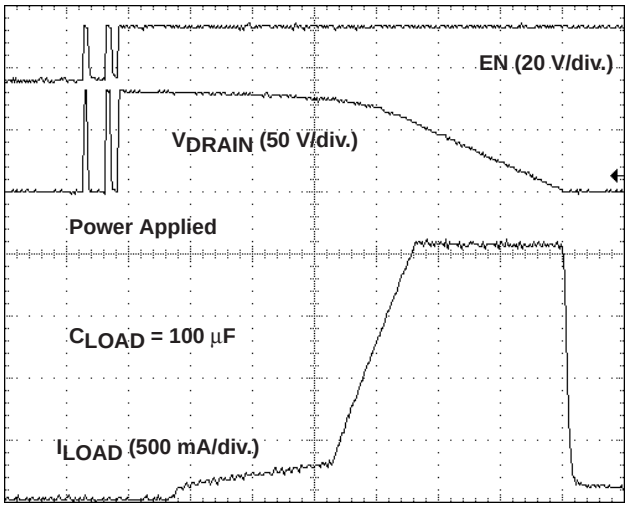
LIVE INSERTION EVENT
VIN = −48 V



t − TIme − 1 ms/div

Figure 1

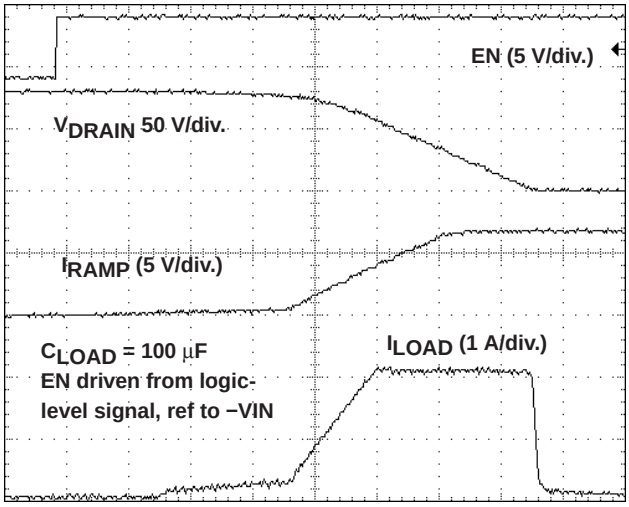
LIVE INSERTION EVENT
VIN = −80 V



t − TIme − 1 ms/div

Figure 2

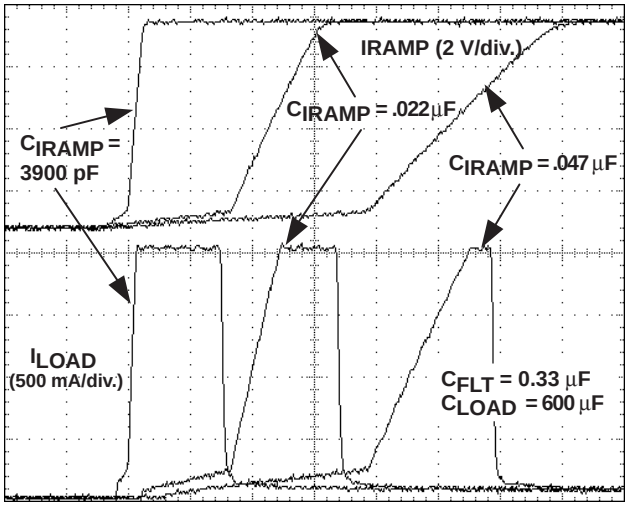
START-UP FROM ENABLE ASSERTION



t − TIme − 1 ms/div

Figure 3

LOAD CURRENT RAMP PROFILES



t − TIme − 10 ms/div

Figure 4

TYPICAL CHARACTERISTICS

TURN-ON INTO SHORTED LOAD (TPS2399)

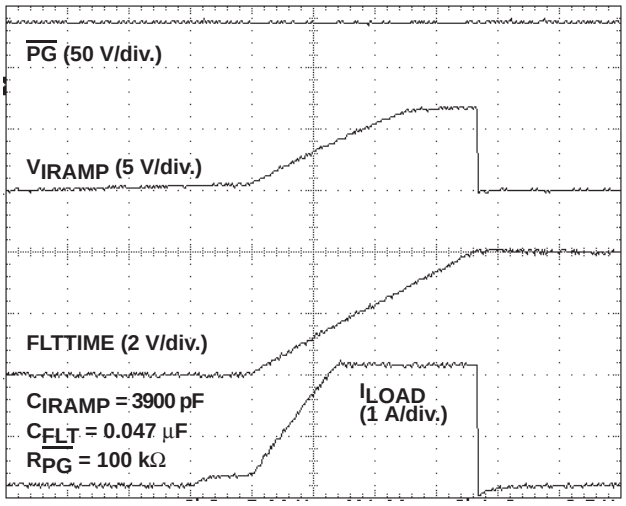


Figure 5

TURN-ON INTO SHORTED LOAD (TPS2398)

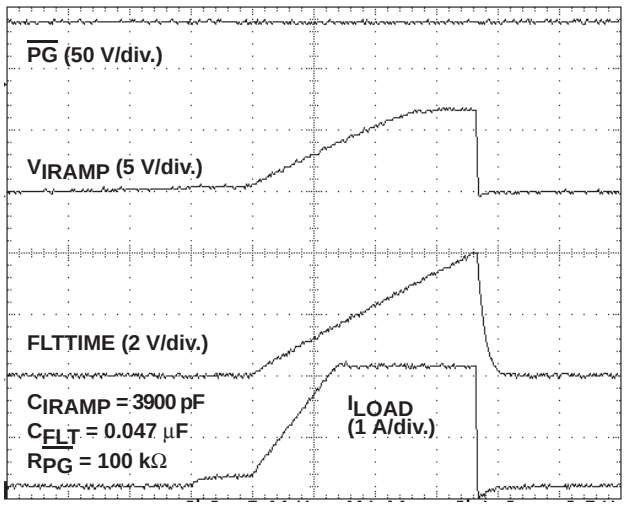


Figure 6

FAULT RETRY OPERATION (TPS2399)

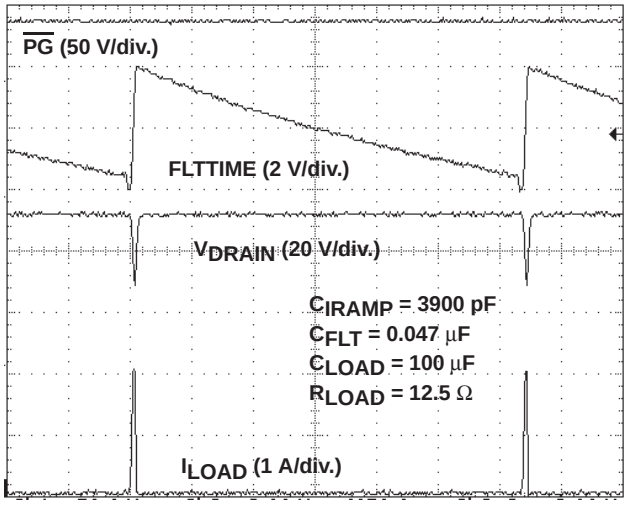


Figure 7

RECOVERY FROM A FAULT − LARGE SCALE VIEW (TPS2399)

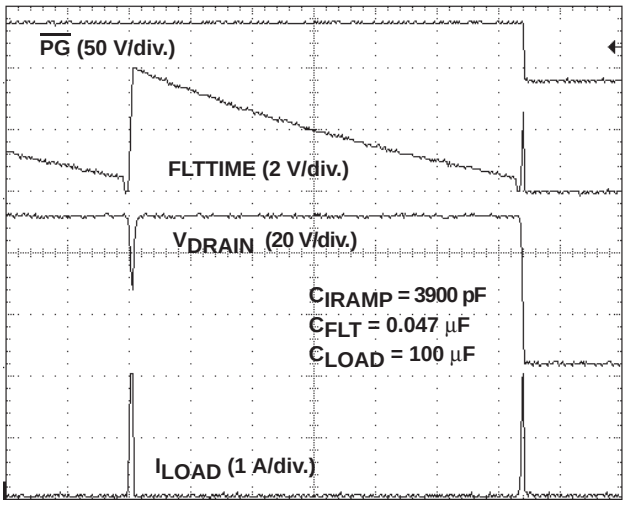


Figure 8

TYPICAL CHARACTERISTICS

RECOVERY FROM A FAULT − EXPANDED VIEW (TPS2399)

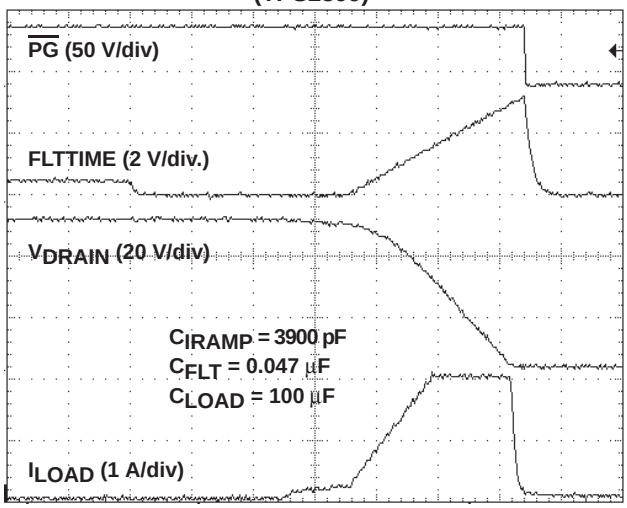


Figure 9

PG OUTPUT TIMING, VOLTAGE QUALIFIED

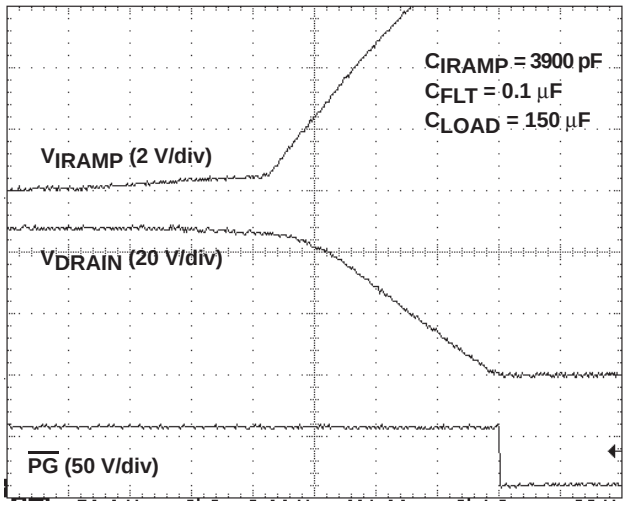


Figure 10

PG OUTPUT TIMING, CURRENT QUALIFIED

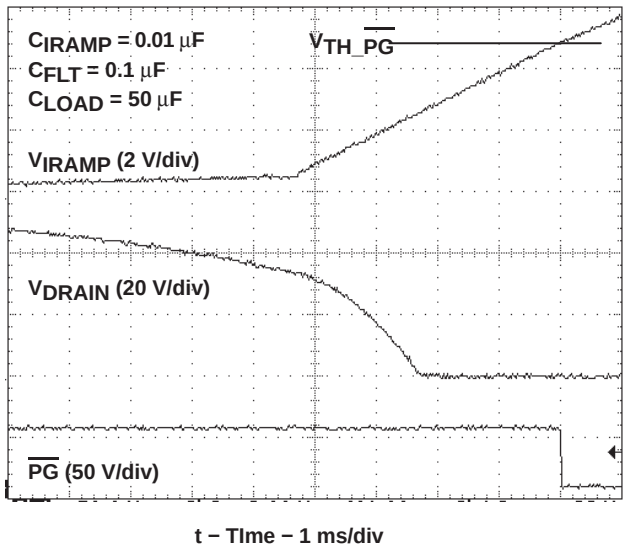


Figure 11

SUPPLY CURRENT vs AMBIENT TEMPERATURE

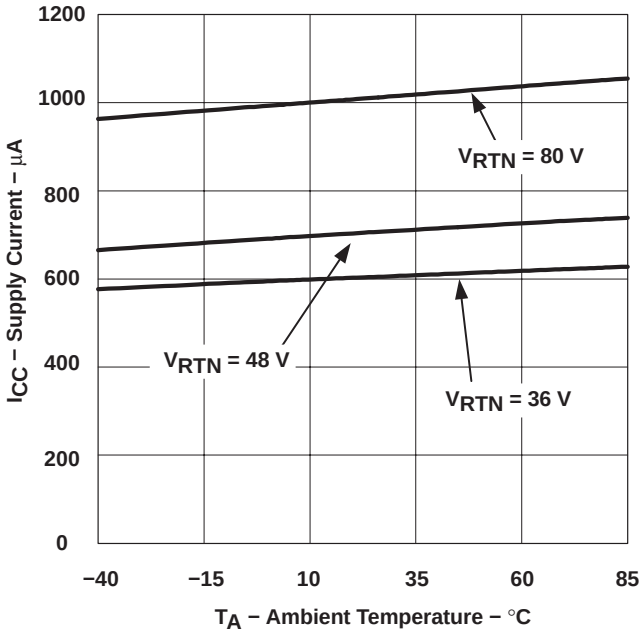


Figure 12

TYPICAL CHARACTERISTICS

GATE HIGH-LEVEL OUTPUT vs AMBIENT TEMPERATURE

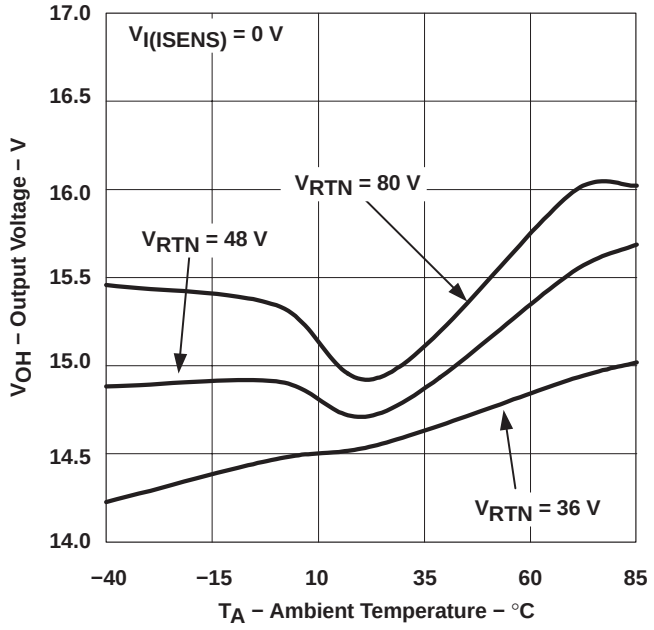


Figure 13

IRAMP OUTPUT CURRENT vs AMBIENT TEMPERATURE, SLOW TURN-ON

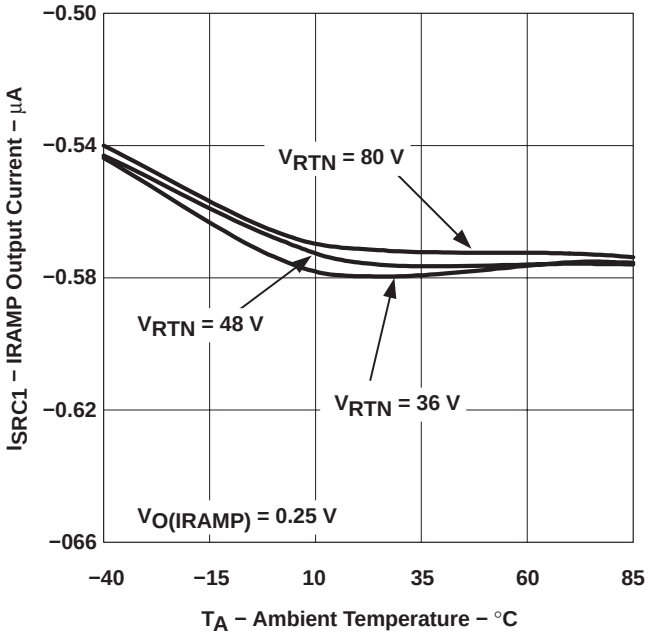


Figure 14

IRAMP OUTPUT CURRENT vs AMBIENT TEMPERATURE, NORMAL RATE

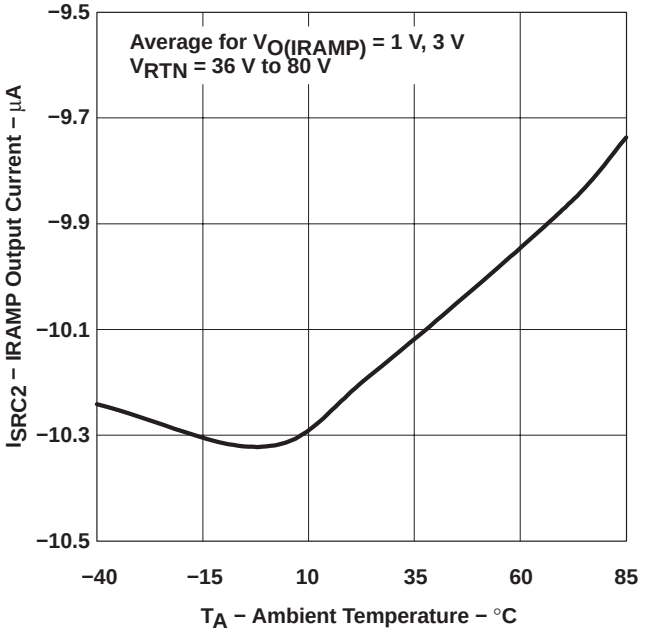


Figure 15

TIMER CHARGING CURRENT vs AMBIENT TEMPERATURE

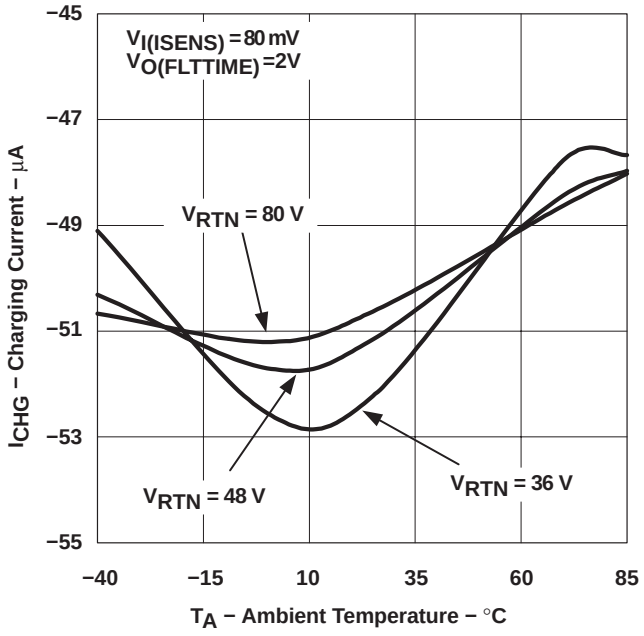


Figure 16

TYPICAL CHARACTERISTICS

FLTTIME DISCHARGE CURRENT vs AMBIENT TEMPERATURE (TPS2399)

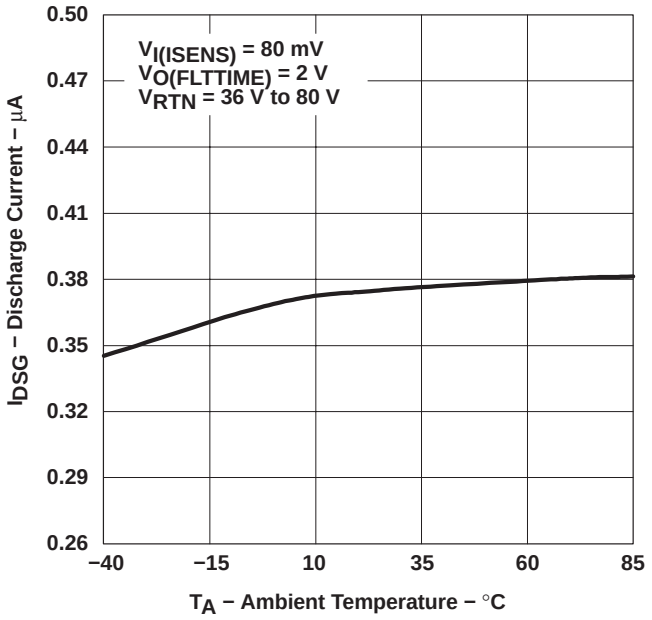


Figure 17

FAULT LATCH THRESHOLD vs AMBIENT TEMPERATURE

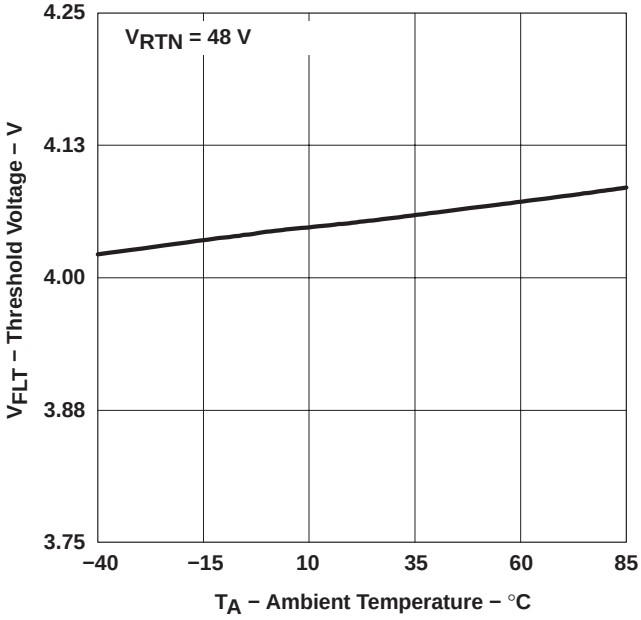


Figure 18

APPLICATION INFORMATION

When a plug-in module or printed circuit card is inserted into a live chassis slot, discharged supply bulk capacitance on the board can draw huge transient currents from the system supplies. Without some form of inrush limiting, these currents can reach peak magnitudes ranging up to several hundred amps, particularly in high-voltage systems. Such large transients can damage connector pins, PCB etch, and plug-in and supply components. In addition, current spikes can cause voltage droops on the power distribution bus, causing other boards in the system to reset.

The TPS2398 and TPS2399 are hot swap power managers designed to limit these peaks to preset levels, as well as control the slew rate (di/dt) at which charging current ramps to the user-programmed limit. These devices use an external N-Channel pass FET and sense element to provide closed-loop control of current sourced to the load. Input supply undervoltage lockout (UVLO) protection allows hot swap circuits to turn on automatically with the application of power, or to be controlled with a system command via the EN input. External capacitors control both the current ramp rate, and the time−out period for load voltage ramping. In addition, an internal overload comparator provides circuit breaker protection against shorts occurring during steady-state (post-turn-on) operation of the card.

The TPS2398 and TPS2399 operate directly from the input supply (nominal −48 VDC rail). The −VIN pin connects to the negative voltage rail, and the RTN pin connects to the supply return. Internal regulators convert input power to the supply levels required by the device circuitry. An input UVLO circuit holds the GATE output low until the supply voltage reaches a nominal 30-V level. A second comparator monitors the EN input; this pin must be pulled above the 1.4-V enable threshold to turn on power to the load.

Once enabled, and when the input supply is above the UVLO threshold, the GATE pull-down is removed, the linear control amplifier (LCA) is enabled, and a large discharge device in the RAMP CONTROL block is turned off. Subsequently, a small current source is now able to charge an external capacitor connected to the IRAMP pin. This results in a linear voltage ramp at IRAMP. The voltage ramp on the capacitor actually has two discrete slopes. As shown in Figure 17, charging current is supplied from either of two sources. Initially at turn-on, the 600-nA source is selected, to provide a slow turn-on rate. This slow turn-on helps ensure that the LCA is pulled out of saturation, and is slewing to the voltage at its non-inverting input before normal rate load charging is allowed. This mechanism helps reduce current steps at turn-on. Once the voltage at the IRAMP pin reaches approximately 0.5 V, an internal comparator deasserts the SLOW signal, and the 10-μA source is selected for the remainder of the ramp period.

The voltage at IRAMP is divided down by a factor of 100, and applied to the non-inverting input of the LCA. Load current magnitude information at the ISENS pin is applied to the inverting input. This voltage is developed by connecting the current sense resistor between ISENS and −VIN. The LCA slews the gate of the external pass FET to force the ISENS voltage to track the divided down IRAMP voltage. Consequently, the load current slew rate tracks the linear voltage ramp at the IRAMP pin, producing a linear di/dt of the load current. The IRAMP capacitor is charged to about 6.5 V; however, the LCA input is clamped at 40 mV. Therefore, the current sourced to the load during turn-on is limited to a value given by $IMAX \leq 40\ mV/R_{SENSE}$, where R_{SENSE} is the value of the sense resistor.

The resultant load current, regulated by the controller, charges the module's input bulk capacitance in a safe fashion. Under normal conditions, this capacitance eventually charges up to the dc input potential. At this point, the load demand drops off, and the voltage at ISENS decreases. The LCA now drives the GATE output to its supply rail.

The device detects this condition as the GATE voltage rises through 7 V or 8 V, latches this status and asserts the $\overline{PG}$ output. If the full sourced current limit is not yet available to the load, as evidenced by the IRAMP voltage being less than 5 V, then the $\overline{PG}$ assertion is delayed until that condition is also met.

The peak, steady-state GATE pin output, typically 14 V, ensures sufficient overdrive to fully enhance the external FET, while not exceeding the typical 20-V V_{GS} rating of common N-channel power FETs.

APPLICATION INFORMATION

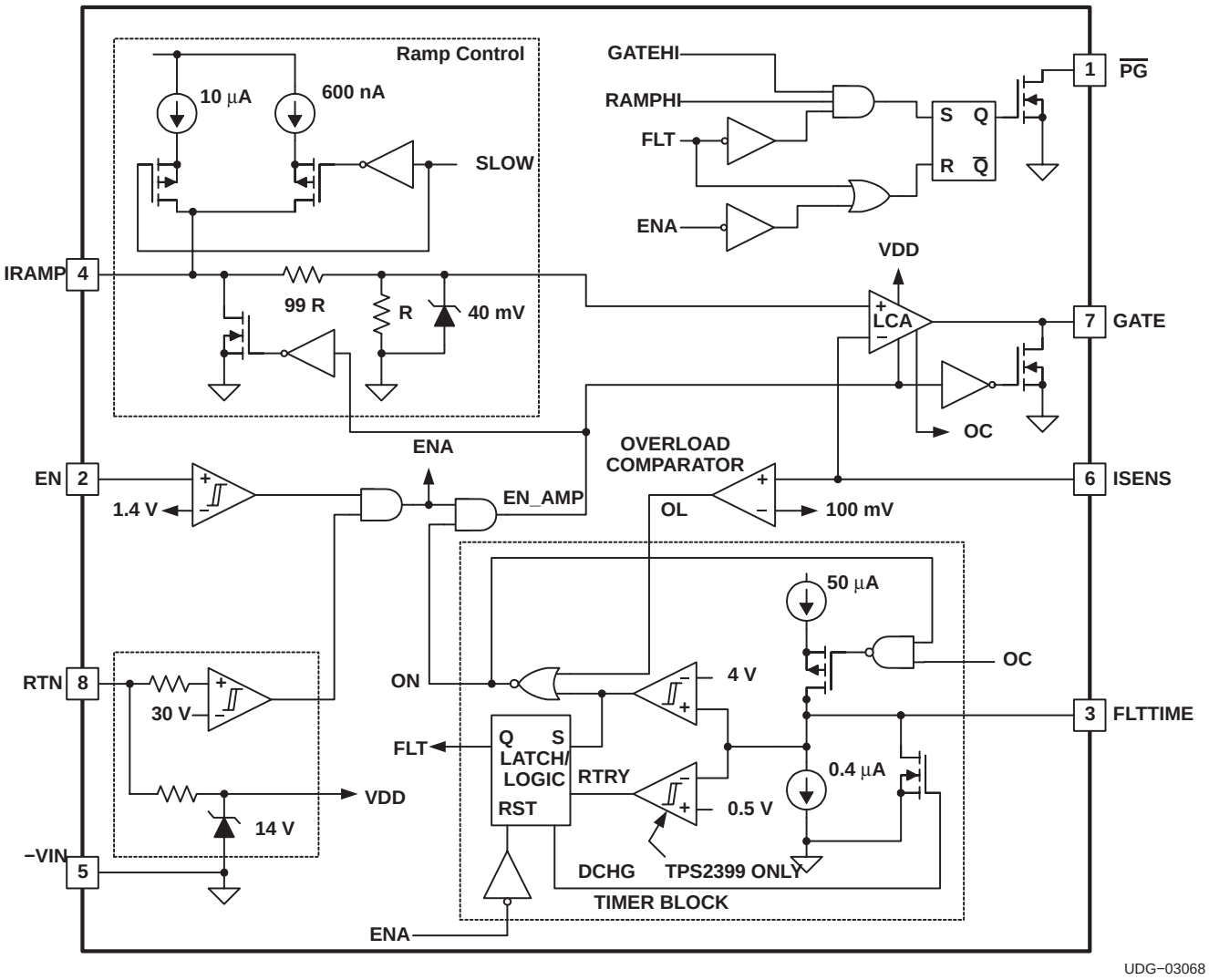


Figure 19. Block Diagram

Fault timing is accomplished by connecting a capacitor between the FLTTIME and −VIN pins, allowing user-programming of the timeout period. Whenever the hot swap controller is in current control mode as described above, the LCA asserts an overcurrent indication (OC in the Figure 17 diagram). Overcurrent fault timing is inhibited during the slow turn-on portion of the IRAMP waveform. However, once the device transitions to the normal rate current ramp ($V_{O(IRAMP)} \geq 0.5$ V), the external capacitor is charged by a 50-μA source, generating a voltage ramp at the FLTTIME pin. If the load voltage ramps successfully, the fault capacitor is discharged (DCHG signal), and load initialization can begin. However, if the timing capacitor voltage attains the 4-V fault threshold, the LCA is disabled, the pass FET is rapidly turned off, and the fault is latched. Fault capacitor charging ceases, and the capacitor is then discharged. In addition, latching of a fault condition causes rapid discharge of the IRAMP capacitor. In this manner, the soft-start function is then reset and ready for the next output enable, if and when conditions permit.

APPLICATION INFORMATION

Subsequent to a plug-in's start-up, and during the module's steady-state operation, load faults that force current limit operation also initiate fault timing cycles as described above. In this case, a fault timeout also clears the previously latched power good status.

The TPS2398 latches off in response to faults; once a fault timeout occurs, the DCHG signal turns on a large NMOS device to rapidly discharge the external capacitor, resetting the timer for any subsequent device reset. The TPS2398 can only be reset by cycling power to the device, or by cycling the EN input.

In response to a latched fault condition, the TPS2399 enters a fault retry mode, wherein it periodically retries the load to test for continued existence of the fault. In this mode, the FLTTIME capacitor is discharged slowly by a about a 0.4-µA constant-current sink. When the voltage at the FLTTIME pin decays below 0.5 V, the LCA and RAMP CONTROL circuits are re-enabled, and a normal turn-on current ramp ensues. Again, during the load charging, the OC signal causes charging of the FLTTIME capacitor until the next delay period elapses. The sequential charging and discharging of the FLTTIME capacitor results in a typical 1% retry duty cycle. If the fault subsides, the timing capacitor is rapidly discharged, duty-cycle operation stops, and the $\overline{PG}$ output is asserted.

Note that because of the timing inhibit during the initial slow ramp period, the duty cycle in practice is slightly greater than the nominal 1% value. However, sourced current during this period peaks at only about one-eighth the maximum limit. The duty cycle of the normal ramp and constant-current periods is approximately 1%.

The FAULT LOGIC within the TIMER BLOCK automatically manages capacitor charge and discharge actions, and the enabling of the GATE output (DCHG and ON signals).

supply transient response

The TPS2398 and TPS2399 also feature a fast-acting overload comparator which acts to clamp large transients from catastrophic faults occurring once the pass FET is fully enhanced, such as short circuits. This function provides a back-up protection to the LCA by providing a hard gate discharge action when the LCA is saturated. If sense voltage excursions above 100 mV are detected, this comparator rapidly pulls down the GATE output, bypassing the fault timer, and terminating the short−circuit condition. Once the spike has been brought down below the overload threshold, the GATE output is released, allowing the circuit to turn on again in either current-ramp or current-limit mode. A 4−µs deglitch filter is applied to the OL signal to help reduce the occurrence of nuisance trips.

In redundant-supply systems, the sudden switchover to a supply of higher voltage potential is one more source of large current spikes. Due to the low impedance of filter capacitance under such high-frequency transients, these spikes are generally indistinguishable from true short-circuit faults to a hot swap controller. However, the TPS2398and TPS2399 transient response addresses this issue by providing rapid circuit-breaker protection for load faults along with minimal interruption of power flow during supply switching events. The scope plots in Figure 20 illustrate how.

Figure 20 is a scope capture of the TPS2398/99 response in a diode-OR configuration to such an input transient event. (All waveforms are referenced to the −VIN pin.) In this example, the module is initially operating from a nominal −44-V supply (relative to the backplane supply return node). At the second major time division, another power supply, with an output of −48 V, is suddenly hot swapped into a secondary, or INB, input. This sudden voltage step is reflected in the −48V_RTN trace. On this board, the 4−V potential difference caused a greater than 6-A spike, as shown by the I_{INB} trace. The GATE pin is rapidly pulled low, which quickly terminates the overload spike. However, it is quickly released, and seen to drive back to the pass FET ON-threshold, in this case, about 4.5 V. The resultant current-limit operation of the circuit is evidenced by the 2-A load on the B supply. Once supply current is flowing again, the filter capacitance is charged up to the new input supply level, seen here on the V_{DRAIN} trace. Once the capacitance is fully charged, the load demand rolls off to the operating 1-A level. As an added benefit, this event is transparent to the $\overline{PG}$ signal, which remains asserted throughout the disturbance.

APPLICATION INFORMATION

INPUT TRANSIENT RESPONSE

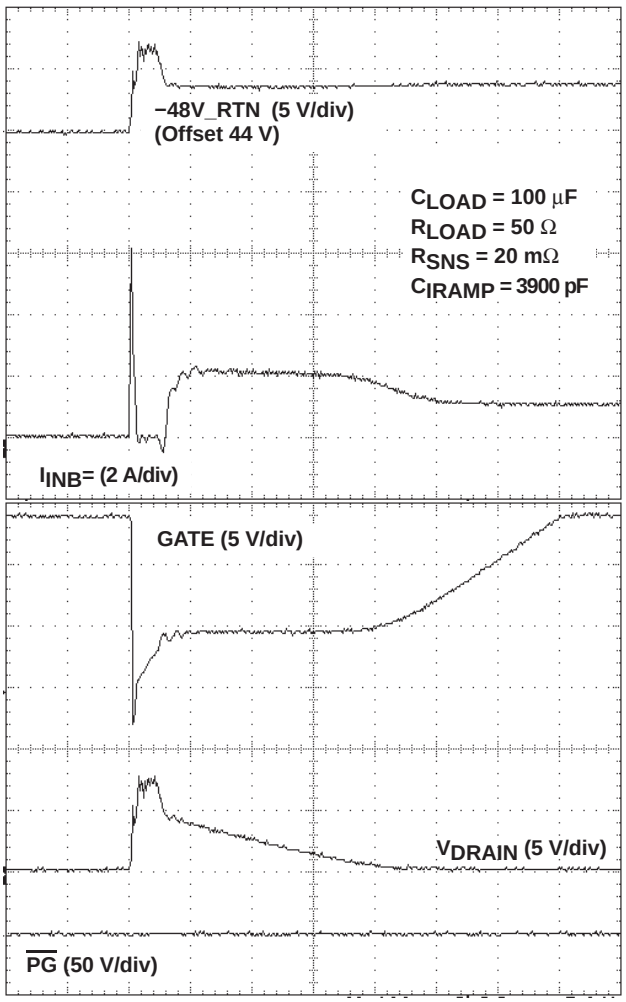


Figure 20

In order for downstream loads (bricks, etc.) to operate through the distribution bus transient, it is important to properly size the filtering capacitance to supply the needed energy during the OFF-time of the pass FET. In this example, once the RTN node stabilizes at about 3.5 V higher than the original potential, about 4.5 V develops across the FET, indicating approximately a 1-V droop across the brick input. Therefore, due to the fast response of the TPS2398/99 devices, the 100-μF capacitor achieves excellent hold-up of the brick input voltage. Actual requirements depend heavily on the individual application. Whether the device turns back on in either current-ramp or current-limit mode depends in part on the size of the ramp capacitor (C_{IRAMP}) and the input capacitance of the pass FET. But in any case, the circuit turns back on in a controlled-current manner after rapidly clamping the potentially damaging spike.

APPLICATION INFORMATION

setting the sense resistor value

Due to the current-limiting action of the internal LCA, the maximum allowable load current for an implementation is easily programmed by selecting the appropriate sense resistor value. The LCA acts to limit the sense voltage $V_{I(ISENS)}$ to its internal reference. Once the voltage at the IRAMP pin exceeds approximately 4 V, this limit is the clamp voltage, V_{REF_K}. Therefore, a maximum sense resistor value can be determined from equation (1).

$$R_{SENSE} \leq \frac{33\ mV}{IMAX} \tag{1}$$

where:

- R_{SENSE} is the resistor value, and
- IMAX is the desired current limit.

When setting the sense resistor value, it is important to consider two factors, the minimum current that may be imposed by the TPS2398 or TPS2399, and the maximum load under normal operation of the module. For the first factor, the specification minimum clamp value is used, as seen in equation (1). This method accounts for the tolerance in the sourced current limit below the typical level expected (40 mV/R_{SENSE}). (The clamp measurement includes LCA input offset voltage; therefore, this offset does not have to be factored into the current limit again.) Second, if the load current varies over a range of values under normal operating conditions, then the maximum load level must be allowed for by the value of R_{SENSE}. One example of this is when the load is a switching converter, or brick, which draws higher input current, for a given power output, when the distribution bus is at the low end of its operating range, with decreasing draw at higher supply voltages. To avoid current-limit operation under normal loading, some margin should be designed in between this maximum anticipated load and the minimum current limit level, or IMAX > $I_{LOAD(max)}$, for equation (1).

For example, using a 20-mΩ sense resistor for a nominal 1-A load application provides a minimum of 650 mA of overhead for load variance/margin. Typical bulk capacitor charging current during turn-on is 2 A (40 mV/20 mΩ).

setting the inrush slew rate

The TPS2398 and TPS2399 devices enable user-programming of the maximum current slew rate during load start-up events. A capacitor tied to the IRAMP pin (C2 in the typical application diagram) controls the di/dt rate. Once the sense resistor value has been established, a value for ramp capacitor C_{IRAMP}, in microfarads, can be determined from equation (2).

$$C_{IRAMP} = \frac{11}{100 \times R_{SENSE} \times \left(\frac{di}{dt}\right)_{MAX}} \tag{2}$$

where:

- R_{SENSE} is in ohms, and
- $(di/dt)_{MAX}$ is the desired maximum slew rate, in amperes/second.

For example, if the desired slew rate for the typical application shown is 1500 mA/ms, the calculated value for C_{IRAMP} is about 3700 pF. Selecting the next larger standard value of 3900 pF (as shown in the diagram) provides some margin for capacitor and sense resistor tolerances.

APPLICATION INFORMATION

As described earlier in this section, the TPS2398 and TPS2399 initiate ramp capacitor charging, and consequently, load current di/dt at a reduced rate. This reduced rate applies until the voltage on the IRAMP pin is about 0.5 V. The maximum di/dt rate, as set by equation (2), is effective once the device has switched to the 10-μA charging source.

setting the fault timing capacitor

The fault timeout period is established by the value of the capacitor connected to the FLTTIME pin, C_{FLT}. The timeout period permits riding out spurious current glitches and surges that may occur during operation of the system, and prevents indefinite sourcing into faulted loads swapped into a live system. However, to ensure smooth voltage ramping under all conditions of load capacitance and input supply potential, the minimum timeout should be set to accommodate these system variables. To do this, a rough estimate of the maximum voltage ramp time for a completely discharged plug-in card provides a good basis for setting the minimum timer delay.

Due to the three-phase nature of the load current at turn-on, the load voltage ramp potentially has three distinct phases (compare Figures 1 and 2). This profile depends on the relative values of load capacitance, input dc potential, maximum current limit and other factors. The first two phases are characterized by the two different slopes of the current ramp; the third phase, if required for bulk capacitance charging, is the constant-current charging at IMAX. Considering the two current ramp phases to be one period at an average di/dt simplifies calculation of the required timing capacitor.

For the TPS2398 and TPS2399, the typical duration of the soft-start ramp period, t_{SS}, is given by equation (3).

$$t_{SS} = 1183 \times C_{IRAMP} \tag{3}$$

where:

- t_{SS} is the soft-start period in ms, and
- C_{IRAMP} is given in μF

During this current ramp period, the load voltage magnitude which is attained is estimated by equation (4).

$$V_{LSS} = \frac{i_{AVG}}{2 \times C_{LOAD} \times C_{IRAMP} \times 100 \times R_{SENSE}} \times \left(t_{SS}\right)^2 \tag{4}$$

where:

- V_{LSS} is the load voltage reached during soft-start,
- i_{AVG} is 3.38 μA for the TPS2398 and TPS2399,
- C_{LOAD} is the amount of the load capacitance, and
- t_{SS} is the soft-start period, in seconds

The quantity i_{AVG} in equation (4) is a weighted average of the two charge currents applied to C_{IRAMP} during turn-on, considering the typical output values.

APPLICATION INFORMATION

If the result of equation (4) is larger than the maximum input supply value, then the load can be expected to charge completely during the inrush slewing portion of the insertion event. However, if this voltage is less than the maximum supply input, $V_{IN(max)}$, the HSPM transitions to the constant-current charging of the load. The remaining amount of time required at IMAX is determined from equation (5).

$$t_{CC} = \frac{C_{LOAD} \times \left(V_{IN\ (max)} - V_{LSS}\right)}{\left(\frac{V_{REF\_K\ (min)}}{R_{SENSE}}\right)} \quad (5)$$

where:

- t_{CC} is the constant-current voltage ramp time, in seconds, and
- $V_{REF\_K(min)}$ is the minimum clamp voltage, 33 mV.

With this information, the minimum recommended value timing capacitor C_{FLT} can be determined. The delay time needed will be either a time t_{SS2} or the sum of t_{SS2} and t_{CC}, according to the estimated time to charge the load. The quantity t_{SS2} is the duration of the normal rate current ramp period, and is given by equation (6).

$$t_{SS2} = 0.35 \times C_{RAMP} \quad (6)$$

where:

- C_{RAMP} is given in microfarads

Since fault timing is generated by the constant−current charging of C_{FLT}, the capacitor value is determined from either equation (7) or (8), as appropriate.

$$C_{FLT(min)} = \frac{55 \times t_{SS2}}{3.75} \quad (7)$$

$$C_{FLT(min)} = \frac{55 \times \left(t_{SS2} + t_{CC}\right)}{3.75} \quad (8)$$

where:

- $C_{FLT(min)}$ is the recommended capacitor value, in microfarads,
- t_{SS2} is the result of equation (6), in seconds, and
- t_{CC} is the result of equation (5), in seconds.

Continuing the typical application example, using a 100-µF input capacitor (C_{LOAD}), equations (3) and (4) estimate the load voltage ramping to approximately −46 V during the soft-start period. If the module should operate down to −72 V input supply, approximately another 1.58-ms of constant-current charging may be required. Therefore, equations (6) and (8) are used to determine $C_{FLT(min)}$, and the result of 0.043-µF suggests the 0.047-µF standard value.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS2398DGK	ACTIVE	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2398DGKG4	ACTIVE	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2398DGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2398DGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2399DGK	ACTIVE	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS2399DGKG4	ACTIVE	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS2399DGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS2399DGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

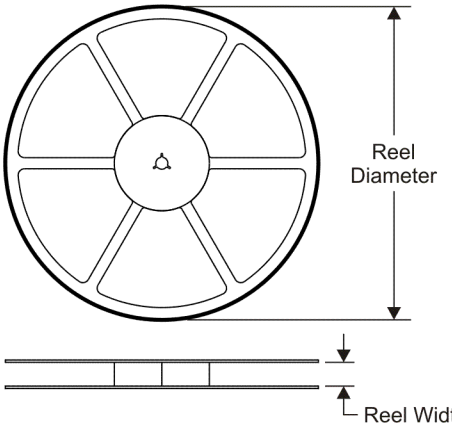
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

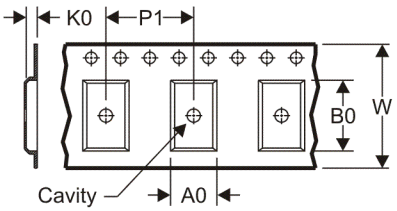
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

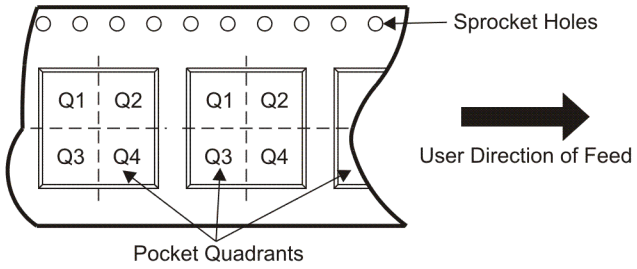


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

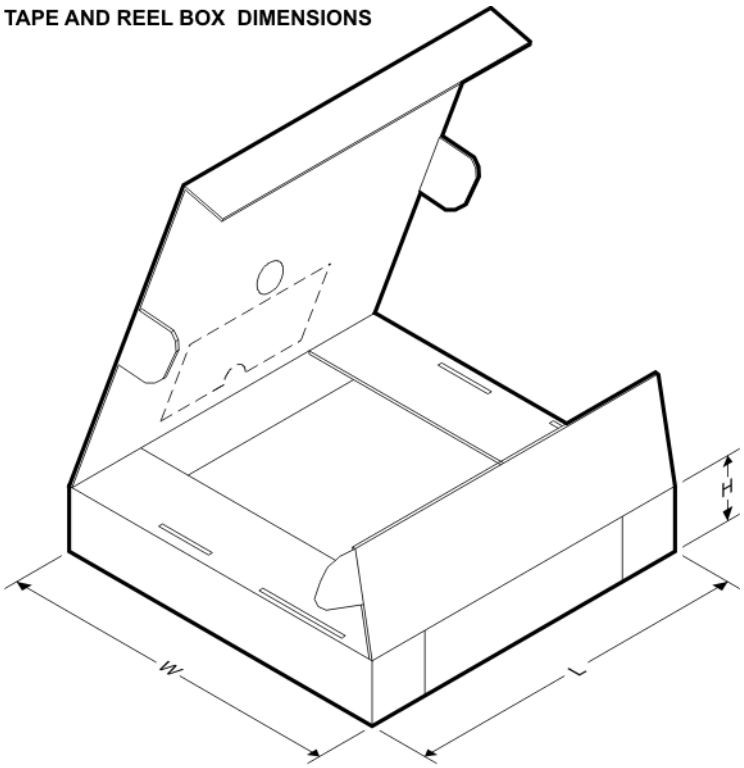
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2398DGKR	MSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2399DGKR	MSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

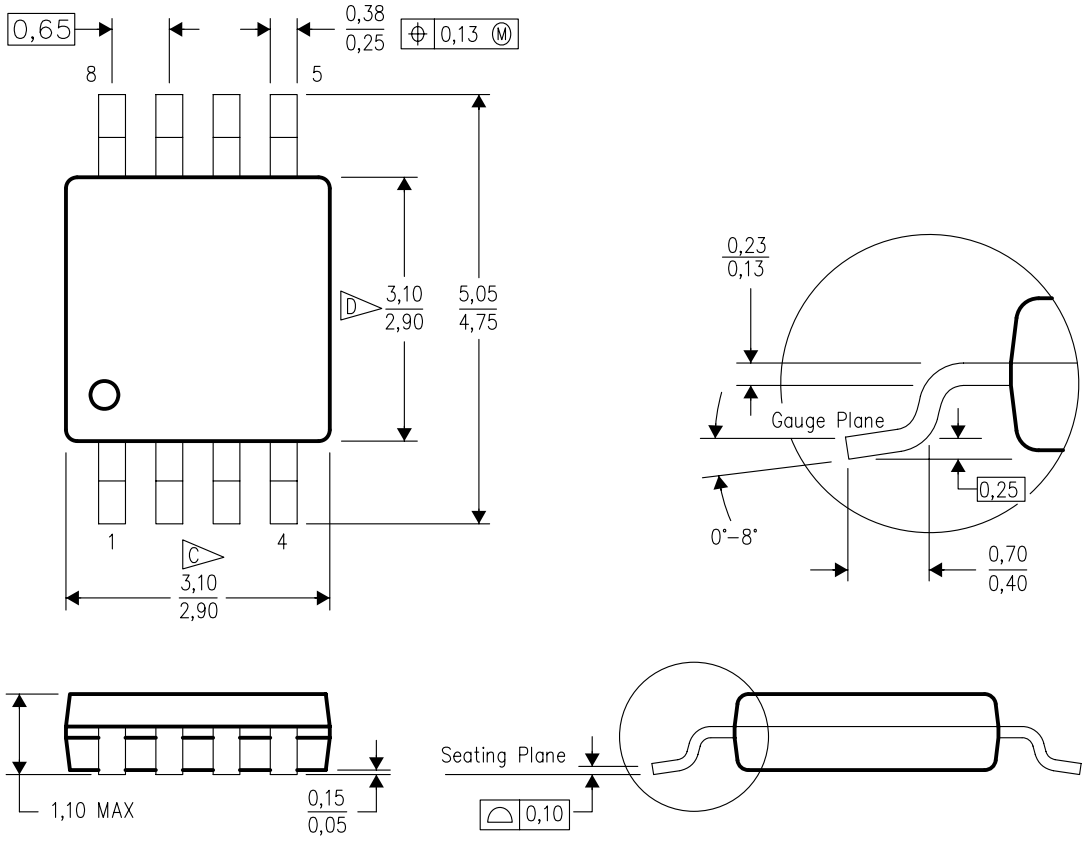
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2398DGKR	MSOP	DGK	8	2500	346.0	346.0	29.0
TPS2399DGKR	MSOP	DGK	8	2500	346.0	346.0	29.0

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2398DGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	2398	Samples
TPS2399DGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	2399	Samples
TPS2399DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 85	2399	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
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(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

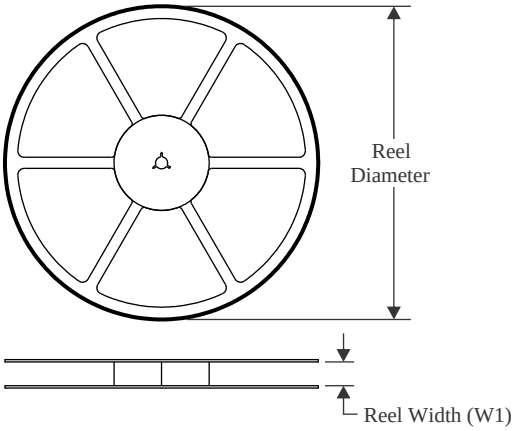
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

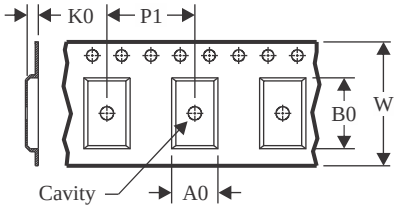
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

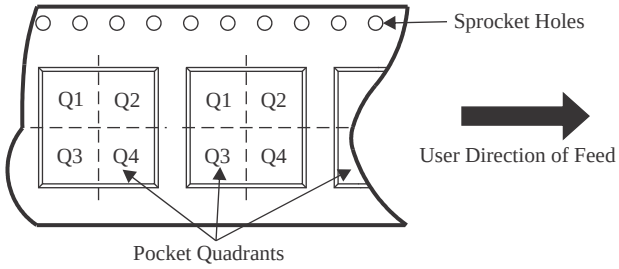


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

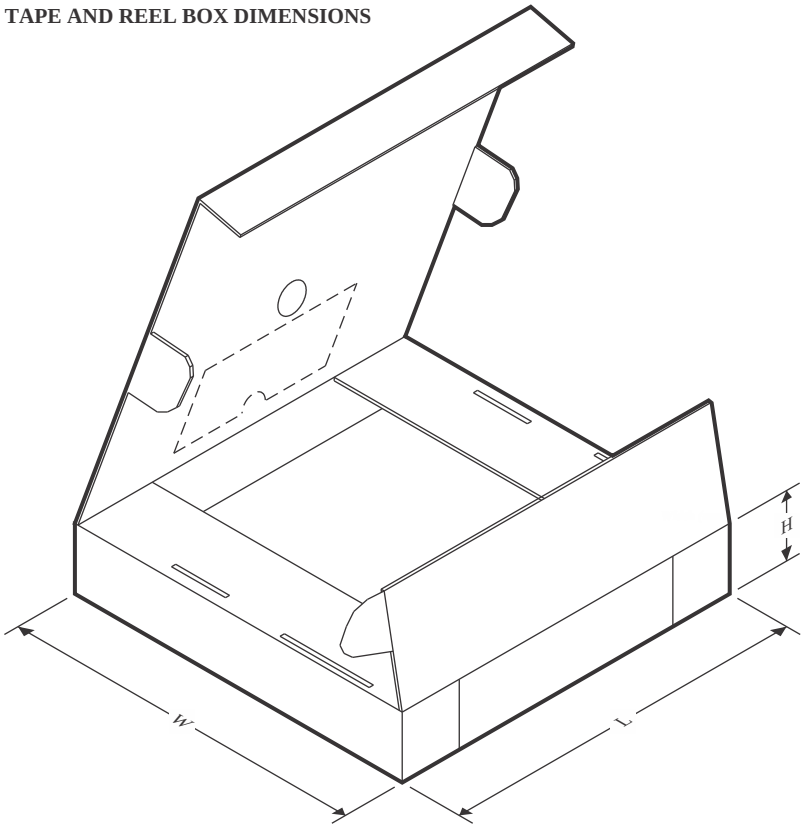
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2399DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

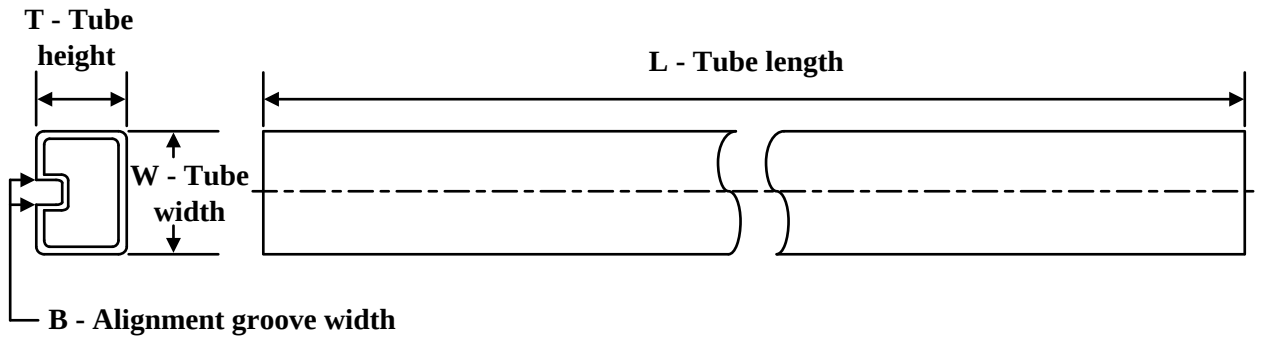
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2399DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0

TUBE



*All dimensions are nominal

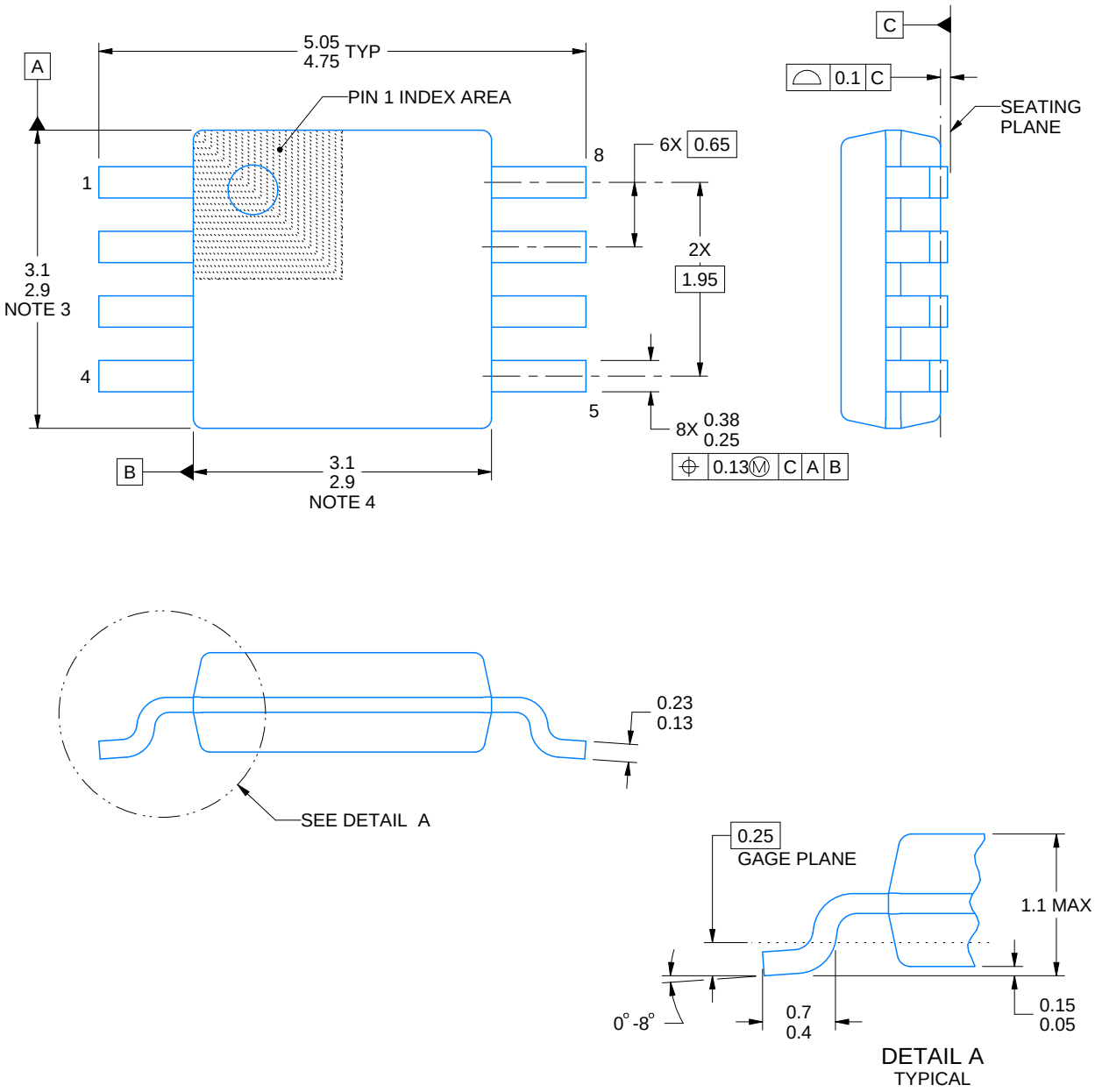
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS2398DGK	DGK	VSSOP	8	80	330	6.55	500	2.88
TPS2399DGK	DGK	VSSOP	8	80	330	6.55	500	2.88

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



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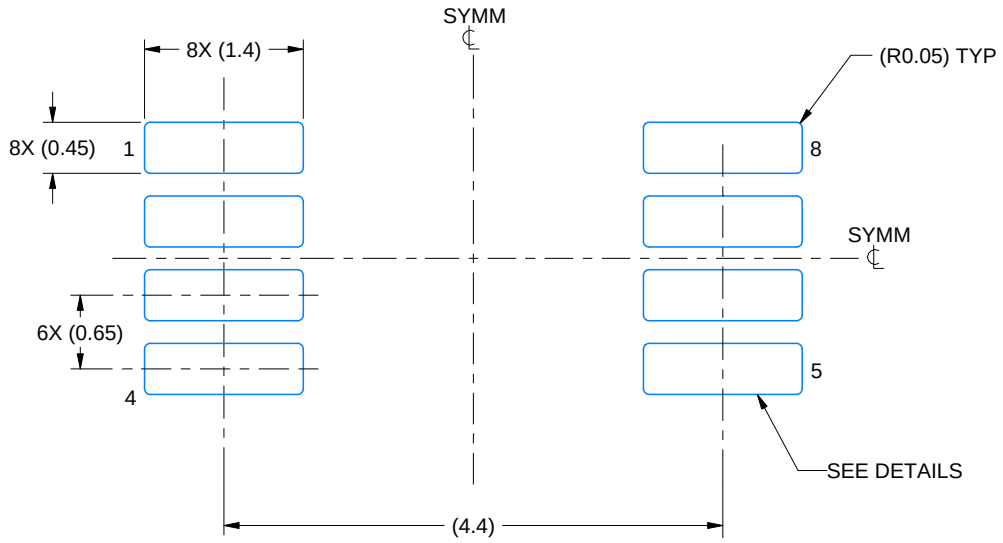
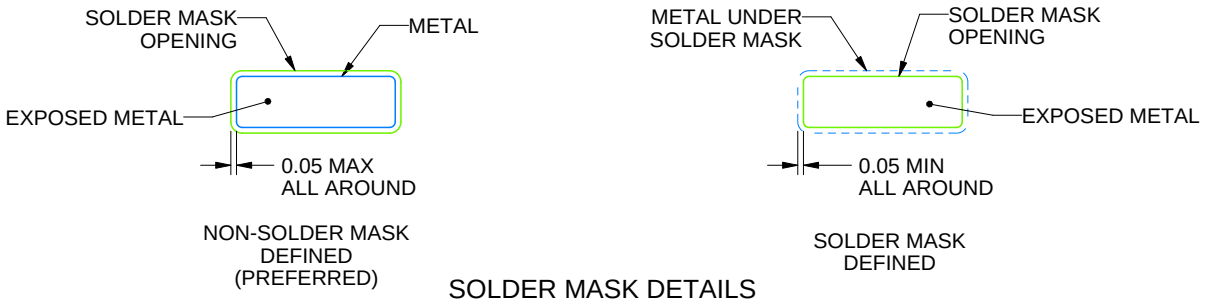
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

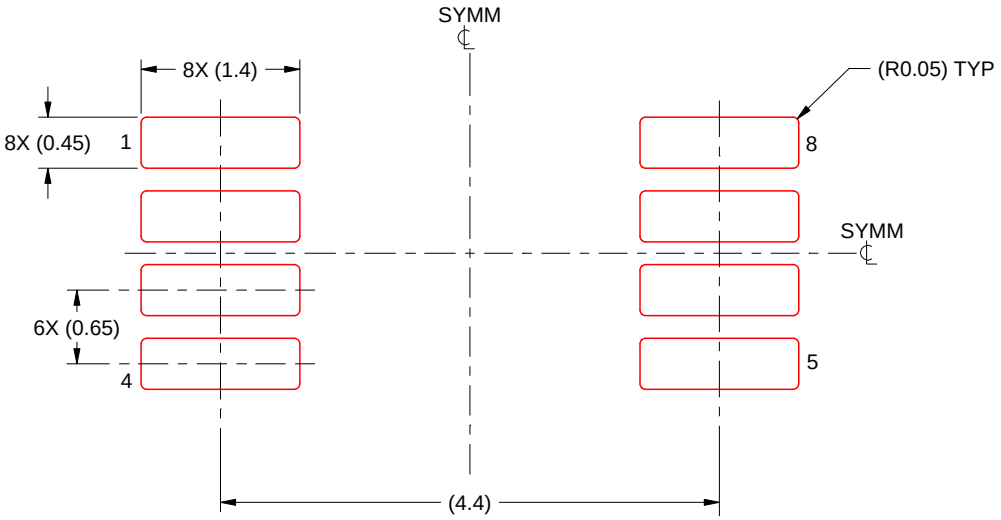


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265