TPS53316 High-Efficiency, 5-A Step-Down Regulator With Integrated Switcher

1 Features

- 96% Maximum Efficiency
- Continuous 5-A Output Current Capability
- Support all MLCC Output Capacitor
- SmoothPWM™ Auto-Skip Eco-Mode™ for Light-Load Efficiency
- Voltage Mode Control
- Single Rail Input
- Selectable Frequency
- Selectable OCP Threshold
- Selectable Soft-Start Time
- 2.9-V to 6-V Input Voltage Range
- Adjustable Output Voltage Ranging from 0.6 V up to 0.8 × V_{IN}
- Soft-Stop Output Discharge During Disable
- Overcurrent, Overvoltage, and Overtemperature Protection
- Open-Drain Power Good Indication
- Internal Bootstrap Switch
- Supports Prebias Start-Up Functionality
- Small 3 mm × 3 mm, 16-Pin, QFN Package
- Low $R_{DS(on)}$, 22-mΩ With 3.3-V Input and 18-mΩ With 5-V Input

2 Applications

- Low-Voltage Applications for 5-V Step-Down Rails
- Low-Voltage Applications for 3.3-V Step-Down Rails

3 Description

The TPS53316 device provides a fully integrated 3.3-V or 5-V input, synchronous buck converter with 16 total components, in 200 mm^2 of PCB area. Due to low $R_{DS(on)}$ and TI proprietary SmoothPWM skip mode of operation, it enables 96% peak efficiency, and over 90% efficiency at load as light as 100 mA. It requires only two 22-µF ceramic output capacitors for a power-dense, 5-A solution.

TPS53316 features 750-kHz, 1.1-MHz, and 2-MHz switching frequency selections, prebias start-up, selectable internal softstart, output soft discharge, internal VBST switch, power good, EN/Input UVLO, overcurrent, overvoltage, undervoltage, and overtemperature protections and all ceramic output capacitor support. It supports input voltages from 2.9 V to 6 V, and no extra bias voltage is needed. The output voltage is adjustable from 0.6 V up to 0.8 × V_{IN}.

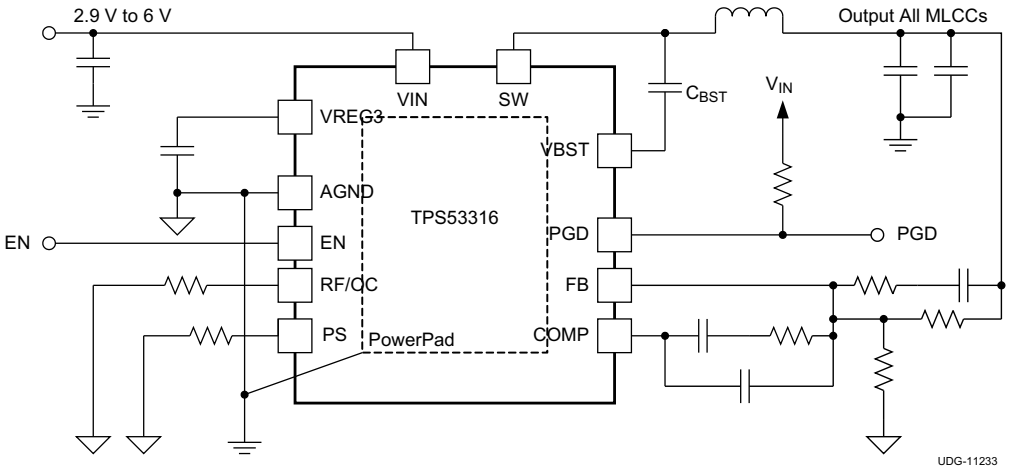
TPS53316 is available in the 3 mm × 3 mm, 16-pin QFN package (Green RoHs compliant and Pb free) and is specified from –40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS53316	QFN (16)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2011) to Revision A **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *Ordering Information* table; see POA at the end of the data sheet ... 1
- Deleted Lead temperature, 1.6 mm (1/16 inch) from case for 10 seconds: 300°C maximum ... 4
- Changed R8 value in the Typical 3.3-V Input Application Circuit Diagram From: 5.76 kΩ To: 57.6 kW ... 18

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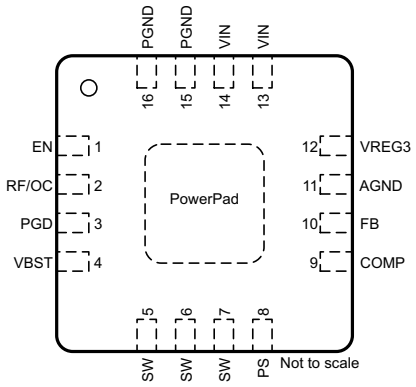
5 Pin Configuration and Functions

RGT Package
16-Pin QFN
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	EN	I	Enable pin. Internally pulled-up to the VIN pin through a 2-MΩ resistor. The EN voltage must be less than (V_{IN} + 0.5 V).
2	RF/OC	I	Switching frequency and OC level configuration pin: Connecting to ground: 1.1 MHz, 6.5-A OCP Pulled high or floating (internal pulled high): 1.1 MHz, 4.5-A OCP Connect with 24.3 kΩ to GND: 750 kHz, 4.5-A OCP Connect with 57.6 kΩ to GND: 750 kHz, 6.5-A OCP Connect with 105 kΩ to GND: 2 MHz, 4.5-A OCP Connect with 174 kΩ to GND: 2 MHz, 6. 5-A OCP
3	PGD	O	Power good output flag. Open-drain output. Pull up to an external rail through a resistor.
4	VBST	P	Supply input for high-side MOSFET (bootstrap terminal). Connect capacitor from this pin to SW terminal.
5	SW	B	Output inductor connection to integrated power devices
6	SW	B	Output inductor connection to integrated power devices
7	SW	B	Output inductor connection to integrated power devices
8	PS	I	Mode configuration pin (with10-µA current): Connecting to ground: Forced CCM with 4x softstart time Pulled high or floating (internal pulled high): Forced CCM master Connect with 24.3 kΩ to GND: HEF mode with 4x softstart time Connect with 57.6 kΩ to GND: HEFF mode Connect with 105 kΩ to GND: DE mode Connect with 174 kΩ to GND: DE mode with 4x softstart time
9	COMP	O	Error amplifier compensation terminal. Type III compensation method is generally recommended for stability.
10	FB	I	Voltage feedback pin. Use for OVP, UVP, and PGD determination.
11	AGND	G	Device analog ground terminal
12	VREG3	O	3.3-V LDO output, serves as supply voltage for internal analog circuitry. The EN pin controls the turnon function of the LDO.
13	VIN	P	Gate driver supply and power conversion input voltage. The input range is from 2.9 V to 6 V.
14	VIN	P	Gate driver supply and power conversion input voltage. The input range is from 2.9 V to 6 V.
15	PGND	P	Device power ground terminal
16	PGND	P	Device power ground terminal
—	PowerPad	—	Thermal pad of the device. Use 4 or 5 vias to connect to GND plane for heat dissipation.

(1) B = Bidirectional, G = Ground, I = Input, O = Output, P = Supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Input voltage	VIN		–0.3	7	V
	VBST		–0.3	17	
	VBST (with respect to LL)		–0.3	7	
	EN		–0.3	7	
	FB, PS, RF/OC		–0.3	3.7	
Output voltage	SW	DC	–1	7	V
		Pulse < 20 ns, E = 5 µJ	≥–5	<10	
	PGD		–0.3	7	
	COMP, VREG3		–0.3	3.7	
	PGND		–0.3	0.3	
Junction temperature, T_J			–40	150	°C
Operating open-air temperature, T_A			–40	85	°C
Storage temperature, T_{stg}			–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
Input voltage	VIN (main supply)	2.9	6	V
	VBST	–0.1	13.5	
	VBST (with respect to SW)	–0.1	6	
	EN,	–0.1	6	
	FB, PS, RF/OC	–0.1	3.5	
Output voltage	SW	–1	6.5	V
	PGD	–0.1	6	
	COMP, VREG3	–0.1	3.5	
	PGND	–0.1	0.1	
T_J Junction temperature		–40	125	°C

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6.4 Thermal Information

THERMAL METRIC[1]		TPS53316 RGT (QFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	18.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range, VIN = 3.3 V, PGND = GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY: VOLTAGE, CURRENTS, AND UVLO						
V_{VIN}	VIN supply voltage	Nominal input voltage range	2.9		6	V
$I_{VIN(sdn)}$	VIN shutdown current	EN = LO			15	µA
I_{VIN}	VIN supply current	EN = HI, V_{FB} = 0.63 V, No load		2	3.5	mA
V_{UVLO}	VIN UVLO threshold	Ramp up, EN = HI		2.8		V
$V_{UVLO(hys)}$	VIN UVLO hysteresis	VIN UVLO hysteresis		120		mV
V_{REG3}	LDO output	V_{VIN} = 5 V, 0 ≤ I_{DD} ≤ 5 mA	3.135	3.3	3.465	V
VOLTAGE FEEDBACK LOOP: VREF AND ERROR AMPLIFIER						
V_{VREF}	VREF	Internal precision reference voltage		0.6		V
TOL_{VREF}	VREF tolerance	0°C ≤ T_A ≤ 85°C	–1%		1%	
		–40°C ≤ T_A ≤ 85°C	–1.25%		1.25%	
UGBW[1]	Unity gain bandwidth		14			MHz
A_{OL}[1]	Open-loop gain		80			dB
I_{FBINT}	FB input leakage current	Sourced from FB pin			30	nA
$I_{EA(max)}$[1]	Output sinking and sourcing current	C_{COMP} = 20 pF		5		mA
SR[1]	Slew rate			5		V/µs
OCP: OVERCURRENT AND ZERO CROSSING						
I_{OCPL3A}[2]	Overcurrent limit on high-side FET	4.5-A setting, when I_{OUT} exceeds this threshold for 4 consecutive cycles, V_{VIN} = 3.3 V, V_{OUT} = 1.5 V with 1-µH inductor, f_{SW} = 1.1 MHz, T_A = 25°C	4.05	4.5	4.95	A
I_{OCPH3A}[2]	One-time overcurrent latch off on the low-side FET	4.5-A setting, immediate shuts down when sensed current reach this value V_{VIN} = 3.3 V, V_{OUT} = 0.6 V with 1-µH inductor, f_{SW} = 1.1 MHz, T_A = 25°C	4.49	5.1	5.61	A
I_{OCPL5A}[2]	Overcurrent limit on high-side FET	6.5-A setting, when I_{OUT} exceeds this threshold for 4 consecutive cycles, V_{VIN} = 3.3 V, V_{OUT} = 1.5 V with 1-µH inductor, f_{SW} = 1.1 MHz, T_A = 25°C	6.1	6.8	7.5	A
I_{OCPH5A}[2]	One time overcurrent latch off on the low-side FET	6.5-A setting, immediate shut down when sensed current reaches this value V_{VIN} = 3.3 V, V_{OUT} = 0.6 V with 1-µH inductor, f_{SW} = 1.1 MHz, T_A = 25°C	6.75	7.5	8.3	A
t_{hiccup}	Hiccup time interval	f_{SW} = 1.1 MHz		14.5		ms
V_{ZXOFF}[1]	Zero crossing comparator internal offset	PGND – SW, SKIP mode	–4.5	–3	–1.5	mV

(1) Ensured by design. Not production tested.
(2) See Figure 5 and Figure 6 on OCP level for other operating conditions.

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Electrical Characteristics (continued)

over operating free-air temperature range, VIN = 3.3 V, PGND = GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PROTECTION: OVP, UVP, PGD, AND INTERNAL THERMAL SHUTDOWN						
V_{OVP}	Overvoltage protection threshold voltage	Measured at the FB w/r/t VREF	114%	117%	120%	
V_{UVP}	Undervoltage protection Threshold voltage	Measured at the FB w/r/t VREF	80%	83%	86%	
V_{PGDL}	PGD low threshold	Measured at the FB w/r/t VREF	80%	83%	86%	
V_{PGDU}	PGD upper threshold	Measured at the FB w/r/t VREF	114%	117%	120%	
$V_{INMINPG}$	Minimum input voltage for valid PGD at start-up	Measured at VIN with 1-mA sink current on PGD pin at start-up		1		V
THSD(1)	Thermal shutdown		130	140	150	°C
$THSD_{HYS}$(1)	Thermal shutdown hysteresis	Controller start again after temperature has dropped		40		°C
LOGIC PINS: I/O VOLTAGE AND CURRENT						
V_{PGPD}	PGD pull-down voltage	Pulldown voltage with 4-mA sink current		0.1	0.3	V
I_{PGLK}	PGD leakage current	Hi-Z leakage current, Apply 3.3 V in off state	–2	0	2	µA
R_{ENPU}	Enable pullup resistor			2.25		MΩ
V_{ENH}	EN logic high	V_{VIN} = 3.3 V	0.82	0.97	1.1	V
		V_{VIN} = 5 V	0.95	1.1	1.25	V
V_{ENHYS}	EN hysteresis	V_{VIN} = 3.3 V		0.16	0.24	V
		V_{VIN} = 5 V		0.2	0.275	V
PS_{THS}	PS mode threshold voltage	Level 1 to level 2(3)		0.12		V
		Level 2 to level 3		0.4		
		Level 3 to level 4		0.8		
		Level 4 to level 5		1.4		
		Level 5 to level 6		2.2		
I_{PS}	PS source	10-µA pull-up current when enabled	8	10	12	µA
RF/OC_{THS}	RF/OC pin threshold voltage	Level 1 to level 2(4)		0.12		V
		Level 2 to level 3		0.4		
		Level 3 to level 4		0.8		
		Level 4 to level 5		1.4		
		Level 5 to level 6		2.2		
$I_{RF/OC}$	RF/OC source current	10-µA pullup current when enabled	8	10	12	µA
BOOT STRAP: VOLTAGE AND LEAKAGE CURRENT						
I_{VBSTLK}	VBST leakage current	V_{VIN} = 3.3 V, V_{VBST} = 6.6 V, T_A = 25°C			1	µA
TIMERS: SS, FREQUENCY, RAMP, ON-TIME AND I/O TIMING						
t_{SS_1}	Delay after EN Asserting	EN = 'HI'		0.2		ms
t_{SS_2}	Soft-start ramp_up time	0 V ≤ V_{SS} ≤ 0.6 V		0.4		ms
		0 V ≤ V_{SS} ≤ 0.6 V, 4 x SS time (option2)		1.6		
$t_{PGDENDLY}$	PGD start-up delay time	V_{SS} = 0.6 V to PGD (SSOK) going high		0.3		ms
		V_{SS} = 0.6 V to PGD (SSOK), option 2		1.2		
t_{OVPDLY}	OVP delay time	Time from FB out of +20% of VREF to OVP fault	1	1.7	2.5	µs
t_{UVPDLY}	UVP delay time	Time from FB out of –20% of VREF to UVP fault		10		µs
f_{SW}	Switching frequency	All modes, f_{SET} = 0.75 MHz	0.653	0.725	0.798	MHz
		All modes, f_{SET} = 1.1 MHz	0.99	1.1	1.21	
		FCCM and DE mode, f_{SET} = 2 MHz	1.71	1.9	2.09	
		HEF mode, f_{SET} = 2 MHz	1.566	1.8	2.034	MHz

(3) See PS pin description for levels.
(4) See RF/OC pin description for levels.

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Electrical Characteristics (continued)

over operating free-air temperature range, VIN = 3.3 V, PGND = GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Ramp amplitude (1)	2.9 V ≤ V_{VIN} ≤ 6 V		V_{VIN}/4		V
$t_{MIN(off)}$	Minimum OFF time, FCCM and DE	All frequencies		90	130	ns
	Minimum OFF time, HEF	f_{SW} = 1.1 MHz		160	240	ns
D_{MAX}	Maximum duty cycle, FCCM and DE	f_{SW} = 1.1 MHz	84%	89%		
D_{MAX}	Maximum duty cycle, HEF	All frequencies	75%	81%		
R_{SFTSTP}	Soft-discharge transistor resistance	EN = LO, V_{VIN} = 3.3 V, V_{OUT} = 0.5 V		60		Ω

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6.6 Typical Characteristics

Inductor used: PCMC065T-1R0, 1 µH, 5.6 mΩ

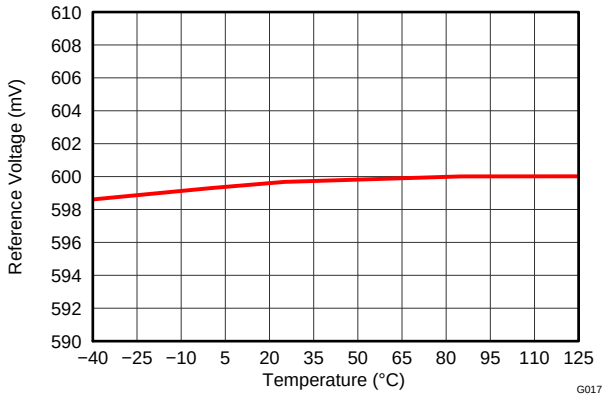

Figure 1. Reference Voltage vs Temperature

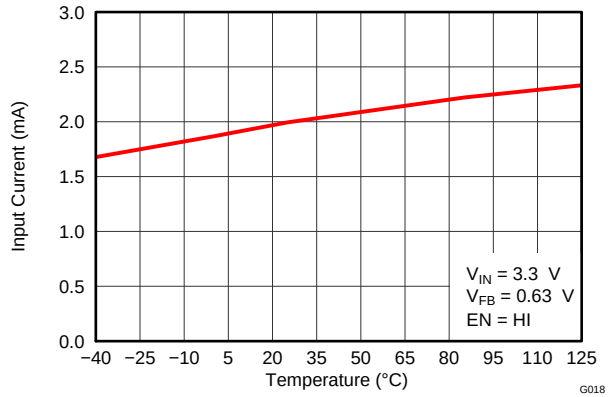

Figure 2. Input Current vs Temperature

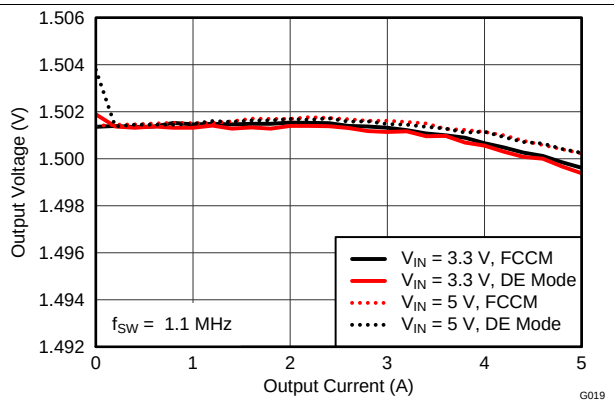

Figure 3. Output Voltage vs Output Current

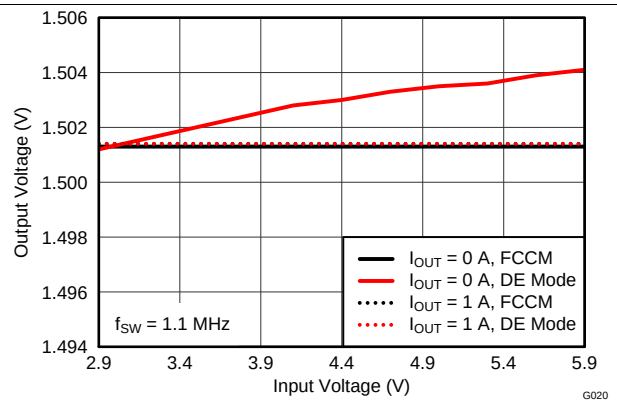

Figure 4. Output Voltage vs Input Voltage

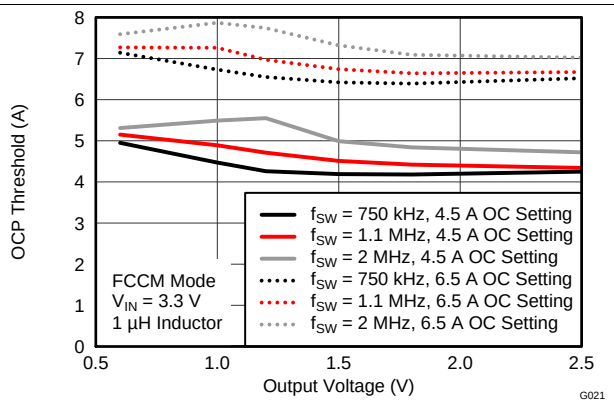

Figure 5. OCP Threshold vs Output Voltage

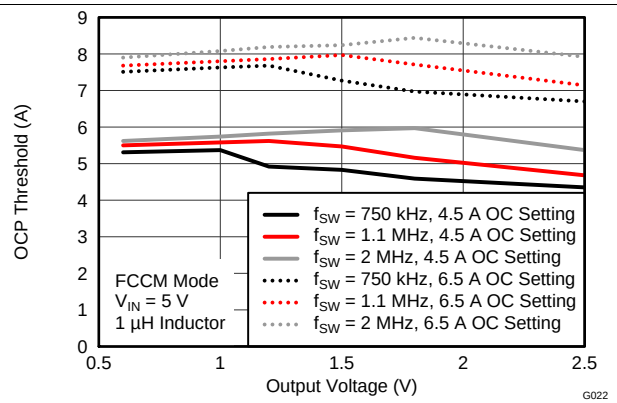

Figure 6. OCP Threshold vs Output Voltage

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Typical Characteristics (continued)

Inductor used: PCMC065T-1R0, 1 µH, 5.6 mΩ

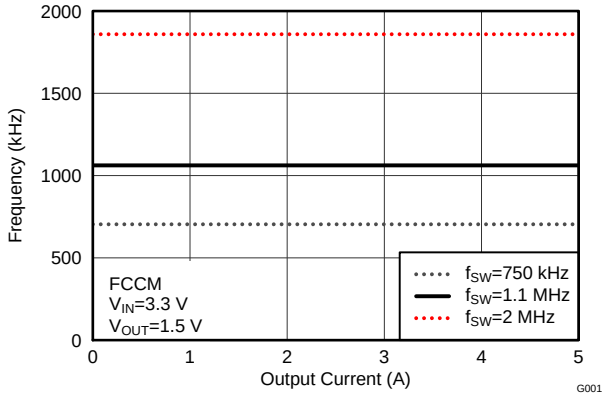

Figure 7. Frequency vs Output Current, FCCM

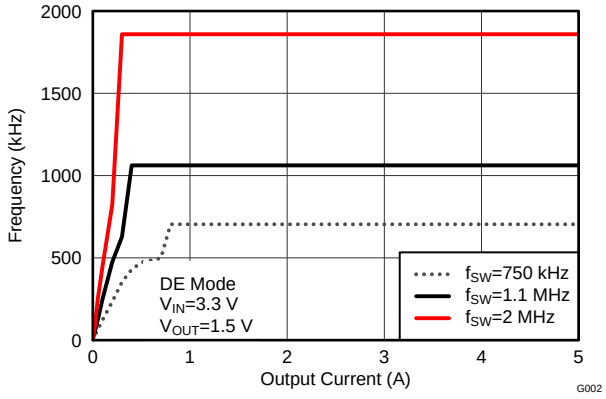

Figure 8. Frequency vs Output Current, DE Mode

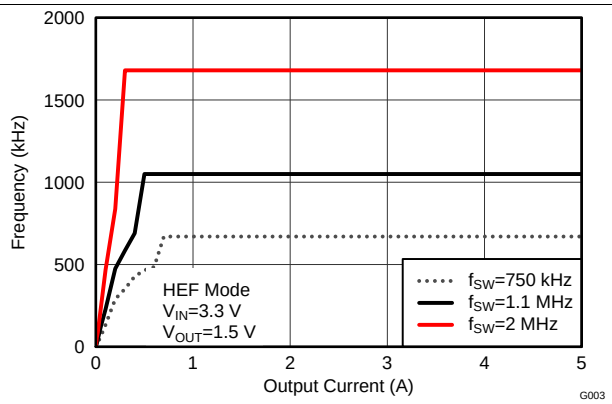

Figure 9. Frequency vs Output Current, HEF Mode

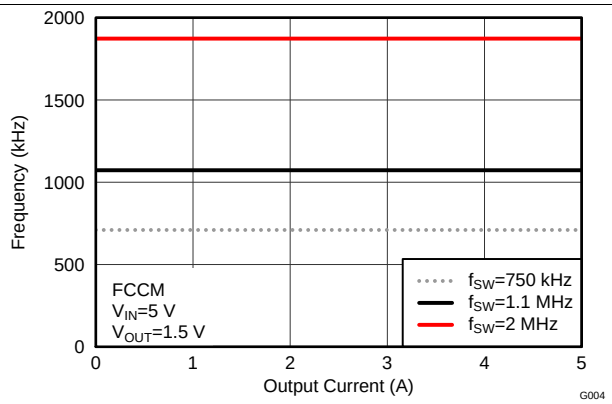

Figure 10. Frequency vs Output Current, FCCM

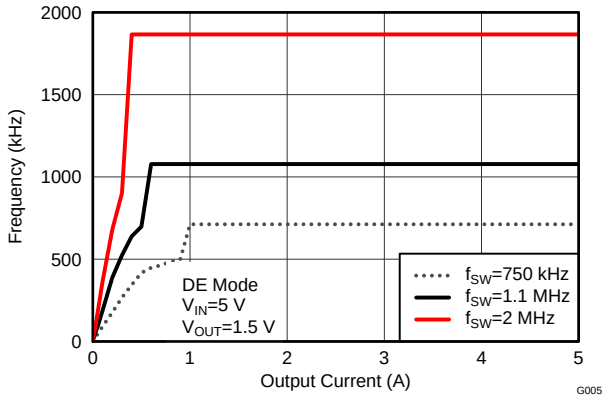

Figure 11. Frequency vs Output Current, DE Mode

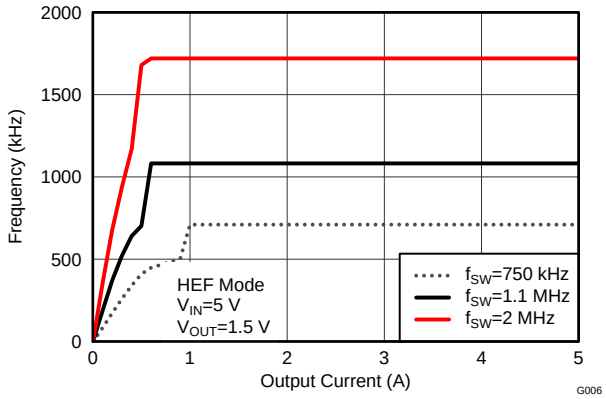

Figure 12. Frequency vs Output Current, HEF Mode

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Typical Characteristics (continued)

Inductor used: PCMC065T-1R0, 1 µH, 5.6 mΩ

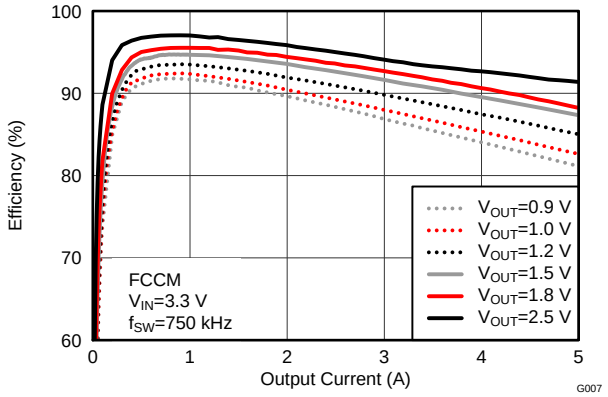

Figure 13. Efficiency vs Output Current, FCCM

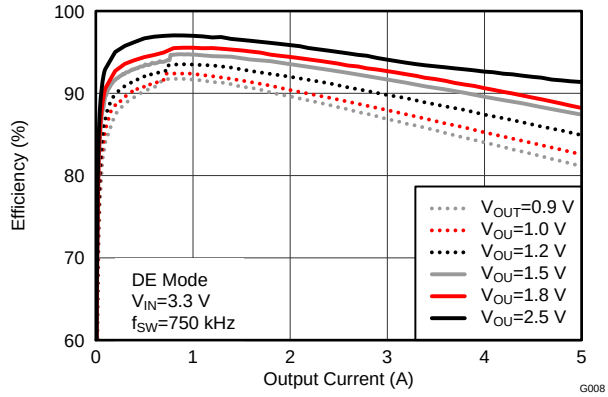

Figure 14. Efficiency vs Output Current, DE Mode

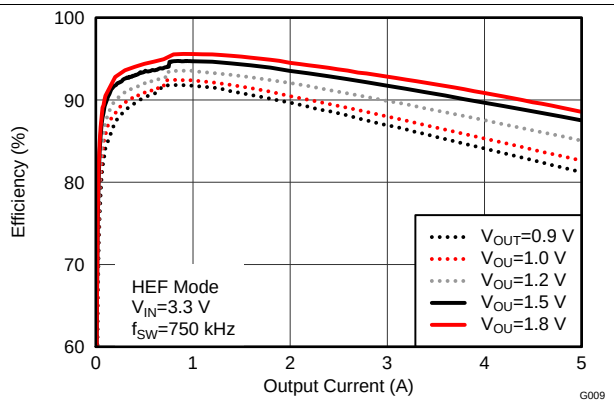

Figure 15. Efficiency vs Output Current, HEF Mode

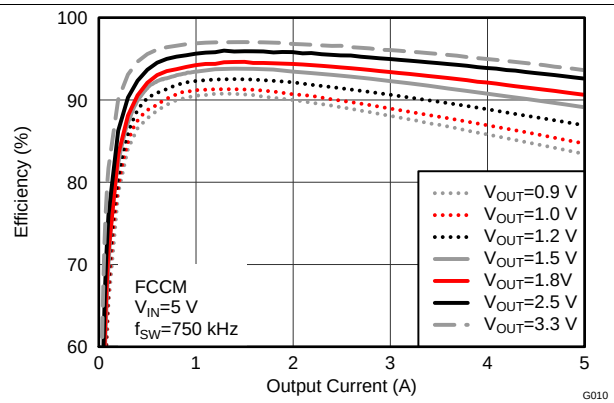

Figure 16. Efficiency vs Output Current, FCCM

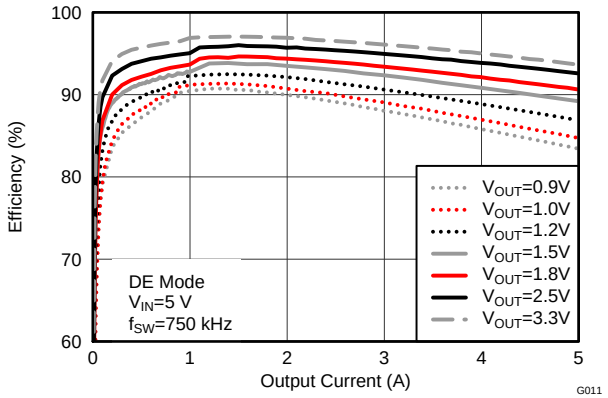

Figure 17. Efficiency vs Output Current, DE Mode

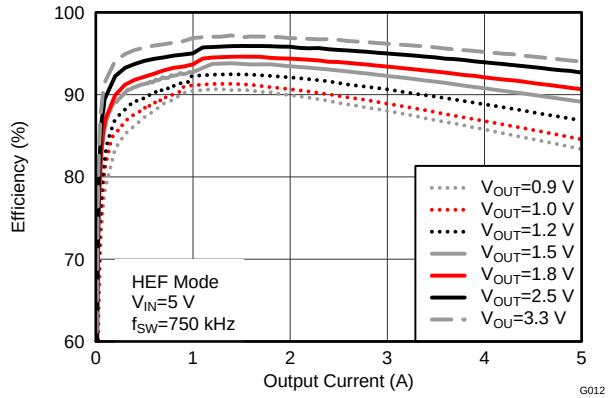

Figure 18. Efficiency vs Output Current, HEF Mode

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Typical Characteristics (continued)

Inductor used: PCMC065T-1R0, 1 µH, 5.6 mΩ

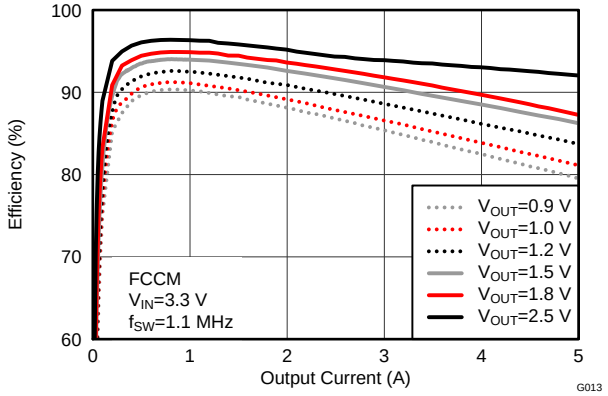

Figure 19. Efficiency vs Output Current, FCCM

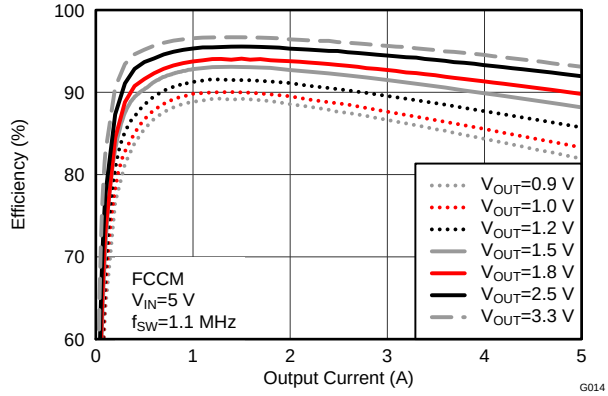

Figure 20. Efficiency vs Output Current, FCCM

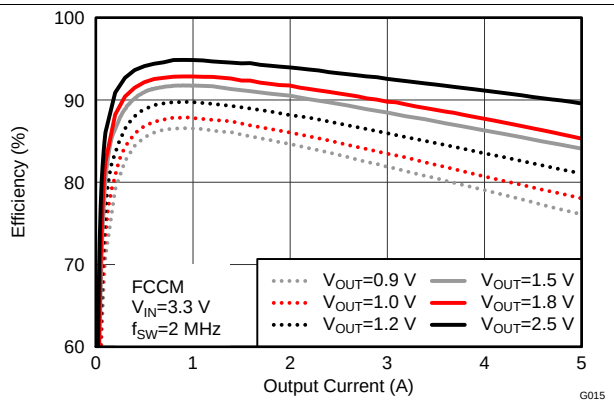

Figure 21. Efficiency vs Output Current, FCCM

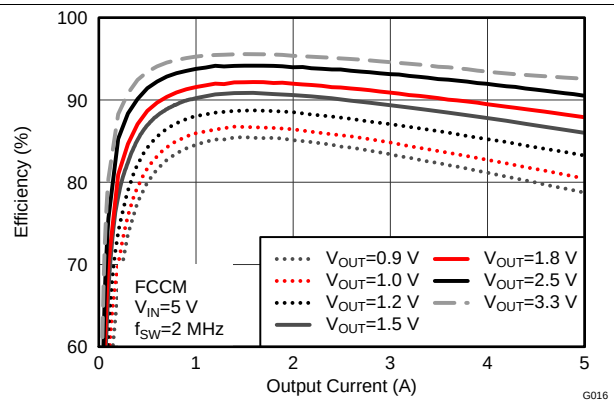

Figure 22. Efficiency vs Output Current, FCCM

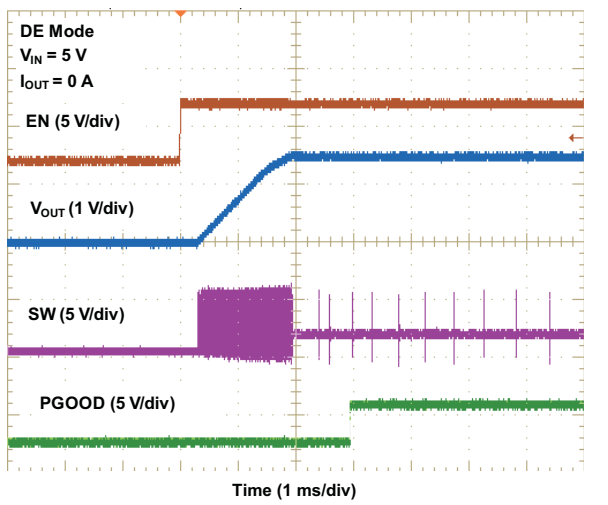

Figure 23. Normal Start-up

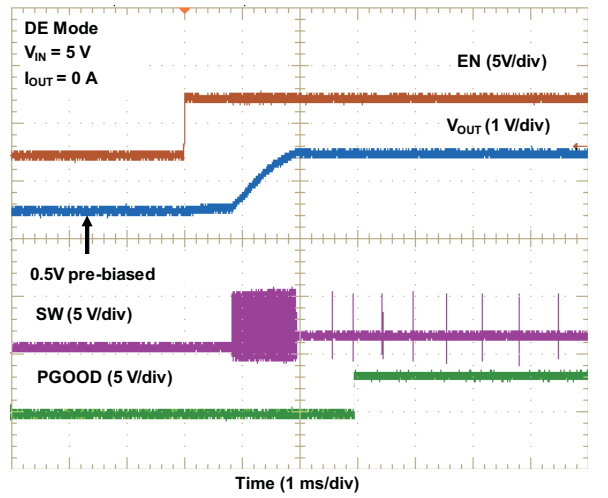

Figure 24. Prebiased Start-up

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Typical Characteristics (continued)

Inductor used: PCMC065T-1R0, 1 µH, 5.6 mΩ

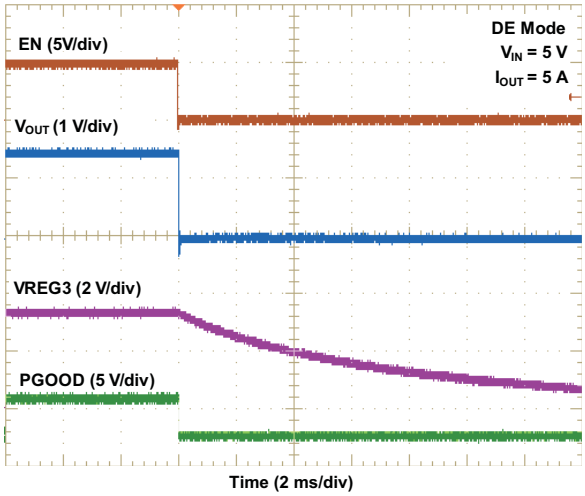

Figure 25. Turnoff Enable

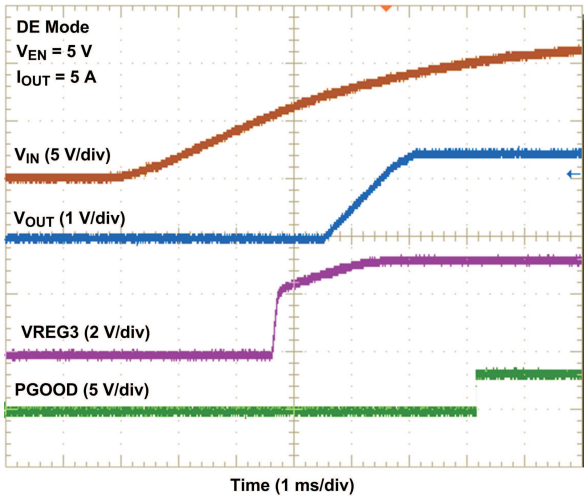

Figure 26. UVLO Start-Up Waveform

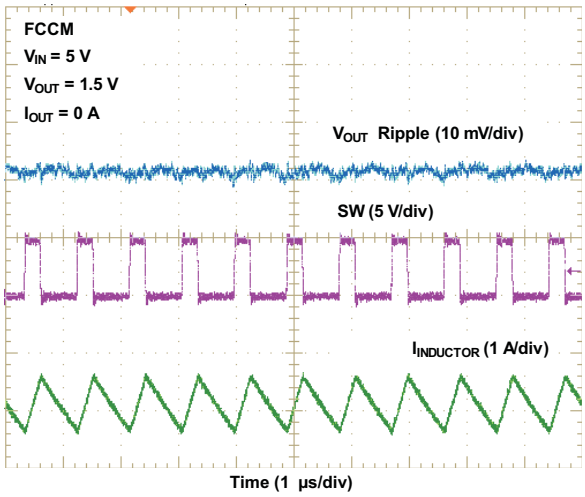

Figure 27. Output Voltage Ripple – FCCM

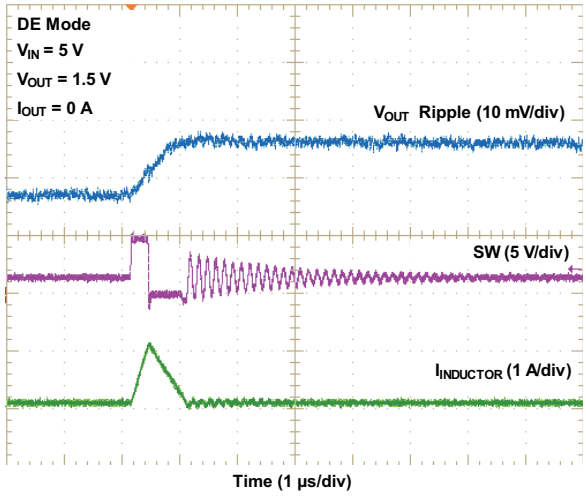

Figure 28. Output Voltage Ripple – DE Mode

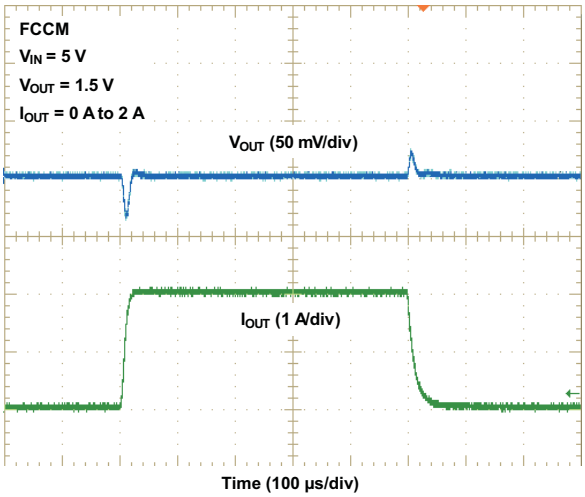

Figure 29. Load Transient – FCCM

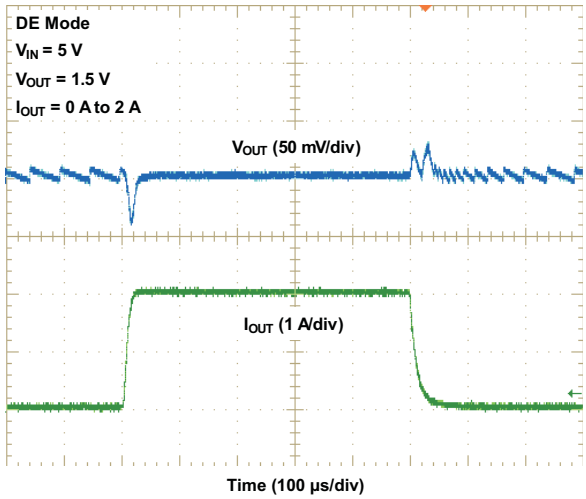

Figure 30. Load Transient – DE Mode

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Typical Characteristics (continued)

Inductor used: PCMC065T-1R0, 1 µH, 5.6 mΩ

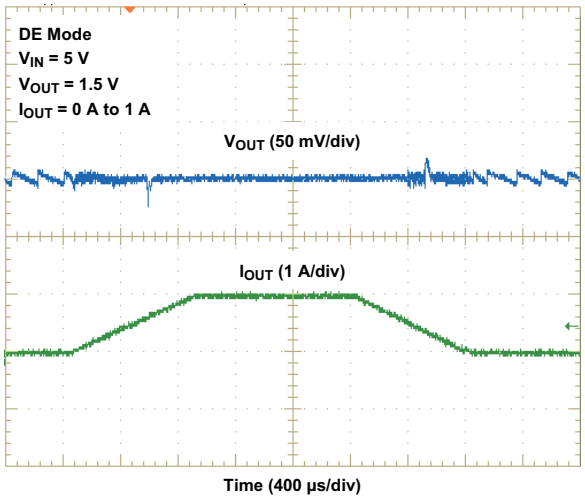


Figure 31. DE Mode DCM and CCM Transition

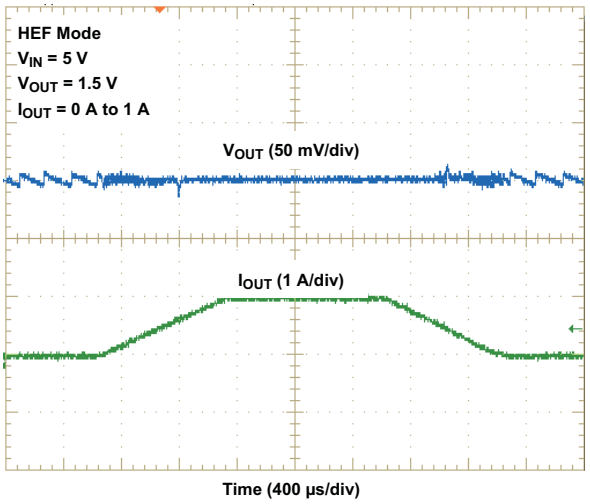


Figure 32. HEF Mode DCM and CCM Transition

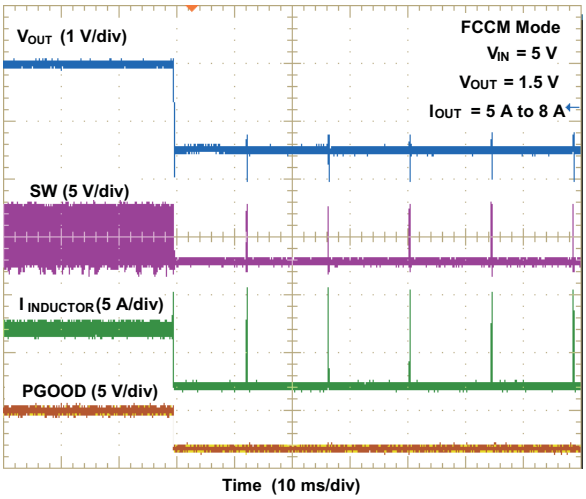


Figure 33. Overcurrent Protection

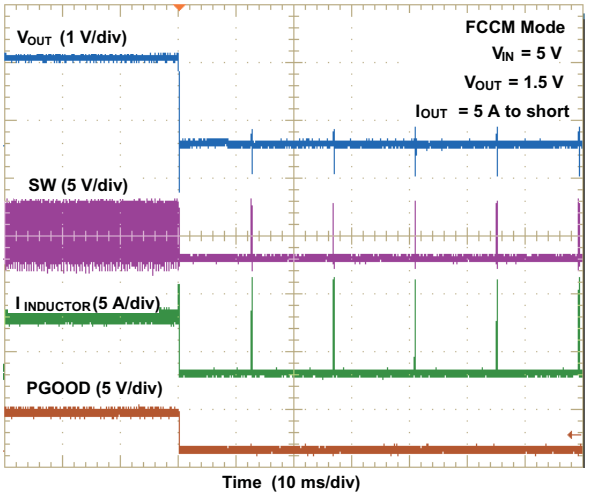


Figure 34. Short-Circuit Protection

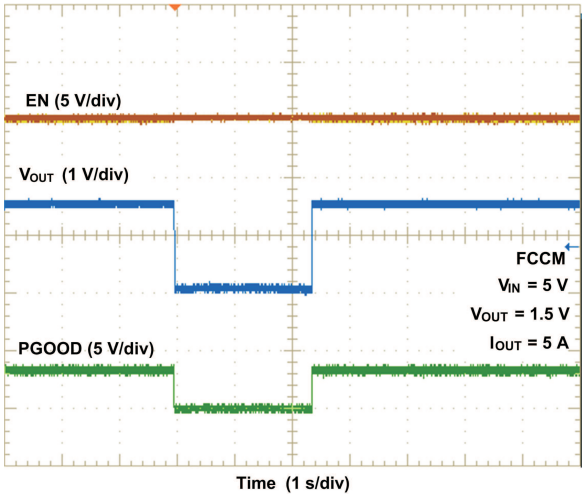


Figure 35. Overtemperature Protection

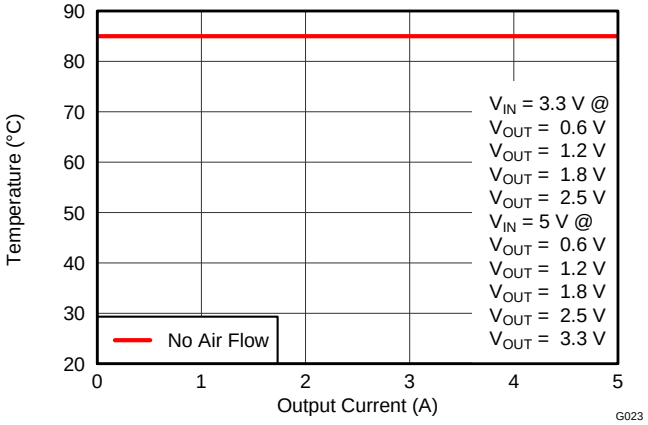


Figure 36. Safe Operating Area

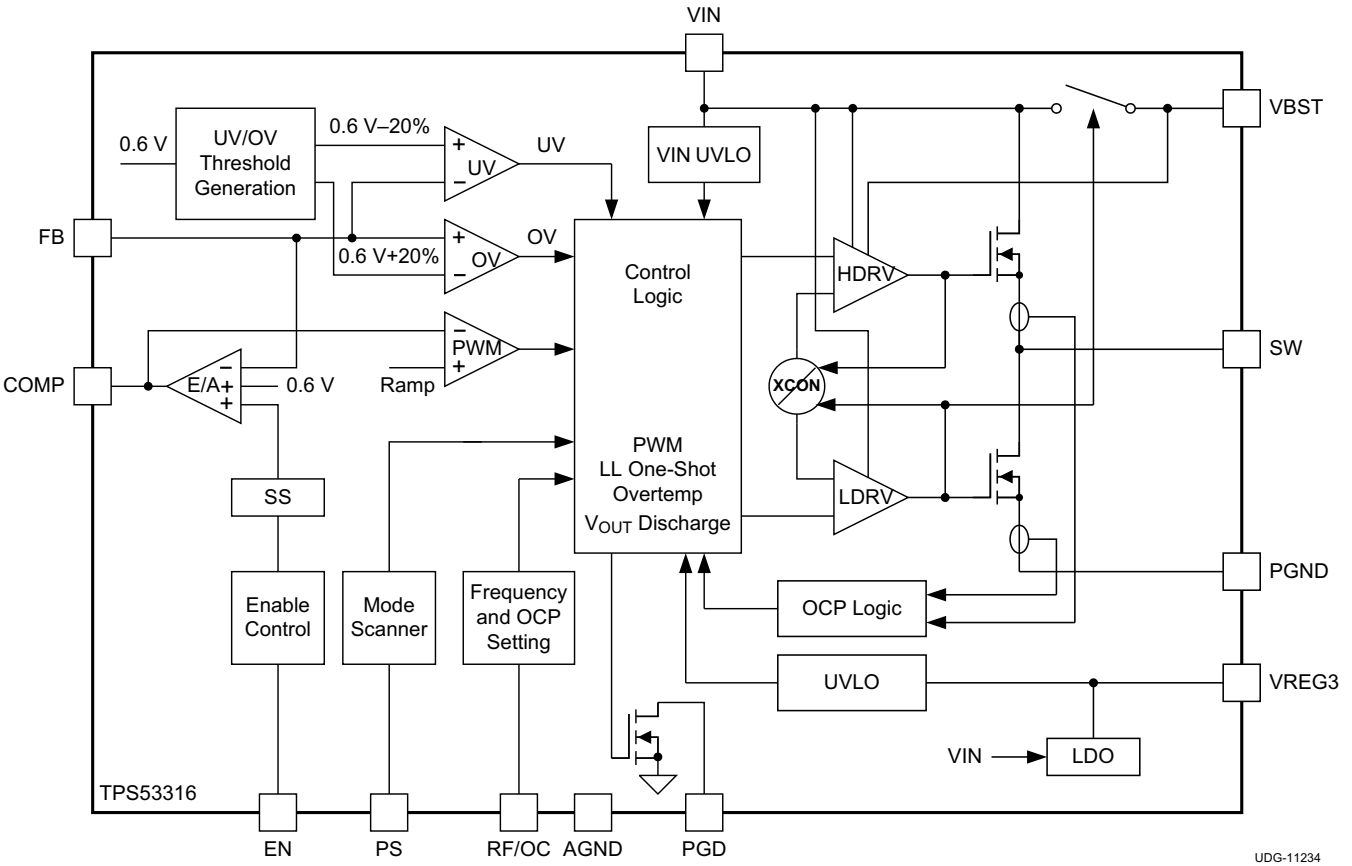
7 Detailed Description

7.1 Overview

The TPS53316 is a high-efficiency switching regulator with two integrated N-channel MOSFETs and is capable of delivering up to 5 A of load current. The TPS53316 provides output voltage from 0.6 V up to 0.8 × V_{IN} from 2.9-V to 6-V wide input voltage range.

This device employs 3 operation modes to fit into various application requirements. The skip mode operation provides reduced power loss and increases the efficiency at light load. The unique, patented PWM modulator enables smooth light load to heavy load transition while maintaining fast load transient.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Overcurrent and Frequency Setting

The overcurrent and frequency setting are determined by RF/OC pin connection as shown in Table 1. At start-up, the RF/OC pin sources 10-µA current and then sense the voltage on this pin to determine the switching frequency and OCP threshold.

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Table 1. Overcurrent and Frequency Setting

RF/OC PIN CONNECTION	FREQUENCY (kHz)	OVERCURRENT THRESHOLD (A)
GND	1100	6.5
24.3 kΩ to GND	750	4.5
57.6 kΩ to GND	750	6.5
105 kΩ to GND	2000	4.5
174 kΩ to GND	2000	6.5
Floating or pulled to VREG3	1100	4.5

7.3.2 Soft-Start Operation

The soft-start operation reduces the inrush current during the start-up time. A slow rising reference is generated by the soft-start circuitry and send to the input of the error amplifier. When the soft-start ramp voltage is less than 600 mV, the error amplifier uses this ramp voltage as the reference. When the ramp voltage reaches 600 mV, the error amplifier switch to a fixed 600-mV reference. The typical soft-start time is 400 µs for 1 × soft-start time setting and 1.6 ms for 4 times the soft-start time setting.

7.3.3 Power Good

The TPS53316 monitors the voltage on the FB pin. If the FB voltage is within 117% and 83% of the reference voltage, the power good signal remains high. If FB voltage is out of this window, power good pin is pulled low by the internal open-drain output.

During start-up operation, the input voltage must be higher than 1 V to have valid power good logic, and the power good signal has 300 µs (1.2 ms with 4 times setting) delay after FB falling into the power good window. There is also 10-µs delay during shutdown after FB falling out of the power good window.

7.3.4 UVLO Function

The TPS53316 provides UVLO protection for input voltage. If the input voltage is higher than UVLO threshold voltage, the device starts up. When the voltage becomes lower than the threshold voltage minus the hysteresis, the device shuts off. The typical UVLO rising threshold is 2.8 V and the hysteresis is 130 mV.

A similar UVLO function is provided to the VREG3 pin. The typical UVLO rising threshold is 2.8 V and the hysteresis is 75 mV for VREG3.

7.3.5 Overcurrent Protection

The TPS53316 continuously monitors the current flowing through high-side and low-side MOSFETs. If the current through the high-side FET exceeds 6.8 A (or 4.5 A with 4.5-A setting), the high-side FET turns off and the low-side FET turns on. An OC counter starts to increment to count the occurrence of the overcurrent events. The converter shuts down immediately when the OC counter reaches 4. The OC counter resets if the detected current is less 6.8 A after an OC event.

Another set of overcurrent circuitry monitors the current through low-side FET. If the current through the low-side FET exceeds 7.5 A (or 5.1 A with 4.5-A setting), the overcurrent protection is engaged and turns off both high-side and low-side FETs immediately. The device is fully protected against overcurrent during both on-time and off-time.

After an OCP event, the device attempts to restart after a hiccup delay (14.5 ms typical). If the OC condition clears before restart, the device starts up normally. Otherwise the hiccup process repeats.

7.3.6 Overvoltage Protection

The TPS53316 monitors the voltage divided feedback voltage to detect the overvoltage and undervoltage conditions. When the feedback voltage is greater than 117% of the reference, the high-side MOSFET turns off and the low-side MOSFET turns on. Then the output voltage drops and reaches the undervoltage threshold. At that point the low-side MOSFET turns off and the device enters high-impedance state.

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7.3.7 Undervoltage Protection

When the feedback voltage is lower than 83% of the reference voltage, the undervoltage protection counter starts. If the feedback voltage remains lower than the undervoltage threshold voltage after 10 µs, the device turns off both high-side and low-side MOSFETs and enters high-impedance state. After a hiccup delay (14.5 ms typical), the device attempts to restart. If the UV condition clears before restart, the device starts up normally. Otherwise the hiccup process repeats.

7.3.8 Overtemperature Protection

The TPS53316 continuously monitors the die temperature. If the die temperature exceeds the threshold value (140°C typical), the device shuts off. When the device is cooled to 40°C below the overtemperature threshold, it restarts and returns to normal operation.

7.3.9 Output Discharge

When the EN pin is low, the TPS53316 discharges the output capacitors through an internal MOSFET switch between SW and GND while the high-side and low-side MOSFETs remain OFF. The typical discharge switch-ON resistance is 60 Ω. This function is disabled when the input voltage is less than 1 V.

7.4 Device Functional Modes

7.4.1 Operation Mode

The TPS53316 has 3 operation modes determined by PS connection as listed in Table 2. Each mode has two soft-start and power good delay options (1 time and 4 times). At start-up, the PS pin sources 10 µA of current and then sense the voltage on this pin to determine the operation mode and soft-start time.

Table 2. Operation Mode Selection

PS PIN CONNECTION	OPERATION MODE	AUTO-SKIP AT LIGHT LOAD	SOFT-START TIME
GND	FCCM	No	4 times
24.3 kΩ to GND	HEF Mode	Yes	4 times
57.6 kΩ to GND	HEF Mode	Yes	1 times
105 kΩ to GND	DE Mode	Yes	1 time
174 kΩ to GND	DE Mode	Yes	4 times
Floating or pulled to VREG3	FCCM	No	1 time

In forced continuous conduction mode (FCCM), the high-side FET is ON during the on-time and low-side FET is ON during the off-time. The switching is synchronized to the internal clock thus the switching frequency is fixed.

In diode emulation mode (DE), the high-side FET is ON during the on-time and low-side FET is ON during the off-time until the inductor current reaches zero. An internal zero-crossing comparator detects the zero crossing of inductor current from positive to negative. When the inductor current reaches zero, the comparator sends a signal to the logic control and turns off the low-side FET.

When the load is increased, the inductor current is always positive and the zero-crossing comparator does not send a zero-crossing signal. The converter enters into continuous conduction mode (CCM) when no zero-crossing is detected for two consecutive PWM pulses. The switching is synchronized to the internal clock and the switching frequency is fixed.

In high-efficiency mode (HEF), the converter does not synchronize to internal clock during CCM. Instead, the PWM modulator determines the switching frequency. The operation in discontinuous conduction mode (DCM) is the same as DE mode.

In both DE and HEF modes, the device operates under CCM with fixed SW frequency if the load current is higher than half of the inductor ripple current. When the load current is decreased and seven consecutive zero-crossing events are detected, the device enters DCM and light load control is enabled. The on-pulse in DCM is designed to be 25% higher than CCM to provide hysteresis to avoid chattering between CCM and DCM.

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The PS pins also set the soft-start time and power good start-up delay of the device. The nominal sort-start time is 400 µs from the time V_{OUT} = 0 V to when V_{OUT} = 100%, and the nominal power good delay is 300 µs from the time V_{OUT} = 100% to when power good is asserted. When the PS pin is connected to GND directly or with a resistor with a value of 24.3 kΩ or 174 kΩ, the soft-start time and power good delay is 4 times the nominal (1.6 ms for soft-start time and 1.2 ms for power good delay).

7.4.2 Light Load Operation

In skip modes (DE and HEF) when the load current is less than half of inductor ripple current, the inductor current reaches zero by the end of off-time. The light load control scheme then turns off the low-side MOSFET when inductor current reaches zero. Because there is no negative inductor current, the energy delivered to the load per switching cycle is increased compared to the normal PWM mode operation. The controller then reduces the switching frequency to maintain the output voltage regulation. The switching loss is reduced and thus efficiency is improved.

In both DE and HEF mode, when the load current decreases, the switching frequency also decreases continuously in discontinuous conduction mode (DCM). When the load current is 0 A, the minimum switching frequency is reached. It is also required that the difference between V_{VBST} and V_{SW} to be higher than 2.4 V to ensure the supply for high-side gate driver.

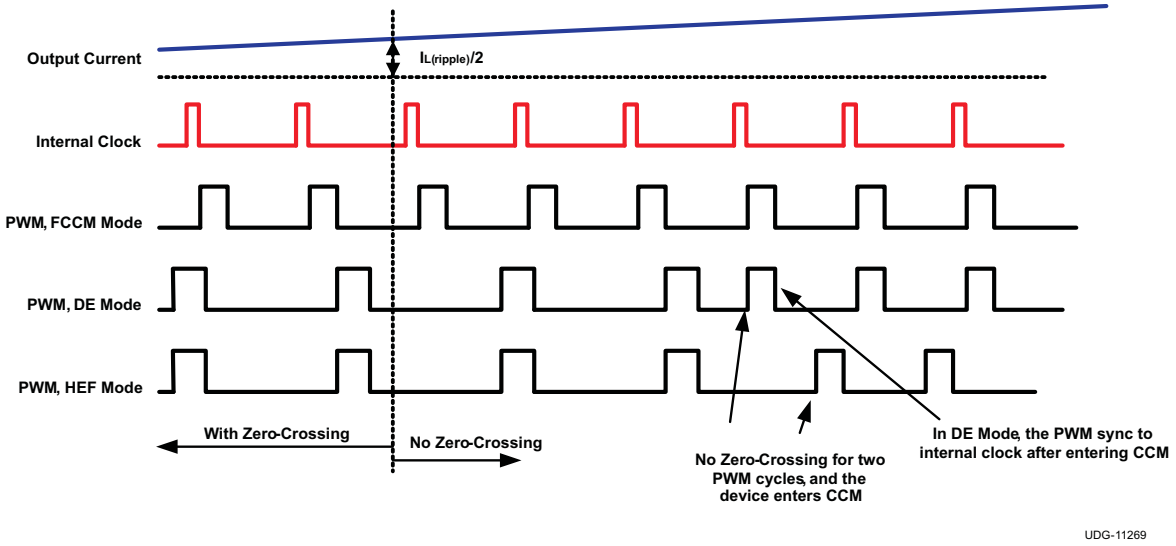

Figure 37. TPS53316 Operation Modes in Light and Heavy Load Conditions

7.4.3 Forced Continuous Conduction Mode

When the PS pin is grounded or greater than 2.2 V, the TPS53316 is operating in continuous conduction mode in both light and heavy load condition. In this mode, the switching frequency remains constant over the entire load range which is suitable for applications requiring tight control of switching frequency at a cost of lower efficiency at light load.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS53316 device is a high-efficiency synchronous-buck converter. The device suits low output voltage point-of-load applications with 5-A or lower output current in computing and similar digital consumer applications.

8.2 Typical Application

This design example describes a voltage-mode, 5-A synchronous buck converter with integrated MOSFETs. The device provides a fixed 1.5-V output at up to 5 A from a 5-V input bus.

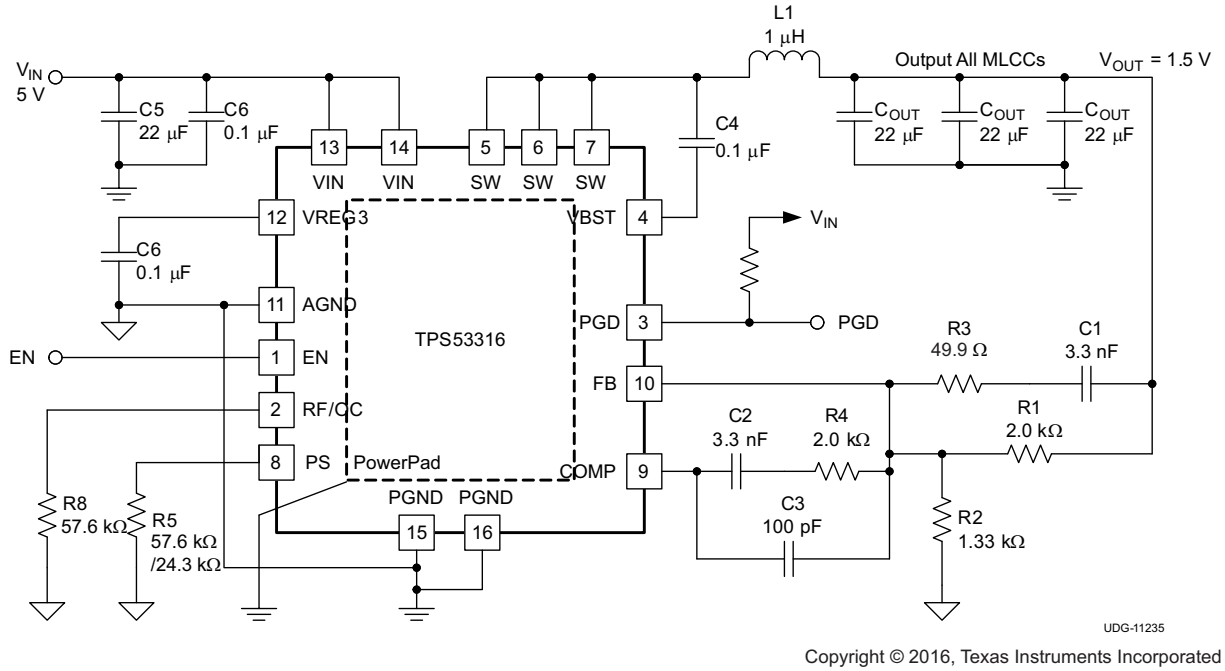

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Figure 38. Typical 3.3-V Input Application Circuit Diagram

8.2.1 Design Requirements

Table 3 lists the parameters for this design example.

Table 3. TPS53316 Design Example Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS					
Voltage range	V_{IN}	2.9	3.3 or 5	6	V
Maximum input current	V_{IN} = 5 V, I_{OUT} = 5 A		1.76		A
No load input current	No load input current V_{IN} = 5 V, I_{OUT} = 0 A under DE/HEF mode		3		mA

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Typical Application (continued)

Table 3. TPS53316 Design Example Specifications (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT CHARACTERISTICS					
Output voltage			1.5		V
Output voltage regulation	Setpoint accuracy (V_{IN} = 2.9 V – 6 V, I_{OUT} = 0 A – 5 A)	–1%		1%	
	Line regulation (V_{IN} = 2.9 V – 6 V, I_{OUT} = 5 A)		0.1%		
	Load regulation (V_{IN} = 5 V, I_{OUT} = 0 A – 5 A)		0.1%		
Output voltage ripple	V_{IN} = 5 V, I_{OUT} = 5 A		10		mVPP
Output load current		0		5	A
Overcurrent limit	V_{IN} = 3.3V, f_{SW} = 750 kHz		6.5 or 4.5		A
SYSTEM CHARACTERISTICS					
Switching frequency			0.75		MHz
Peak efficiency	V_{IN} = 5 V, I_{OUT} = 1.8 A, f_{SW} = 750 kHz		92.7%		
Full-load efficiency	V_{IN} = 5 V, I_{OUT} = 5 A, f_{SW} = 750 kHz		89%		
Operating temperature			25		°C

8.2.2 Detailed Design Procedure

Select the external components using the following steps.

8.2.2.1 Determine the Value of R1 and R2

The output voltage is programmed by the voltage-divider resistor, R1 and R2 shown in Figure 38. R1 is connected between VFB pin and the output, and R2 is connected between the VFB pin and GND. Recommended value for R1 is between 1 kΩ and 10 kΩ. Determine R2 using Equation 1.

$$R2 = \frac{0.6}{V_{OUT} - 0.6} \times R1 \quad (1)$$

8.2.2.2 Choose the Inductor

The inductance value must be determined to give the ripple current of approximately 20% to 40% of maximum output current. The inductor ripple current is determined by Equation 2.

$$I_{L(ripple)} = \frac{1}{L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (2)$$

The inductor also must have a low DCR to achieve good efficiency, as well as enough room above peak inductor current before saturation.

8.2.2.3 Choose the Output Capacitor(s)

The output capacitor selection is determined by output ripple and transient requirement. When operating in CCM, the output ripple has three components. $V_{RIPPLE(C)}$ represents the ripple due to the output capacitance and is shown in Equation 4.

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)} \quad (3)$$

$$V_{RIPPLE(C)} = \frac{I_{L(ripple)}}{8 \times C_{OUT} \times f_{SW}} \quad (4)$$

$$V_{RIPPLE(ESR)} = I_{L(ripple)} \times ESR \quad (5)$$

$$V_{RIPPLE(ESL)} = \frac{V_{IN} \times ESL}{L} \quad (6)$$

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When ceramic output capacitor is chosen, the ESL component is usually negligible. In the case when multiple output capacitors are used, the total ESR and ESL must be the equivalent of the all output capacitors in parallel.

When operating in DCM, the output ripple is dominated by the component determined by capacitance. It also varies with load current and can be expressed as shown in Equation 7.

$$V_{RIPPLE(DCM)} = \frac{\left(\alpha \times I_{L(ripple)} - I_{OUT}\right)^2}{2 \times f_{SW} \times C_{OUT} \times I_{L(ripple)}}$$

where

- α is the DCM on-time coefficient (typical value is 1.25) and can be expressed as $\alpha = \frac{t_{ON(DCM)}}{t_{ON(CCM)}}$ (7)

Figure 39 illustrates the DCM output voltage ripple.

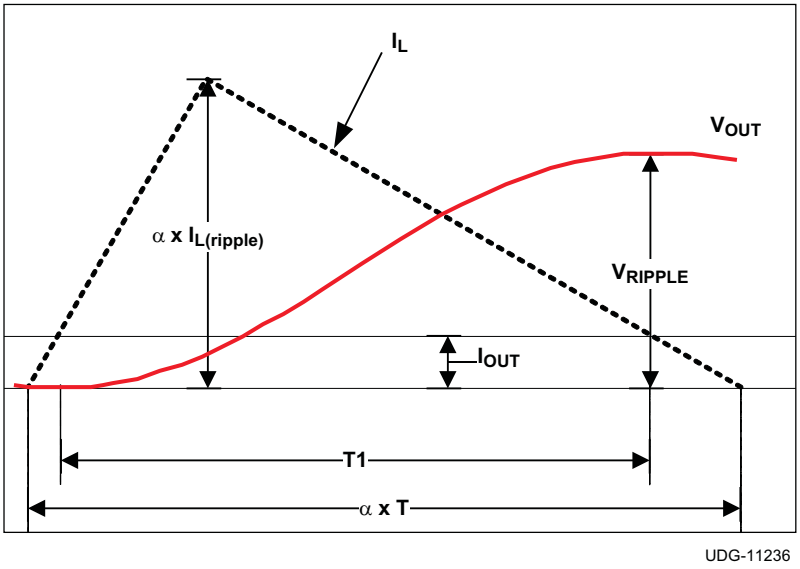

Figure 39. Discontinuous Mode Output Voltage Ripple

8.2.2.4 Choose the Input Capacitors

The selection of input capacitor must be determined by the ripple current requirement. The ripple current generated by the converter must be absorbed by the input capacitors as well as the input source. The RMS ripple current from the converter can be expressed as shown in Equation 8.

$$I_{IN(ripple)} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

where

- D is the duty cycle and can be expressed as $D = \frac{V_{OUT}}{V_{IN}}$ (8)

To minimize the ripple current drawn from the input source, sufficient input decoupling capacitors must be placed close to the device. The ceramic capacitor is recommended due to the low ESR and low ESL. The input voltage ripple can be calculated in Equation 9 when the total input capacitance is determined.

$$V_{IN(ripple)} = \frac{I_{OUT} \times D}{f_{SW} \times C_{IN}} \quad (9)$$

8.2.2.5 Compensation Design

The TPS53316 employs voltage mode control. To effectively compensation the power stage and ensures fast transient response, Type III compensation is typically used.

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The control to output transfer function can be described in Equation 10.

$$G_{CO} = 4 \times \frac{1 + s \times C_{OUT} \times ESR}{1 + s \times \left(\frac{L}{DCR + R_{LOAD}} + C_{OUT} \times (ESR + DCR) \right) + s^2 \times L \times C_{OUT}} \quad (10)$$

The output LC filter introduces a double pole which can be calculated in Equation 11.

$$f_{DP} = \frac{1}{2 \times \pi \times \sqrt{L \times C_{OUT}}} \quad (11)$$

The ESR zero of can be calculated in Equation 12.

$$f_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}} \quad (12)$$

Figure 40 shows the configuration of Type III compensation and typical pole and zero locations. Equation 13 through Equation 15 describe the compensator transfer function and poles and zeros of the Type III network.

$$G_{EA} = \frac{(1 + s \times C1 \times (R1 + R3))(1 + s \times R4 \times C2)}{(s \times R1 \times (C2 + C3)) \times (1 + s \times C1 \times R3) \times \left(1 + s \times R4 \frac{C2 \times C3}{C2 + C3}\right)} \quad (13)$$

$$f_{Z1} = \frac{1}{2 \times \pi \times R4 \times C2} \quad (14)$$

$$f_{Z2} = \frac{1}{2 \times \pi \times (R1 + R3) \times C1} \cong \frac{1}{2 \times \pi \times R1 \times C1} \quad (15)$$

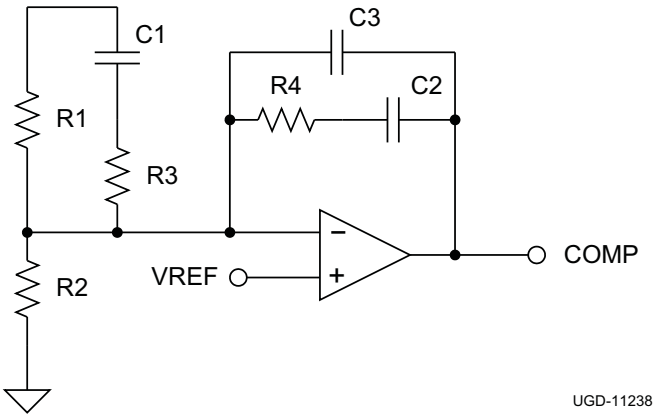

Figure 40. Type III Compensation Network Schematic

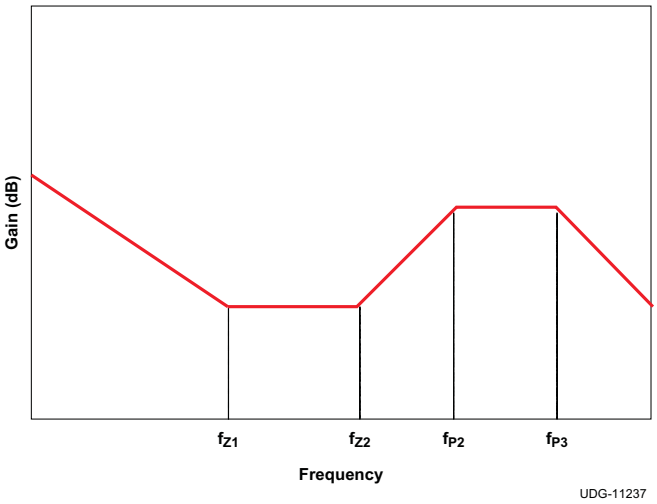

Figure 41. Type III Compensation Network Waveform

$$f_{P1} = 0 \quad (16)$$

$$f_{P2} = \frac{1}{2 \times \pi \times R3 \times C1} \quad (17)$$

$$f_{P3} = \frac{1}{2 \times \pi \times R4 \times \left(\frac{C2 \times C3}{C2 + C3} \right)} \cong \frac{1}{2 \times \pi \times R4 \times C3} \quad (18)$$

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The two zeros can be placed near the double-pole frequency to cancel the response from the double pole. One pole can be used to cancel ESR zero, and the other non-zero pole can be placed at half switching frequency to attenuate the high frequency noise and switching ripple. Suitable values can be selected to achieve a compromise between high phase margin and fast response. A phase margin higher than 45° is required for stable operation.

For DCM operation, a C3 capacitor value between 56 pF and 150 pF is recommended for output capacitance between 20 µF to 200 µF.

8.2.3 Application Curves

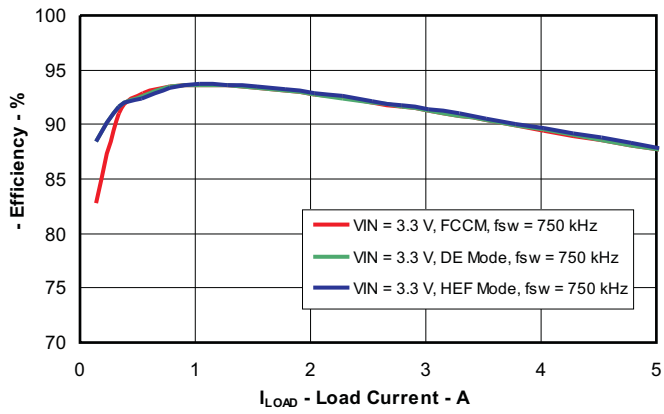

Figure 42. 3.3-V Input Efficiency

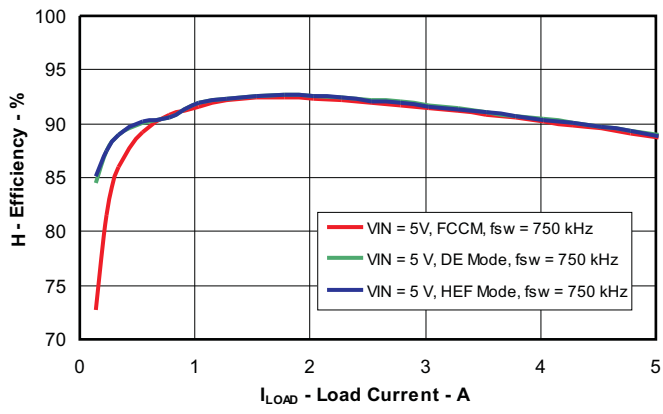

Figure 43. 5-V Input Efficiency

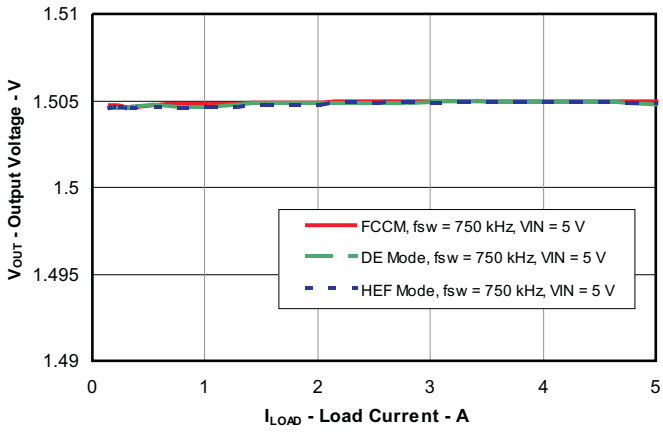

Figure 44. Load Regulation

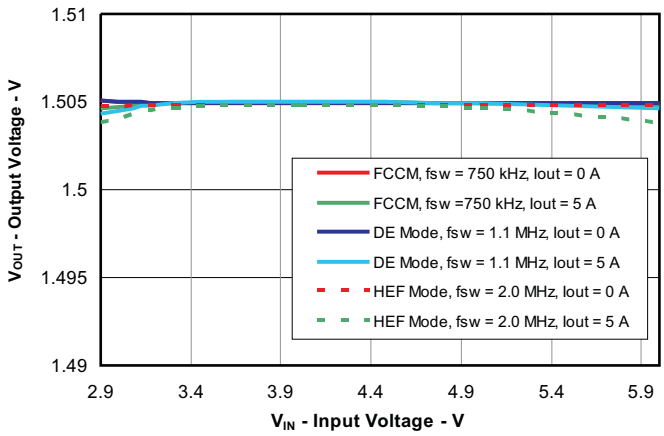

Figure 45. Line Regulation

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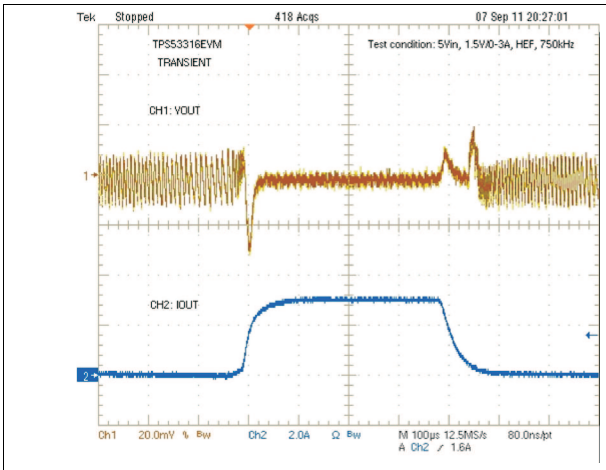
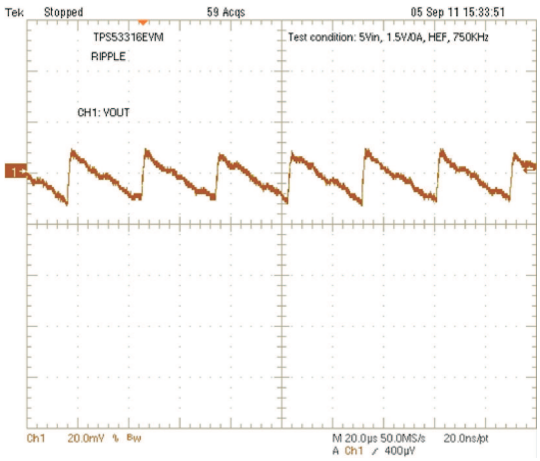


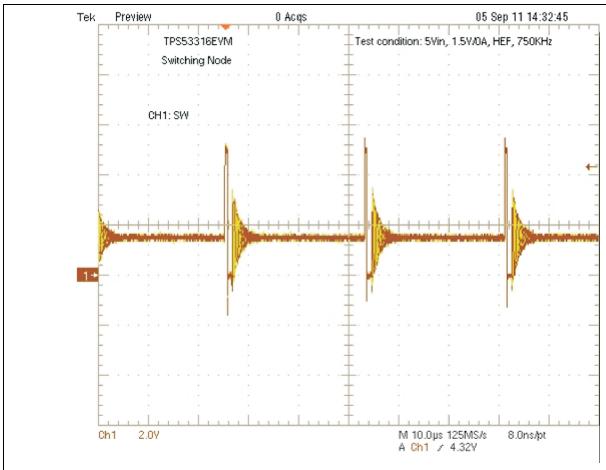
5-V VIN, 1.5-V VOUT, HEF Mode, and f_{SW} = 750 kHz

Figure 46. Load 0-3 A Transient Under HEF Mode



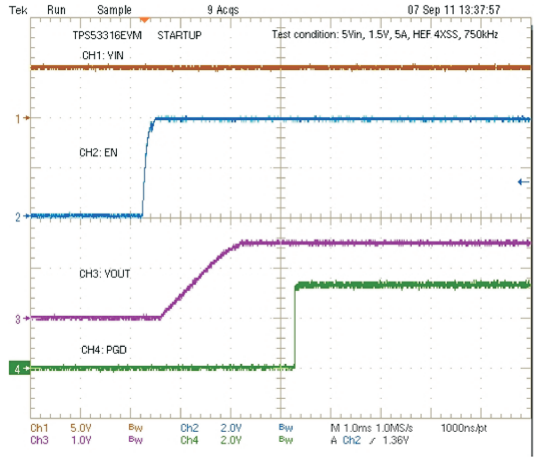
5-V VIN, 1.5-V VOUT, 0-A, HEF Mode, and f_{SW} = 750 kHz

Figure 47. Output Ripple



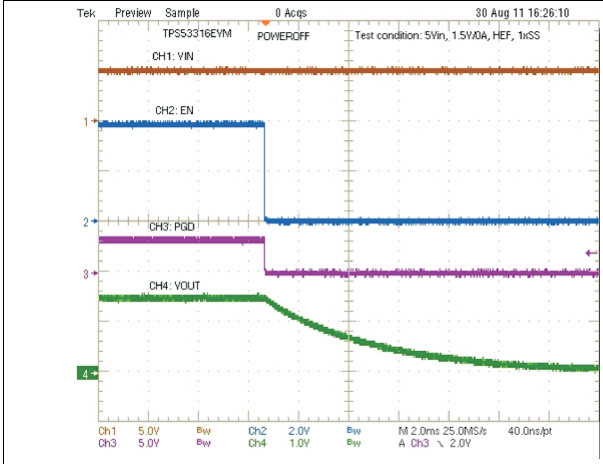
5-V VIN, 1.5-V VOUT, 0-A, HEF Mode, and f_{SW} = 750 kHz

Figure 48. Switching Node



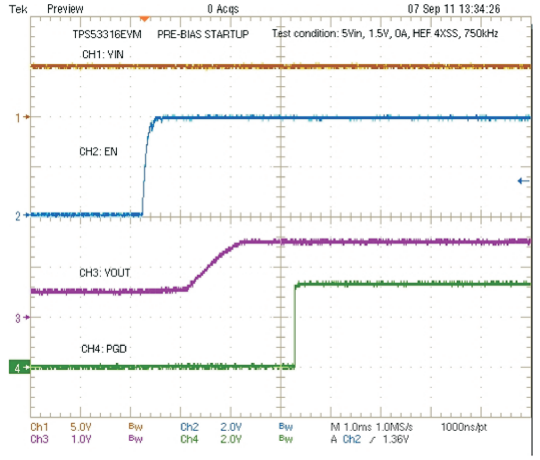
5-V VIN, 1.5-V VOUT, 5-A IOUT, and 4 times soft start

Figure 49. Turnon Waveform



5-V VIN, 1.5-V VOUT, and 0-A IOUT

Figure 50. Turnoff Waveform



5-V VIN, 1.5-V VOUT, 0-A IOUT, 4 times soft start, and 0.5-V prebias

Figure 51. Prebias Turnon Waveform

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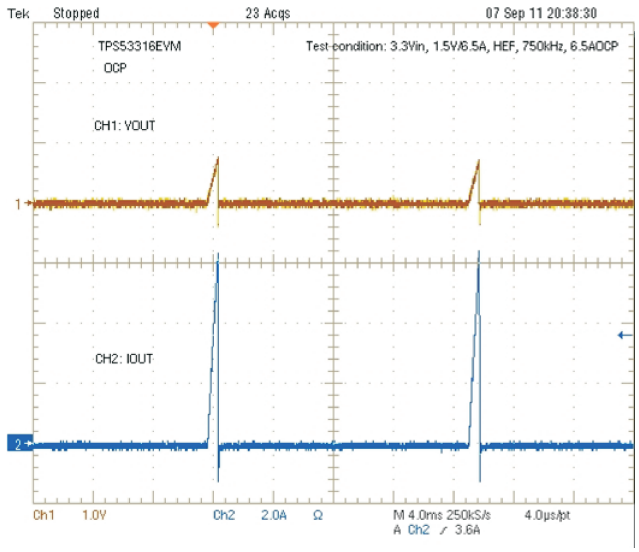

3.3-V VIN, 1.5-V VOUT, 6.5-A IOUT, 4 times soft start, 750 kHz, and 6.5-A OCP

Figure 52. Overcurrent Protection Waveform

5-V VIN, 1.5-V VOUT, 5-A IOUT, HEF mode, and f_{SW} = 750 kHz

Figure 53. Loop Gain

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9 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 2.9 V and 6 V. The input voltage source VIN must be a 0-V to 6-V variable DC source capable of supplying 5 ADC. Proper bypassing of input supplies is also critical for noise performance, as is PCB layout and grounding scheme. See the recommendations in *Layout*.

10 Layout

10.1 Layout Guidelines

Good layout is essential for stable power supply operation. Follow these guidelines for an efficient PCB layout:

- Separate the power ground and analog ground. Connect analog ground to GND plane with single via or a 0-Ω resistor at a quiet place.
- Use 4 vias to connect the thermal pad to power ground.
- Place VIN and VREG3 decoupling capacitors as close to the device as possible.
- Use wide traces for VIN, VOUT, PGND and SW. These nodes carry high-current and also serve as heat sinks.
- Place feedback and compensation components as close to the device as possible.
- Keep analog signals (FB, COMP) away from noisy signals (SW, VBST).
- See *5-A Step-Down Regulator with Integrated Switcher* (SLUU671) for a layout example.

10.2 Layout Example

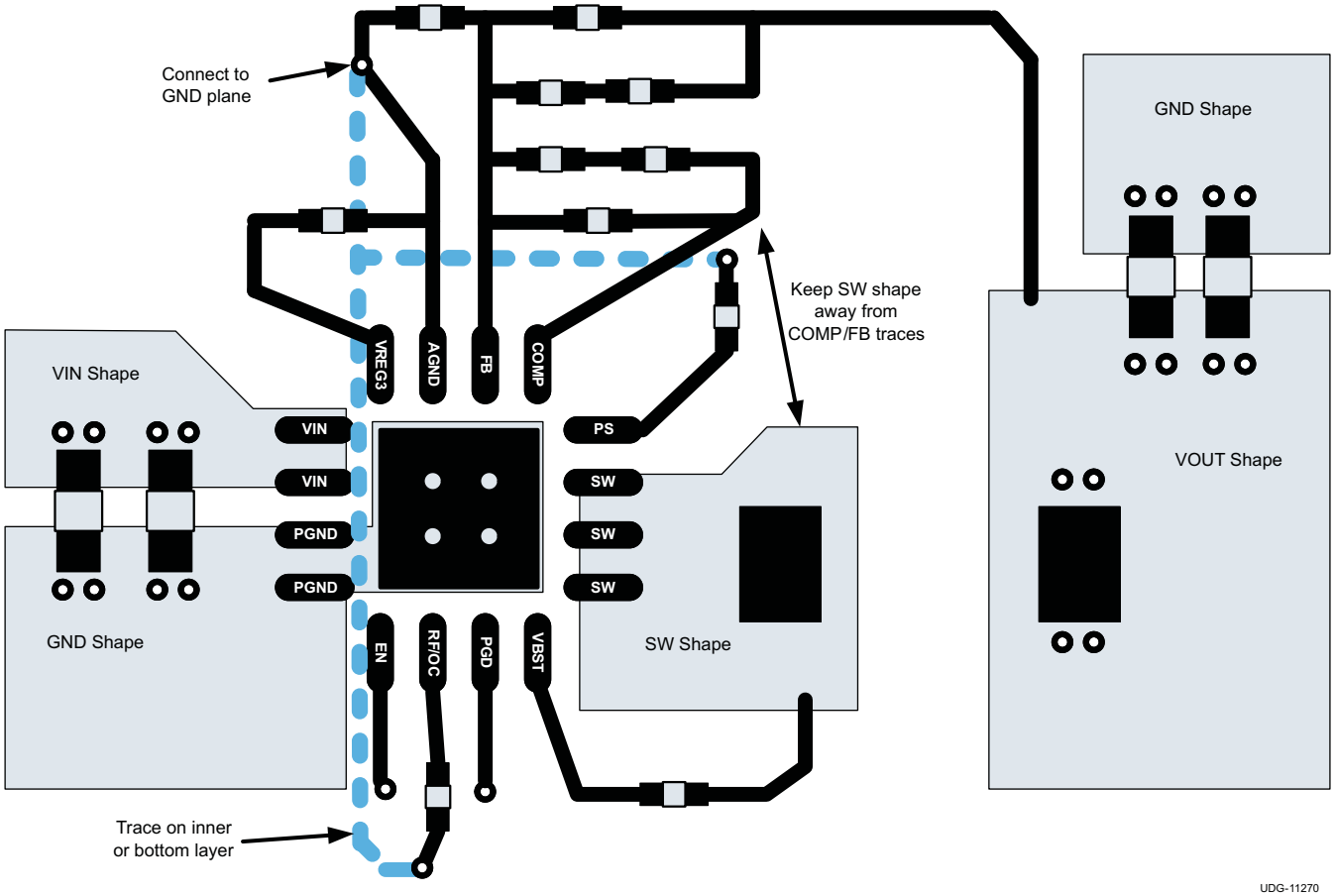

Figure 54. Layout Recommendation

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

5-A Step-Down Regulator with Integrated Switcher (SLUU671)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

SmoothPWM, Eco-Mode, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS53316RGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	3316	Samples
TPS53316RGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	3316	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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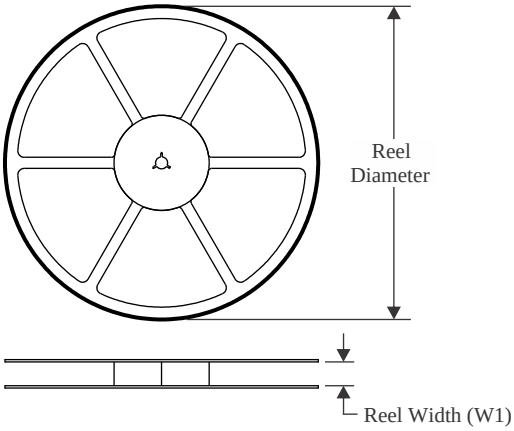
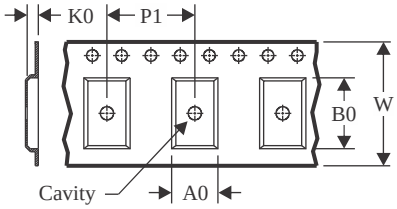
TAPE AND REEL INFORMATION

REEL DIMENSIONS

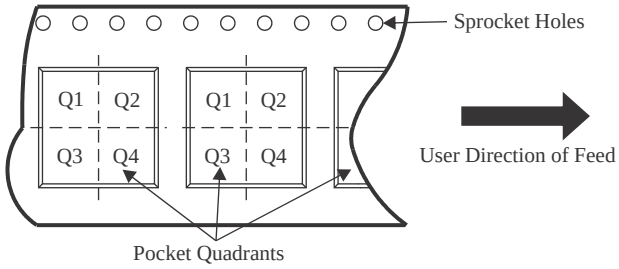


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

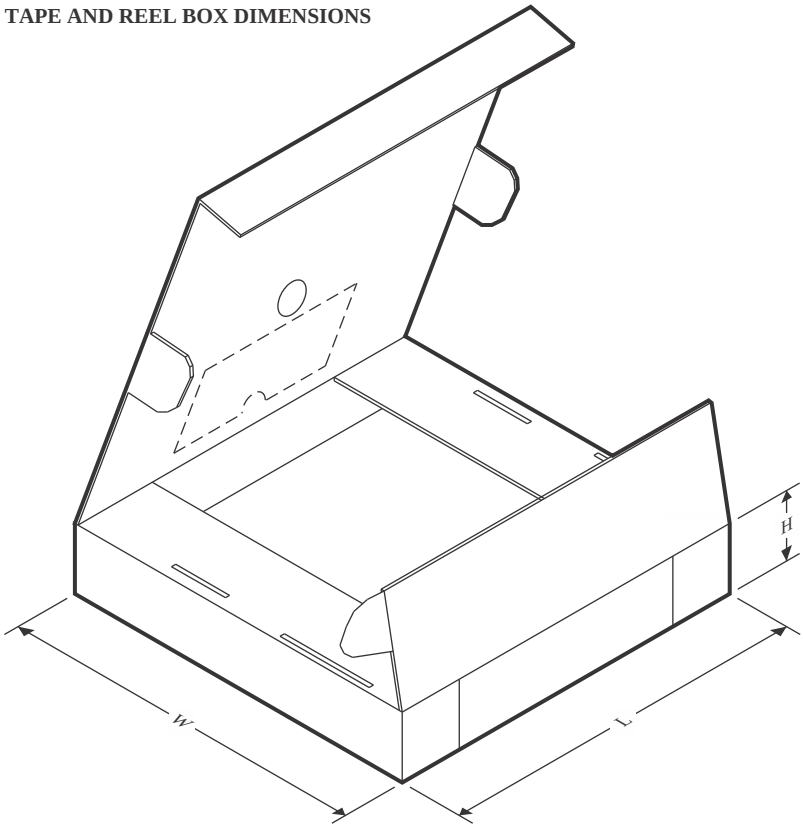
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53316RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS53316RGTT	VQFN	RGT	16	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

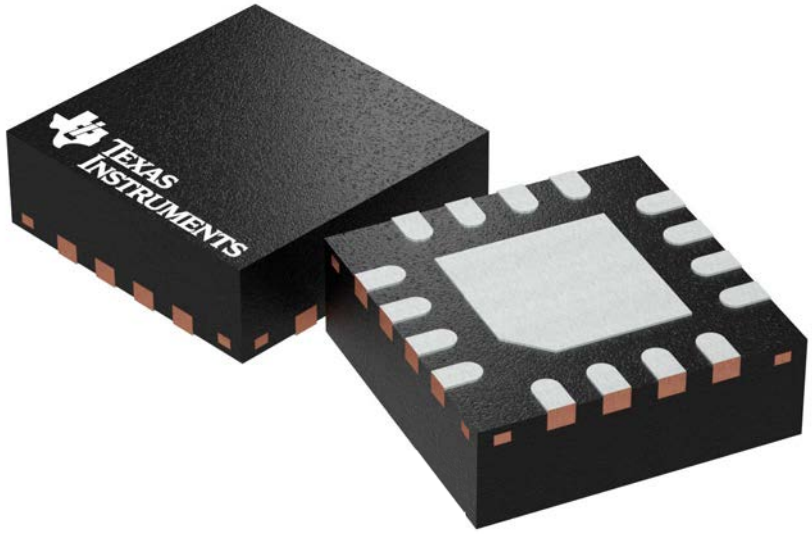


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53316RGTR	VQFN	RGT	16	3000	338.0	355.0	50.0
TPS53316RGTT	VQFN	RGT	16	250	205.0	200.0	33.0

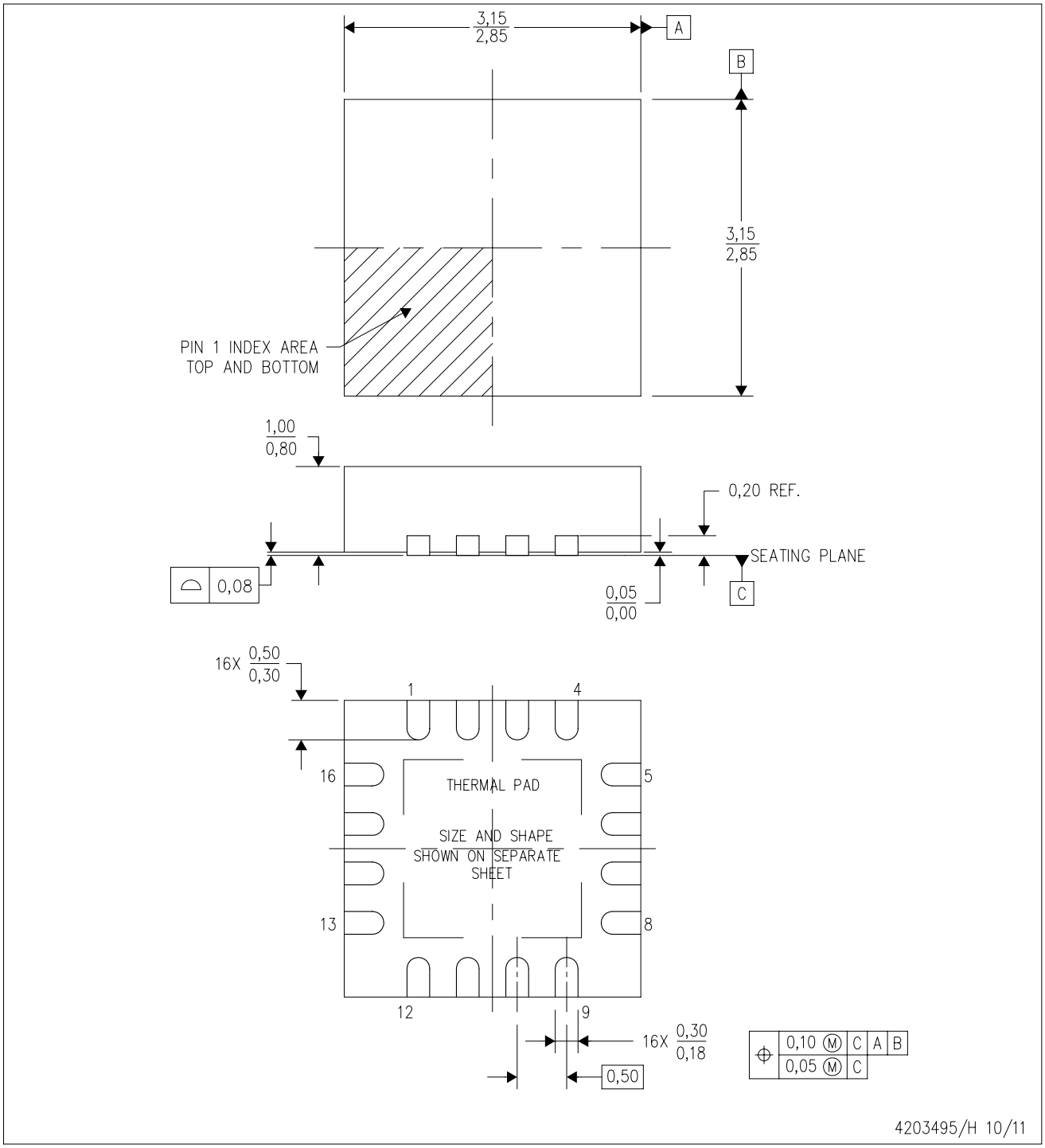
RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

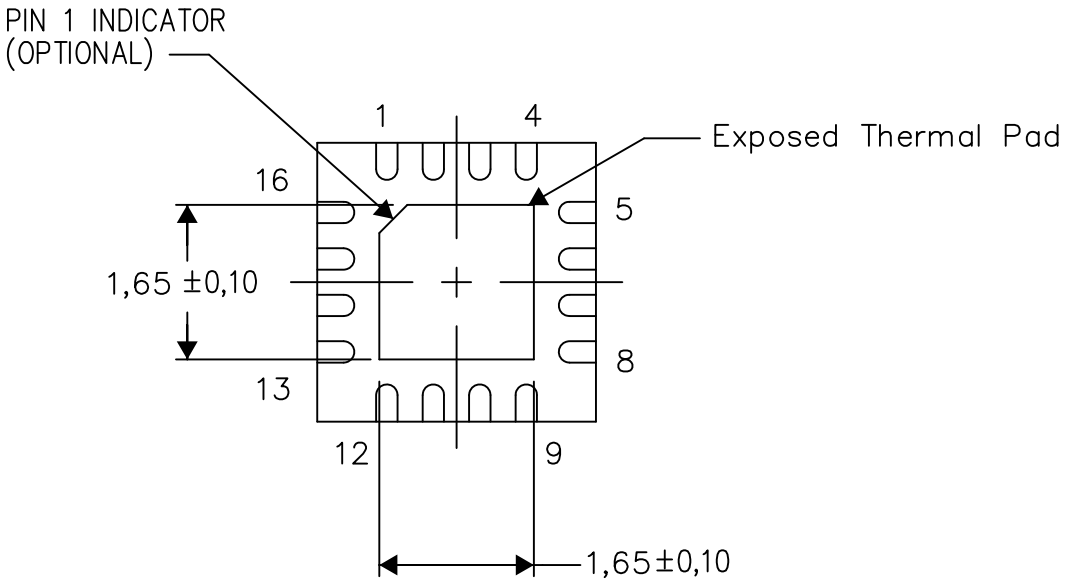
RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206349–7/Z 08/15

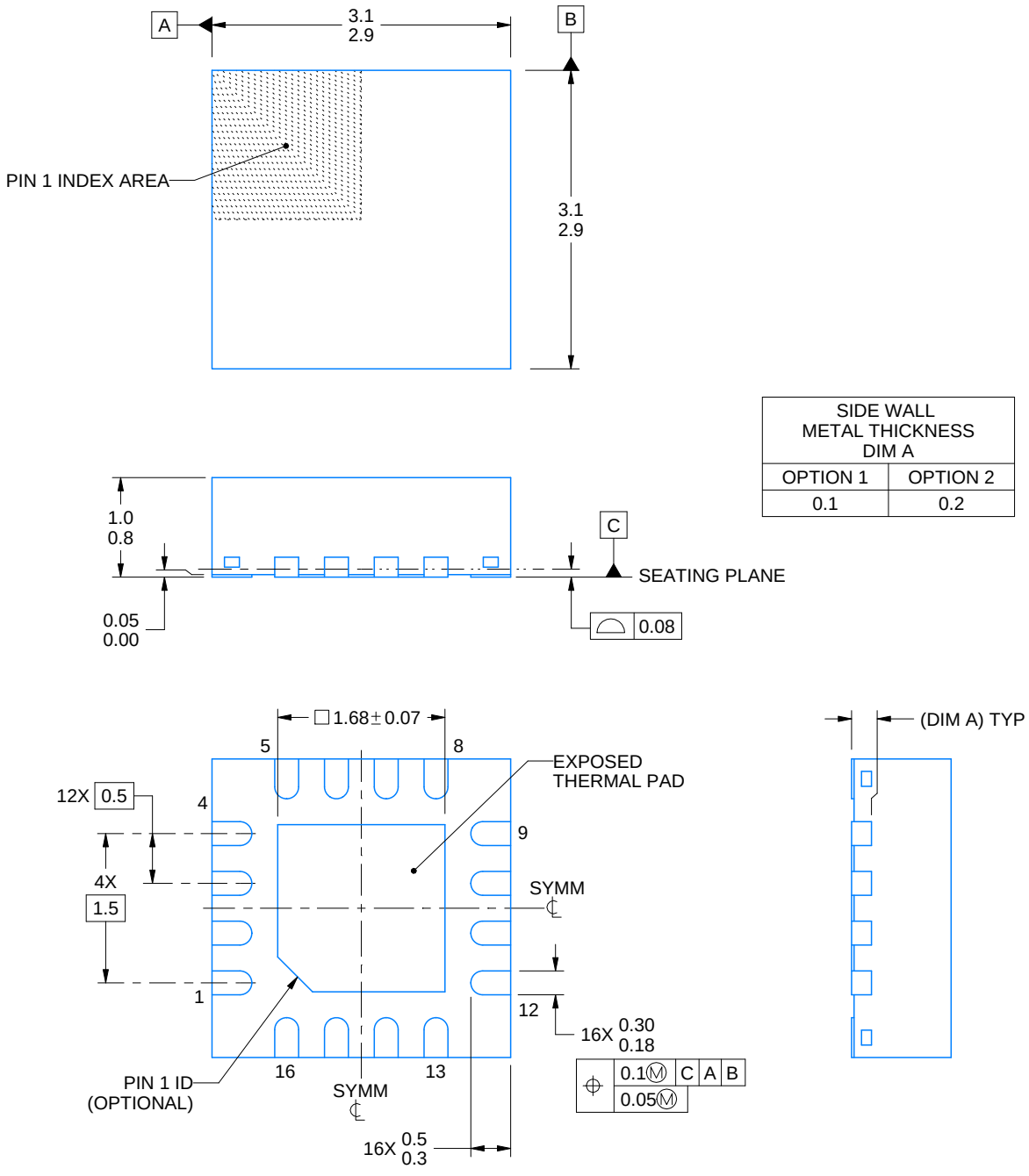
NOTE: All linear dimensions are in millimeters

PACKAGE OUTLINE

RGT0016C

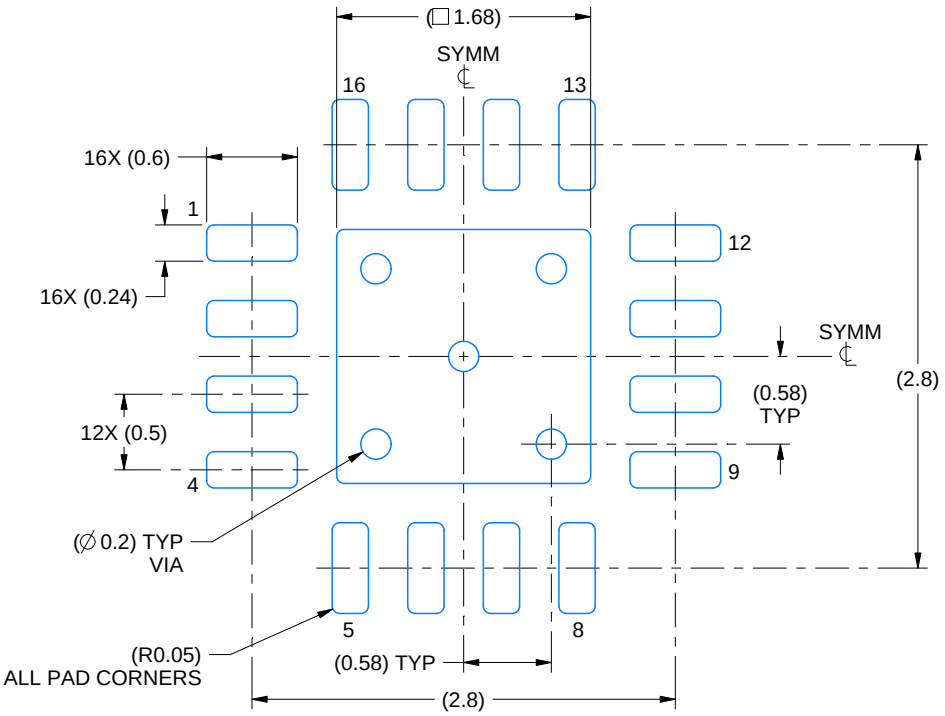
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

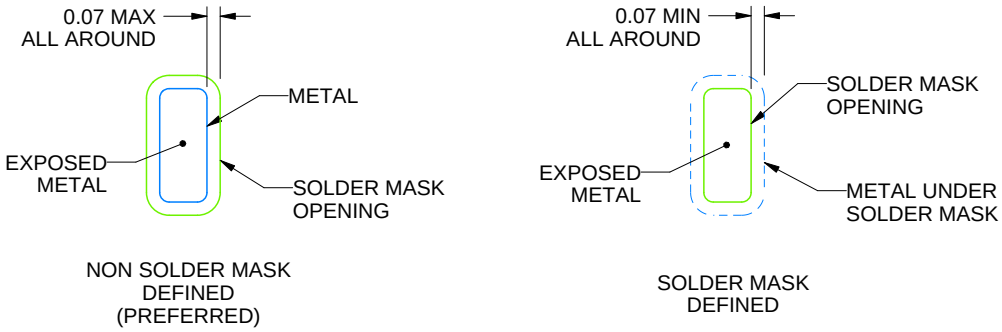


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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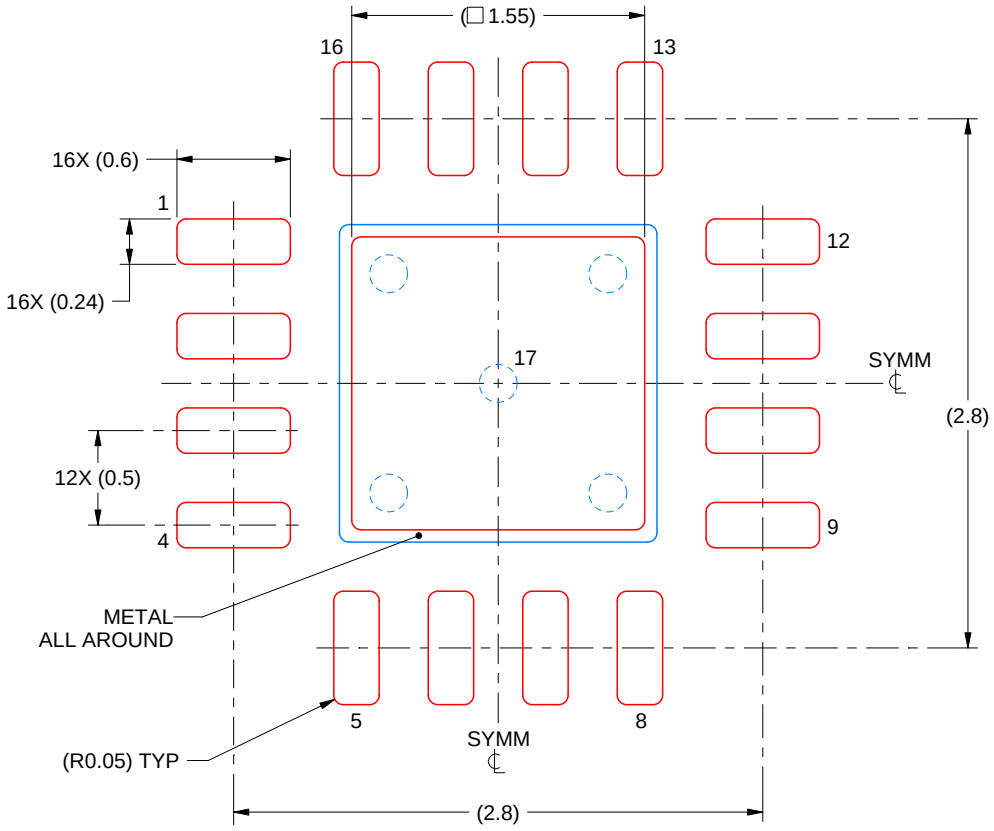
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/D 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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