1 Features

- Increases System Operation Time Between Charges
  - Configurable 300-mA Buck Regulator (1.8-V Default)
  - 700 nA (typical) Iq with Buck Converter Enabled (No Load)
  - Configurable Load Switch or 100mA LDO Output (Load Switch by Default)
  - Up to 300-mA Charge Current for Fast Charging
  - 0.5% Accurate Battery Voltage Regulation (Configurable from 3.6 V to 4.65 V in 10-mV Steps)
  - Configurable Termination Current Down to 500 µA
  - Simple Voltage Based Battery Monitor
- Highly Integrated Solution with Small Footprint
  - 2.5 mm x 2.5 mm WCSP Package and 6 External Components for Minimal Solution
  - Push-Button Wake-Up and Reset with Adjustable Timers
  - Power Path Management for Powering the System and Charging the Battery
  - Power Path Management enables <50 nA Ship Mode Battery Quiescent Current for Longest Shelf Life
  - Battery Charger Operates from 3.4 V – 5.5 V IN (5.5-V OVP / 20-V Tolerant)
  - Dedicated Pins for Input Current Limit, Charge Current, Termination Current, and Status Output
- \( \text{I}^2\text{C} \) Communication Control
  - Charge Voltage and Current
  - Termination Threshold
  - Input Current Limit
  - VINDPM Threshold
  - Timer Options
  - Load Switch Control
  - Controls for Interrupts for Faults and Status
  - System Output Voltage Adjustment
  - LDO Output Voltage Adjustment

2 Applications

- Smart Watches and other Wearable Devices
- Fitness Accessories
- Health Monitoring Medical Accessories
- Rechargeable Toys

3 Description

The bq2512x is a highly integrated battery charge management IC that integrates the most common functions for wearable devices: Linear charger, regulated output, load switch, manual reset with timer, and battery voltage monitor. The integrated buck converter is a high efficiency, low \( \text{I}_0 \) switcher using DCS control that extends light load efficiency down to 10-µA load currents. The low quiescent current during operation and shutdown enables maximum battery life. The device supports charge currents from 5 mA to 300 mA. The input current limit, charge current, buck converter output voltage, LDO output voltage, and other parameters are programmable through the \( \text{I}^2\text{C} \) interface.

Device Information(1)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>BQ2512x</td>
<td>DSBGA (25)</td>
<td>2.50 mm x 2.50 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic

---

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
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2 Applications .......................................................... 1
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7 Pin Configuration and Functions ................................. 5
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 2016) to Revision C

- Changed or expanded descriptive text in the Pin Functions table for several pin names. ........................................... 5
- Deleted sentence: “For proper operation of the device...” from the BAT pin Description in the Pin Functions table. ...... 6
- Changed term From: V_{(OCP)} To: V_{(OVP)} in Conditions statement of Electrical Characteristics. ................................. 9
- Deleted I_{(O)} spec ..................................................... 10
- Added T_{j} = -40°C to 60°C to Conditions for I_{(N)} spec. and deleted 0 from TYP column .............................................. 12
- Changed Conditions statement for Typical Start-Up Timing and Operation timing diagram. ............................... 14
- Changed Conditions statement for Battery Operation and Sleep Mode timing diagram. ........................................ 15
- Changed Q3, Q4, and Q5 symbols in the Functional Block Diagram to PFET devices ................................................... 18
- Changed text in Ship Mode section for clarity. ........................................... 19
- Changed text in Active Battery Only Connected for clarity. ........................................................................... 19
- Subscripted V_{BATU_LO} signal name in Active Battery Only Connected section. ................................................. 19
- Changed the description for Input Overvoltage Protection and Undervoltage Status Indication section for clarification. ........................................... 21
- Changed text in Battery Charging Process and Charge Profile section for clarity ........................................... 21
- Changed I_{PRETERM} and IPRE_TERMT names to iPRETERM in Termination and Pre-Charge Current Programming by External Components (IPRETERM) section for clarification ........................................... 22
- Changed terms in Equation 5 for clarification ........................................... 26
- Changed and added text in Status Indicators (PG and INT) section for clarification ........................................... 26
- Changed text in Buck (PWM) Output section. ................................................ 27
- Deleted “(TO BE TESTED)” from the COMMENT column of Table 8 ....... 28
- Changed first sentence of Manual Reset Timer and Reset Output (MR and RESET) description ........................................... 29
- Changed text in Manual Reset Timer and Reset Output (MR and RESET) section for clarification ........................................... 29
- Changed text in Modes and Functions for clarification ........................................... 30
- Changed text in Fault and Status Condition Responses for clarification ........................................... 31

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Revision History (continued)

- Changed text in Table 12. ................................................................................................................................................... 35
- Added text in Fast Charge Control Register description. .................................................................................................... 38
- Added Receiving Notification of Documentation Updates section. ...................................................................................... 63

Changes from Revision A (August 2015) to Revision B

<table>
<thead>
<tr>
<th>Change</th>
<th>Page</th>
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<tbody>
<tr>
<td>Added BQ25121 device to data sheet ...........................................</td>
<td>4</td>
</tr>
<tr>
<td>Added BQ25121 device to BATTERY-PACK NTC MONITOR specs in the Electrical Characteristics table .......................</td>
<td>11</td>
</tr>
<tr>
<td>Changed Figure 1 ............................................................................</td>
<td>14</td>
</tr>
<tr>
<td>Added Figure 14 typical characteristics graph .........................................</td>
<td>16</td>
</tr>
<tr>
<td>Changed text From: &quot;... current out of ISET is 1/400 (±10%)...&quot; To: &quot;...current out of ISET is 1/100 (±10%)...&quot; in Charge Current Programming by External Components (ISET) section. ...............................................</td>
<td>23</td>
</tr>
<tr>
<td>Added sentence “This bit is for testing and debug only and not intended to be used in the final system.” to the Buck (PWM) Output for clarification of the EN_SYS_OUT bit description. .........................................................</td>
<td>27</td>
</tr>
<tr>
<td>Added text to Bit B3 Description in Table 14 ..................................................</td>
<td>37</td>
</tr>
</tbody>
</table>

Changes from Original (August 2015) to Revision A

<table>
<thead>
<tr>
<th>Change</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Changed From: Product Preview To: Production data ..........................</td>
<td>1</td>
</tr>
</tbody>
</table>
5 Description (continued)

The battery is charged using a standard Li-Ion charge profile with three phases: precharge, constant current and constant voltage. A voltage-based JEITA compatible battery pack thermistor monitoring input (TS) is included that monitors battery temperature and automatically changes charge parameters to prevent the battery from charging outside of its safe temperature range. The charger is optimized for 5-V USB input, with 20-V tolerance to withstand line transients. The buck converter is run from the input or battery. When in battery only mode, the device can run from a battery up to 4.65 V.

A configurable load switch allows system optimization by disconnecting infrequently used devices. The manual reset with timer allows multiple different configuration options for wake are reset optimization. A simple voltage based monitor provides battery level information to the host in 2% increments from 60% to 100% of the programmed $V_{\text{BATREG}}$.

6 Device Comparison Table

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>VINDPM</th>
<th>DEFAULT SYS OUTPUT</th>
<th>DEFAULT LDO OUTPUT</th>
<th>DEFAULT VBERG</th>
<th>DEFAULT CHARGE CURRENT</th>
<th>DEFAULT TERMINATION CURRENT</th>
<th>DEFAULT SHIP MODE</th>
</tr>
</thead>
<tbody>
<tr>
<td>BQ25120</td>
<td>Enabled</td>
<td>1.8 V</td>
<td>Load Switch</td>
<td>4.2 V</td>
<td>10 mA</td>
<td>2 mA</td>
<td>Off</td>
</tr>
<tr>
<td>BQ25121</td>
<td>Enabled</td>
<td>2.5 V</td>
<td>Load Switch</td>
<td>4.2 V</td>
<td>10 mA</td>
<td>2 mA</td>
<td>Off</td>
</tr>
</tbody>
</table>
## 7 Pin Configuration and Functions

### Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN</td>
<td>A2</td>
<td>DC Input Power Supply. IN is connected to the external DC supply. Bypass IN to GND with at least 1 µF of capacitance using a ceramic capacitor.</td>
</tr>
<tr>
<td>PMID</td>
<td>A3, B3</td>
<td>High Side Bypass Connection. Connect at least 3µF of ceramic capacitance with DC bias derating from PMID to GND as close to the PMID and GND pins as possible.</td>
</tr>
<tr>
<td>GND</td>
<td>A1, D5</td>
<td>Ground connection. Connect to the ground plane of the circuit.</td>
</tr>
<tr>
<td>PGND</td>
<td>A5</td>
<td>Power ground connection. Connect to the ground plane of the circuit. Connect the output filter cap from the buck converter to this ground as shown in the layout example.</td>
</tr>
<tr>
<td>CD</td>
<td>E2</td>
<td>Chip Disable. Drive CD low to place the part in High-Z mode with battery only present, or enable charging when V\textsubscript{IN} is valid. Drive CD high for Active Battery mode when battery only is present, and disable charge when V\textsubscript{IN} is present. CD is pulled low internally with 900 kΩ.</td>
</tr>
<tr>
<td>SDA</td>
<td>E4</td>
<td>I²C Interface Data. Connect SDA to the logic rail through a 10-kΩ resistor.</td>
</tr>
<tr>
<td>SCL</td>
<td>E5</td>
<td>I²C Interface Clock. Connect SCL to the logic rail through a 10-kΩ resistor.</td>
</tr>
<tr>
<td>ILIM</td>
<td>C2</td>
<td>Adjustable Input Current Limit Programming. Connect a resistor from ILIM to GND to program the input current limit. The input current includes the system load and the battery charge current. Connect ILIM to GND to set the input current limit to the internal default threshold. ILIM can also be updated through I²C.</td>
</tr>
<tr>
<td>LSCTRL</td>
<td>E3</td>
<td>Load Switch and LDO Control Input. Pull high to enable the LS/LDO output, pull low to disable the LS/LDO output.</td>
</tr>
<tr>
<td>ISET</td>
<td>C1</td>
<td>Fast-Charge Current Programming Input. Connect a resistor from ISET to GND to program the fast-charge current level. Connect a resistor from ISET to GND to set the charge current to the internal default. ISET can also be updated through I²C. While charging, the voltage at ISET reflects the actual charging current and can be used to monitor charge current if an ISET resistor is present and the device is not in host mode.</td>
</tr>
<tr>
<td>IPRETERM</td>
<td>D1</td>
<td>Termination current programming input. Connect a 0-Ω to 10-kΩ resistor from IPRETERM to GND to program the termination current between 5% and 20% of the charge current. The pre-charge current is the same as the termination current setting. Connect IPRETERM to GND to set the termination current to the internal default threshold. IPRETERM can also be updated through I²C.</td>
</tr>
</tbody>
</table>
Pin Functions (continued)

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>INT</td>
<td>D2</td>
<td>O</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Status Output. INT is an open-drain output that signals charging status and fault interrupts. INT pulls low during charging. INT is high impedance when charging is complete, disabled, or the charger is in high impedance mode. When a fault occurs, a 128µs pulse is sent out as an interrupt for the host. INT charge indicator function is enabled/disabled using the EN_INT bit in the control register. Connect INT to a logic rail using an LED for visual indication of charge status or through a 100kΩ resistor to communicate with the host processor.</td>
</tr>
<tr>
<td>PG</td>
<td>D4</td>
<td>O</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Open-drain Power Good status indication output. PG pulls to GND when VIN is above V(BAT) + V(SLP) and less than V(OVP). PG is high-impedance when the input power is not within specified limits. Connect PG to the desired logic voltage rail using a 1kΩ to 100kΩ resistor, or use with an LED for visual indication. PG can also be configured as a push-button voltage shifted output (MRS) in the registers, where the output of the PG pin reflects the status of the MR input, but pulled up to the desired logic voltage rail using a 1kΩ to 100kΩ resistor.</td>
</tr>
<tr>
<td>RESET</td>
<td>D3</td>
<td>O</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Reset Output. RESET is an open drain active low output that goes low when MR is held low for longer than t(RESET), which is configurable by the MRRESET registers. RESET is deasserted after the t(RESET_D), typically 400ms.</td>
</tr>
<tr>
<td>MR</td>
<td>E1</td>
<td>I</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Manual Reset Input. MR is a push-button input that must be held low for greater than t(RESET) to assert the reset output. If MR is pressed for a shorter period, there are two programmable timer events, t(WAKE1) and t(WAKE2), that trigger an interrupt to the host. The MR input can also be used to bring the device out of Ship mode.</td>
</tr>
<tr>
<td>SW</td>
<td>A4</td>
<td>O</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Inductor Connection. Connect to the switched side of the external inductor.</td>
</tr>
<tr>
<td>SYS</td>
<td>B5</td>
<td>I</td>
</tr>
<tr>
<td></td>
<td></td>
<td>System Voltage Sense Connection. Connect SYS to the system output at the output bulk capacitors. Bypass SYS locally with at least 4.7 µF of effective ceramic capacitance.</td>
</tr>
<tr>
<td>LS/LDO</td>
<td>C5</td>
<td>O</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Load Switch or LDO output. Connect 1 µF of effective ceramic capacitance to this pin to assure stability. Be sure to account for capacitance bias voltage derating when selecting the capacitor.</td>
</tr>
<tr>
<td>VINLS</td>
<td>B4, C4</td>
<td>I</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Input to the Load Switch / LDO output. Connect 1 µF of effective ceramic capacitance from this pin to GND.</td>
</tr>
<tr>
<td>BAT</td>
<td>B1, B2</td>
<td>I/O</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Battery Connection. Connect to the positive terminal of the battery. Bypass BAT to GND with at least 1 µF of ceramic capacitance.</td>
</tr>
<tr>
<td>TS</td>
<td>C3</td>
<td>I</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Battery Pack NTC Monitor. Connect TS to the center tap of a resistor divider from VIN to GND. The NTC is connected from TS to GND. The TS function provides four thresholds for JEITA compatibility. TS faults are reported by the I²C interface during charge mode.</td>
</tr>
</tbody>
</table>
8 Specifications

8.1 Absolute Maximum Ratings
over operating free-air temperature range (unless otherwise noted) \(^{(1)}\)

<table>
<thead>
<tr>
<th>Input voltage</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN</td>
<td>–0.3</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>PMID, VINLS</td>
<td>–0.3</td>
<td>7.7</td>
<td>V</td>
</tr>
<tr>
<td>CDSDA, SCL, ILIM, ISET, IPRETERM, LSCTRL, INT, RESET, TS</td>
<td>–0.3</td>
<td>5.5</td>
<td>V</td>
</tr>
</tbody>
</table>

| Output voltage | SYS | 3.6 | V    |
| Input current  | IN  | 400 | mA   |
| Sink current   | INT | 10  | mA   |
| Sink/Source Current | RESET | 10 | mA   |
| Output Voltage Continuous | SW | –0.7| 7.7 | V    |
| Output Current Continuous | SW | 400 | mA   |
| Current        | LS/LDO | 150 | mA   |
| BAT Operating Voltage | VBAT, MR | 6.6 | V    |
| Junction Temperature | –40| 125 | °C   |
| Storage Temperature, T\(_{stg}\) | 300 | °C   |

\(^{(1)}\) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

<table>
<thead>
<tr>
<th>ESD</th>
<th>Electrostatic discharge</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V(_{ESD})</td>
<td>Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(^{(1)})</td>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Charged device model (CDM), per JEDEC specification JESD22-C101(^{(2)})</td>
<td>±500</td>
<td>V</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Any voltage greater than shown should be a transient event.  

\(^{(2)}\) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions
over operating free-air temperature range (unless otherwise noted)

| V\(_{IN}\) | IN voltage range | 3.4 | 5 | 20 | V |
| V\(_{BAT}\) | V\(_{BAT}\) operating voltage range | 3.4 | 5 | 5.5 | V |
| V\(_{VINLS}\) | V\(_{VINLS}\) voltage range for Load Switch | 0.8 | 5.5\(^{(2)}\) | V |
| V\(_{LDO}\) | V\(_{LDO}\) voltage range for LDO | 2.2 | 5.5 | V |
| I\(_{IN}\) | Input Current, IN input | 400 | mA |
| I\(_{SW}\) | Output Current from SW, DC | 300 | mA |
| I\(_{PMID}\) | Output Current from PMID, DC | 300 | mA |
| I\(_{LS/LDO}\) | Output Current from LS/LDO | 100 | mA |
| I\(_{BAT}\), I\(_{SYS}\) | Charging and discharging using internal battery FET | 300 | mA |
| T\(_{J}\) | Operating junction temperature range | –40 | 125 | °C |

\(^{(1)}\) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

\(^{(2)}\) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
8.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>bq2512x</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{JA} ) Junction-to-ambient thermal resistance</td>
<td>60</td>
<td>°C/W</td>
</tr>
<tr>
<td>( R_{JC(top)} ) Junction-to-case (top) thermal resistance</td>
<td>0.3</td>
<td>°C/W</td>
</tr>
<tr>
<td>( R_{JB} ) Junction-to-board thermal resistance</td>
<td>12.0</td>
<td>°C/W</td>
</tr>
<tr>
<td>( \psi_{JT} ) Junction-to-top characterization parameter</td>
<td>1.2</td>
<td>°C/W</td>
</tr>
<tr>
<td>( \psi_{JB} ) Junction-to-board characterization parameter</td>
<td>12.0</td>
<td>°C/W</td>
</tr>
<tr>
<td>( R_{JC(bot)} ) Junction-to-case (bottom) thermal resistance</td>
<td>N/A</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

\(^{(1)}\) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
8.5 Electrical Characteristics

Circuit of Figure 1, \( V_{\text{(UVLO)}} < V_{\text{IN}} < V_{\text{(OVP)}} \) and \( V_{\text{IN}} > V_{\text{(BAT)}} + V_{\text{(SLP)}} \), \( T_J = -40 \) to 85°C and \( T_J = 25°C \) for typical values (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETERS</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_N )</td>
<td>Supply Current for Control</td>
<td>( V_{\text{(UVLO)}} &lt; V_{\text{IN}} &lt; V_{\text{(OVP)}} ) and ( V_{\text{IN}} &gt; V_{\text{(BAT)}} + V_{\text{(SLP)}} ) PWM Switching, ( -40 &lt; T_J &lt; 85 ^\circ C )</td>
<td>1 mA</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( I_{\text{(BAT,HZ)}} )</td>
<td>Battery discharge current in High Impedance Mode</td>
<td>( V_{\text{(UVLO)}} &lt; V_{\text{IN}} &lt; V_{\text{(OVP)}} ) and ( V_{\text{IN}} &gt; V_{\text{(BAT)}} + V_{\text{(SLP)}} ) PWM Switching, ( -40 &lt; T_J &lt; 85 ^\circ C, V_{\text{IN}} = 5 ) V, Charge Disabled</td>
<td>1.5 mA</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( I_{\text{BAT_ACTIVE}} )</td>
<td>Battery discharge current in Active Battery Mode</td>
<td>( V_{\text{(UVLO)}} &lt; V_{\text{IN}} &lt; V_{\text{(OVP)}} ) and ( V_{\text{IN}} &gt; V_{\text{(BAT)}} + V_{\text{(SLP)}} ) PWM Switching, LSLDO enabled, ( 0°C &lt; T_J &lt; 85°C )</td>
<td>1.35 mA</td>
<td>4.25</td>
<td>mA</td>
</tr>
<tr>
<td>( I_{\text{BAT_ACTIVE}} )</td>
<td>Battery discharge current in Ship Mode</td>
<td>( V_{\text{(UVLO)}} &lt; V_{\text{IN}} &lt; V_{\text{(OVP)}} ) and ( V_{\text{IN}} &gt; V_{\text{(BAT)}} + V_{\text{(SLP)}} ) PWM Switching, LSLDO enabled, ( 0°C &lt; T_J &lt; 85°C )</td>
<td>1.35 mA</td>
<td>4.25</td>
<td>mA</td>
</tr>
</tbody>
</table>

**Power-Path Management and Input Current Limit**

| \( V_{\text{DO(IN,PMID)}} \) | \( V_{\text{IN}} - V_{\text{(PMID)}} \) | \( V_{\text{IN}} = 5 \) V, \( I_N = 300 \) mA | 125 | 170 | mA |
| \( V_{\text{DO(BAT-PMID)}} \) | \( V_{\text{(BAT)}} - V_{\text{(PMID)}} \) | \( V_{\text{IN}} = 0 \) V, \( V_{\text{(BAT)}} > 3 \) V, \( I_P = 400 \) mA | 120 | 160 | mA |
| \( V_{\text{(BSUP1)}} \) | Enter supplement mode threshold | \( V_{\text{(BAT)}} > V_{\text{(BUVLO)}} \) | \( V_{\text{(PMID)}} > V_{\text{(BAT)}} + 25 \) mV | V |
| \( V_{\text{(BSUP2)}} \) | Exit supplement mode threshold | \( V_{\text{(BAT)}} > V_{\text{(BUVLO)}} \) | \( V_{\text{(PMID)}} > V_{\text{(BAT)}} + 5 \) mV | V |
| \( I_{\text{BAT_OCP)}} \) | Current Limit, Discharge Mode | \( V_{\text{(BAT)}} > V_{\text{(BUVLO)}} \) | 0.85 | 1.15 | A |
| \( I_{\text{ILIM)}} \) | Input Current Limit | Programmable Range, 50-mA steps | 50 | 400 | mA |
| \( K_{\text{ILIM)}} \) | Maximum input current factor | \( I_{\text{ILIM}} = 50 \) mA to 100 mA | 175 | 200 | 225 | AΩ |
| \( K_{\text{ILIM)}} \) | Maximum input current factor | \( I_{\text{ILIM}} = 100 \) mA to 400 mA | 190 | 200 | 210 | AΩ |
| \( V_{\text{(IN,PMID)}} \) | Input voltage threshold when input current is reduced | Programmable Range using \( V_{\text{IN,PMID,ON}} \) Registers. Can be disabled using \( V_{\text{IN,PMID,OFF}} \) | 4.2 | 4.9 | V |
| \( V_{\text{(BUVLO)}} \) | Charge Voltage | Operating in voltage regulation, Programmable Range, 10mV steps | 3.6 | 4.65 | V |
| \( V_{\text{(BATREG)}} \) | Voltage Regulation Accuracy | \( T_J = 25°C \) | –0.5% | 0.5% | |
| \( V_{\text{(BATREG)}} \) | Voltage Regulation Accuracy | \( T_J = 0°C \) to 85°C | –0.5% | 0.5% | |

**BATTERY CHARGER**

| \( V_{\text{DO(PDM)}} \) | PMID voltage threshold when charge current is reduced | Above \( V_{\text{(BATREG)}} \) | 0.2 | | V |
| \( R_{\text{ON(BAT,PMID)}} \) | Internal Battery Charger MOSFET on-resistance | Measured from BAT to PMID, \( V_{\text{(BAT)}} = 4.35 \) V, High-Z mode | 300 | 400 | mA |
| \( V_{\text{(BATREG)}} \) | Charge Voltage | Operating in voltage regulation, Programmable Range, 10mV steps | 3.6 | 4.65 | V |

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Product Folder Links: BQ25120 BQ25121
Electrical Characteristics (continued)

Circuit of Figure 1, \( V_{\text{UVLO}} < V_{\text{IN}} < V_{\text{OVP}} \) and \( V_{\text{IN}} > V_{\text{BAT}} \) + \( V_{\text{SLP}} \), \( T_{J} = -40 \) to \( 85^\circ \text{C} \) and \( T_{J} = 25^\circ \text{C} \) for typical values (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETERS</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
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<tbody>
<tr>
<td>( I_{\text{CHARGE}} )</td>
<td>Fast Charge Current Range</td>
<td>( V_{\text{BATUVLO}} &lt; V_{\text{BAT}} &lt; V_{\text{BATREG}} )</td>
<td>5</td>
<td>300</td>
<td>mA</td>
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<tr>
<td></td>
<td>Fast Charge Current using ISET</td>
<td>( K_{\text{SET}} / R_{\text{SET}} )</td>
<td>A</td>
<td></td>
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<tr>
<td></td>
<td>Fast Charge Current Accuracy</td>
<td>-5%</td>
<td>5%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( K_{\text{SET}} )</td>
<td>Fast Charge Current Factor</td>
<td>5 mA &gt; ( I_{\text{CHARGE}} &gt; 300 ) mA</td>
<td>190</td>
<td>200</td>
<td>210</td>
</tr>
<tr>
<td>( I_{\text{TERM}} )</td>
<td>Termination charge current</td>
<td>Termination current programmable range over ( I_{\text{TH}} )</td>
<td>0.5</td>
<td>37</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>Termination Current using IPRETERM</td>
<td>( I_{\text{CHARGE}} &lt; 300 ) mA, ( R_{\text{TERM}} = 15 ) kΩ</td>
<td>5</td>
<td>% of ( I_{\text{SET}} )</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>( I_{\text{CHARGE}} &lt; 300 ) mA, ( R_{\text{TERM}} = 4.99 ) kΩ</td>
<td>10</td>
<td>% of ( I_{\text{SET}} )</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>( I_{\text{CHARGE}} &lt; 300 ) mA, ( R_{\text{TERM}} = 1.65 ) kΩ</td>
<td>15</td>
<td>% of ( I_{\text{SET}} )</td>
<td></td>
</tr>
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<td></td>
<td></td>
<td>( I_{\text{CHARGE}} &lt; 300 ) mA, ( R_{\text{TERM}} = 549 ) Ω</td>
<td>20</td>
<td>% of ( I_{\text{SET}} )</td>
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<td></td>
<td>Accuracy</td>
<td>( I_{\text{TERM}} &gt; 4 ) mA</td>
<td>-10%</td>
<td>10%</td>
<td></td>
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<tr>
<td>( I_{\text{PRE-CHARG}} )</td>
<td>Pre-charge current</td>
<td>Pre-charge current programmable range over ( I_{\text{TH}} )</td>
<td>0.5</td>
<td>37</td>
<td>mA</td>
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<tr>
<td></td>
<td>Accuracy</td>
<td>-10%</td>
<td>10%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{\text{RCH}} )</td>
<td>Recharge threshold voltage</td>
<td>Below ( V_{\text{BATREG}} )</td>
<td>100</td>
<td>120</td>
<td>140</td>
</tr>
<tr>
<td>( t_{\text{DGL(RCHG)}} )</td>
<td>Recharge threshold deglitch time</td>
<td>( t_{\text{FALL}} = 100 ) ns typ, ( V_{\text{RCH}} ) falling</td>
<td>32</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>( R_{\text{DS(ON_HS)}} )</td>
<td>PMID = 3.6 V, ( I_{\text{SYS}} = 50 ) mA</td>
<td>675</td>
<td>850</td>
<td>mΩ</td>
<td></td>
</tr>
<tr>
<td>( R_{\text{DS(ON_LS)}} )</td>
<td>PMID = 3.6 V, ( I_{\text{SYS}} = 50 ) mA</td>
<td>300</td>
<td>475</td>
<td>mΩ</td>
<td></td>
</tr>
<tr>
<td>( R_{\text{DS(CH_SYS)}} )</td>
<td>MOSFET on-resistance for SYS discharge</td>
<td>( V_{\text{IN}} = 3.6 ) V, ( I_{\text{OUT}} = -10 ) mA into ( V_{\text{OUT}} ) pin</td>
<td>22</td>
<td>40</td>
<td>Ω</td>
</tr>
<tr>
<td>( I_{\text{UMF}} )</td>
<td>SW Current limit HS</td>
<td>2.2 V &lt; ( V_{\text{PMID}} &lt; 5.5 ) V</td>
<td>525</td>
<td>600</td>
<td>675</td>
</tr>
<tr>
<td></td>
<td>SW Current limit LS</td>
<td>2.2 V &lt; ( V_{\text{PMID}} &lt; 5.5 ) V</td>
<td>525</td>
<td>700</td>
<td>850</td>
</tr>
<tr>
<td>( I_{\text{UM,SS}} )</td>
<td>PMOS switch current limit during softstart</td>
<td>Current limit is reduced during softstart</td>
<td>80</td>
<td>130</td>
<td>200</td>
</tr>
<tr>
<td>( V_{\text{SYS}} )</td>
<td>SYS Output Voltage Range</td>
<td>Programmable range, 100 mV Steps</td>
<td>1.1</td>
<td>3.3</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Output Voltage Accuracy</td>
<td>( V_{\text{IN}} = 5 ) V, PFM mode, ( I_{\text{OUT}} = 10 ) mA, ( V_{\text{SYS}} = 1.8 ) V</td>
<td>-2.5%</td>
<td>0</td>
<td>2.5%</td>
</tr>
<tr>
<td></td>
<td>DC Output Voltage Load Regulation in PWM mode</td>
<td>( V_{\text{OUT}} = 2 ) V, Load range</td>
<td>0.01</td>
<td>%/mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>DC Output Voltage Line Regulation in PWM mode</td>
<td>( V_{\text{OUT}} = 2 ) V, ( I_{\text{OUT}} = 100 ) mA, ( V_{\text{IN}} ) RANGE</td>
<td>0.01</td>
<td>%/V</td>
<td></td>
</tr>
<tr>
<td>( V_{\text{IN(LS)}} )</td>
<td>Input voltage range for LS/LDO</td>
<td>Load Switch Mode</td>
<td>0.8</td>
<td>6.6</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Input voltage range for LDO Mode</td>
<td>LDO Mode</td>
<td>2.2</td>
<td>6.6</td>
<td>V</td>
</tr>
<tr>
<td>( V_{\text{OUT}} )</td>
<td>DC output accuracy</td>
<td>( T_{J} = 25^\circ )C</td>
<td>-2%</td>
<td>±1%</td>
<td>2%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Over ( V_{\text{IN}}, I_{\text{OUT}} ); temperature</td>
<td>-3%</td>
<td>±2%</td>
<td>3%</td>
</tr>
<tr>
<td>( V_{\text{LODO}} )</td>
<td>Output range for LS/LDO</td>
<td>Programmable Range, 0.1 V steps</td>
<td>0.8</td>
<td>3.3</td>
<td>V</td>
</tr>
<tr>
<td>( \Delta V_{\text{OUT}} / \Delta V_{\text{IN}} )</td>
<td>DC Line regulation</td>
<td>( V_{\text{OUT}}(\text{Nom}) + 0.5 ) V &lt; ( V_{\text{IN}} &lt; 6.6 ) V, ( I_{\text{OUT}} = 5 ) mA</td>
<td>-1%</td>
<td>1%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>DC Load regulation</td>
<td>0 mA &lt; ( I_{\text{OUT}} &lt; 100 ) mA</td>
<td>-1%</td>
<td>1%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Load Transient</td>
<td>2 uA to 100 mA, ( V_{\text{OUT}} = 1.8 ) V</td>
<td>-120</td>
<td>60</td>
<td>mV</td>
</tr>
<tr>
<td>( R_{\text{DS(L channels, LDO)}} )</td>
<td>FET Rdson</td>
<td>( V_{\text{VIN(LS)}} = 3.6 ) V</td>
<td>460</td>
<td>600</td>
<td>mΩ</td>
</tr>
<tr>
<td>( R_{\text{DS(ON_LDO)}} )</td>
<td>MOSFET on-resistance for LS/LDO discharge</td>
<td>1.7 V &lt; ( V_{\text{VIN(LS)}} &lt; 6.6 ) V, ( I_{\text{LOAD}} = -10 ) mA</td>
<td>30</td>
<td>Ω</td>
<td></td>
</tr>
</tbody>
</table>
Electrical Characteristics (continued)

Circuit of Figure 1, \( V_{(UVLO)} < V_{IN} < V_{(OVP)} \) and \( V_{IN} > V_{(BAT)} + V_{(SLP)} \), \( T_J = -40 \) to \( 85^\circ C \) and \( T_J = 25^\circ C \) for typical values (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETERS</th>
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<th>MIN</th>
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<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{(OCL_LDO)} )</td>
<td>Output Current Limit – LDO</td>
<td>( V_{LS_LDO} = 0.9 \times V_{LS_LDO_NOM} )</td>
<td>275</td>
<td>365</td>
<td>450</td>
</tr>
<tr>
<td>( I_{(SL_LDO)} )</td>
<td>Output Current</td>
<td>( V_{(VINLS)} = 3.6 \ V, \ V_{SL_LDO} = 3.3 \ V )</td>
<td>100</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{(VINLS)} = 3.3 \ V, \ V_{SL_LDO} = 0.8 \ V )</td>
<td>100</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{(VINLS)} = 2.2 \ V, \ V_{SL_LDO} = 0.8 \ V )</td>
<td>10</td>
<td></td>
<td></td>
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<tr>
<td>( I_{(N_LDO)} )</td>
<td>Quiescent current for ( VINLS ) in LDO mode</td>
<td></td>
<td></td>
<td>0.9</td>
<td>( \mu A )</td>
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<tr>
<td></td>
<td>OFF-state supply current</td>
<td></td>
<td></td>
<td>0.25</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( V_{(H_LSCTRL)} )</td>
<td>High-level input voltage for LSCTRL</td>
<td>( 1.15 \ V &gt; V_{(VINLS)} &gt; 6.6 \ V )</td>
<td>( 0.75 \times V_{(SYS)} )</td>
<td>6.6</td>
<td>V</td>
</tr>
<tr>
<td>( V_{(L_LSCTRL)} )</td>
<td>Low-level input voltage for LSCTRL</td>
<td>( 1.15 \ V &gt; V_{(VINLS)} &gt; 6.6 \ V )</td>
<td>( 0.25 \times V_{(SYS)} )</td>
<td></td>
<td>V</td>
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**PUSHBUTTON TIMER** (MR)

<table>
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<tr>
<th>PARAMETERS</th>
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<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
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<tbody>
<tr>
<td>( V_N )</td>
<td>Low-level input voltage</td>
<td></td>
<td></td>
<td>0.3</td>
<td>( V )</td>
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<tr>
<td>( R_{PU} )</td>
<td>Internal pull-up resistance</td>
<td></td>
<td></td>
<td>120</td>
<td>( k\Omega )</td>
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**VBAT MONITOR**

<table>
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<tr>
<th>PARAMETERS</th>
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<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
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<tbody>
<tr>
<td>( V_{BMON} )</td>
<td>Battery Voltage Monitor Accuracy</td>
<td>( V_{BAT} ) falling - Including 2% increment</td>
<td>( -3.5 )</td>
<td>3.5</td>
<td>( %V_{(BATREG)} )</td>
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</tbody>
</table>

**BATTERY-PACK NTC MONITOR**

<table>
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<tr>
<th>PARAMETERS</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
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</thead>
<tbody>
<tr>
<td>( V_{(HOT)} )</td>
<td>High temperature threshold</td>
<td>( V_{TS} ) falling, 1% ( V_{IN} ) Hysteresis</td>
<td>bq25120</td>
<td>14.5</td>
<td>15</td>
</tr>
<tr>
<td>( V_{(WARM)} )</td>
<td>Warm temperature threshold</td>
<td>( V_{TS} ) falling, 1% ( V_{IN} ) Hysteresis</td>
<td>bq25120</td>
<td>20.1</td>
<td>20.5</td>
</tr>
<tr>
<td>( V_{(COOL)} )</td>
<td>Cool temperature threshold</td>
<td>( V_{TS} ) rising, 1% ( V_{IN} ) Hysteresis</td>
<td>bq25120</td>
<td>35.4</td>
<td>36</td>
</tr>
<tr>
<td>( V_{(COLD)} )</td>
<td>Low temperature threshold</td>
<td>( V_{TS} ) rising, 1% ( V_{IN} ) Hysteresis</td>
<td>bq25120</td>
<td>39.3</td>
<td>39.8</td>
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<td>bq25121</td>
<td>39.5</td>
<td>40</td>
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<tr>
<td>( TS_{OFF} )</td>
<td>TS Disable threshold</td>
<td>( V_{TS} ) rising, 2% ( V_{IN} ) Hysteresis</td>
<td>bq25120</td>
<td>55</td>
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<td></td>
<td>bq25121</td>
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<tr>
<td>( T_{SHUTDOWN} )</td>
<td>Thermal trip</td>
<td>( V_{IN} &gt; V_{(UVLO)} )</td>
<td></td>
<td>114</td>
<td></td>
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<tr>
<td>( T_{HYS} )</td>
<td>Thermal hysteresis</td>
<td>( V_{IN} &gt; V_{(UVLO)} )</td>
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</table>

**PROTECTION**

<table>
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<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
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<tbody>
<tr>
<td>( V_{(UVLO)} )</td>
<td>IC active threshold voltage</td>
<td>( V_{IN} ) rising</td>
<td>3.4</td>
<td>3.6</td>
<td>3.8</td>
</tr>
<tr>
<td>( V_{(UVLO_HYB)} )</td>
<td>IC active hysteresis</td>
<td>( V_{IN} ) falling from above ( V_{(UVLO)} )</td>
<td></td>
<td>150</td>
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</tr>
<tr>
<td>( V_{(BV_LO)} )</td>
<td>Battery Undervoltage Lockout threshold Range</td>
<td>Programmable Range for ( V_{(BV_LO)} ) ( V_{BAT} ) falling, 200 mV Hysteresis</td>
<td>bq25120</td>
<td>2.2</td>
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<td></td>
<td>bq25121</td>
<td>3.0</td>
<td></td>
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<td></td>
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<td></td>
<td>Default Battery Undervoltage Lockout Accuracy</td>
<td>( V_{BAT} ) falling</td>
<td>( -2.5% )</td>
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<tr>
<td>( V_{(BAT_SHORT)} )</td>
<td>Battery short circuit threshold</td>
<td>Battery voltage falling</td>
<td></td>
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<tr>
<td>( V_{(BAT_SHORT_HYB)} )</td>
<td>Hysteresis for ( V_{(BAT_SHORT)} )</td>
<td></td>
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<td>100</td>
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<tr>
<td>( I_{(BAT_SHORT)} )</td>
<td>Battery short circuit charge current</td>
<td>( I_{(PRETERM)} )</td>
<td></td>
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<td></td>
</tr>
<tr>
<td>( V_{(SLP)} )</td>
<td>Sleep entry threshold, ( V_{IN} &lt; V_{(BAT)} )</td>
<td>( 2 \ V &lt; V_{BAT} &lt; V_{(BATREG)} )</td>
<td>( V_{IN} ) falling</td>
<td>65</td>
<td>120</td>
</tr>
<tr>
<td>( V_{(SLP_HYB)} )</td>
<td>Sleep-mode exit hysteresis</td>
<td>( V_{IN} ) rising above ( V_{(SLP)} )</td>
<td>40</td>
<td>65</td>
<td>100</td>
</tr>
<tr>
<td>( V_{(OVP)} )</td>
<td>Maximum Input Supply OVP threshold voltage</td>
<td>( V_{IN} ) rising, 100 mV hysteresis</td>
<td>5.35</td>
<td>5.55</td>
<td>5.75</td>
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<tr>
<td>( t_{DGL_OVP} )</td>
<td>Deglitch time, ( VIN ) OVP falling</td>
<td>( V_{IN} ) falling below ( V_{(OVP)} ), 1V/us</td>
<td>32</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( T_{SHUTDOWN} )</td>
<td>Thermal trip</td>
<td>( V_{IN} &gt; V_{(UVLO)} )</td>
<td></td>
<td>114</td>
<td></td>
</tr>
<tr>
<td>( T_{HYS} )</td>
<td>Thermal hysteresis</td>
<td>( V_{IN} &gt; V_{(UVLO)} )</td>
<td></td>
<td>11</td>
<td></td>
</tr>
</tbody>
</table>
Electrical Characteristics (continued)

Circuit of Figure 1, $V_{(UVLO)} < V_{IN} < V_{(OVP)}$ and $V_{IN} > V_{(BAT)} + V_{(SLP)}$, $T_J = -40$ to 85°C and $T_J = 25°C$ for typical values (unless otherwise noted)

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<tr>
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</thead>
<tbody>
<tr>
<td>$t_{DGL_SHUTDOWN}$</td>
<td>Deglitch time, Thermal shutdown</td>
<td>$T_J$ rising above $T_{SHUTDOWN}$</td>
<td>4</td>
<td></td>
<td>$\mu s$</td>
</tr>
</tbody>
</table>

I2C INTERFACE

<table>
<thead>
<tr>
<th>$V_{IL}$</th>
<th>Input low threshold level</th>
<th>$V_{PULLUP} = 1.1 \text{ V, SDA and SCL}$</th>
<th></th>
<th></th>
<th>V</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>Input high threshold level</td>
<td>$V_{PULLUP} = 1.1 \text{ V, SDA and SCL}$</td>
<td>0.825</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output low threshold level</td>
<td>$IL = 5m\text{A}$, sink current, $V_{PULLUP} = 1.1 \text{ V}$</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{BIAS}$</td>
<td>High-Level leakage current</td>
<td>$V_{PULLUP} = 1.8\text{ V, SDA and SCL}$</td>
<td>0.275</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

INT, PG, and RESET OUTPUT (Open Drain)

<table>
<thead>
<tr>
<th>$V_{OL}$</th>
<th>Low level output threshold</th>
<th>Sinking current = 5 mA</th>
<th></th>
<th></th>
<th>V</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{IN}$</td>
<td>Bias current into pin</td>
<td>Pin is high impedance, $I_{OUT} = 0 \text{ mA}$; $T_J = -40°C$ to 60°C</td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>$V_{IN_BAT_DELTA}$</td>
<td>Input voltage above $V_{BAT}$ where PG sends two 128 $\mu s$ pulses each minute to signal the host of the input voltage status</td>
<td>$V_{UVLO} &lt; V_{IN} &lt; V_{OVP}$</td>
<td>0.825</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

INPUT PIN (CD LSCTRL)

<table>
<thead>
<tr>
<th>$V_{IL_CD_LSCTRL}$</th>
<th>Input low threshold</th>
<th>$V_{PULLUP} = 1 \text{ V}$</th>
<th></th>
<th></th>
<th>V</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH_CD_LSCTRL}$</td>
<td>Input high threshold</td>
<td>$V_{PULLUP} = 1 \text{ V}$</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$R_{PULLDOWN_CD}$</td>
<td>Internal pull-down resistance</td>
<td></td>
<td>900</td>
<td></td>
<td>k$\Omega$</td>
</tr>
<tr>
<td>$R_{LSCTRL}$</td>
<td>Internal pull-down resistance</td>
<td></td>
<td>2</td>
<td></td>
<td>M$\Omega$</td>
</tr>
</tbody>
</table>
### 8.6 Timing Requirements

<table>
<thead>
<tr>
<th><strong>POWER-PATH MANAGEMENT AND INPUT CURRENT LIMIT</strong></th>
<th><strong>MIN</strong></th>
<th><strong>TYP</strong></th>
<th><strong>MAX</strong></th>
<th><strong>UNIT</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>t\textsuperscript{DGL_SC} Deglitch Time, PMID or SW Short Circuit during Discharge Mode</td>
<td>250</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>t\textsuperscript{REC_SC} Recovery time, OUT Short Circuit during Discharge Mode</td>
<td>2</td>
<td></td>
<td></td>
<td>s</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>BATTERY CHARGER</strong></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>t\textsuperscript{DGL_SHORT} Deglitch time transition from ISET short to I\textsubscript{CHARGE} disable</td>
<td>1 ms</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>BATTERY CHARGING TIMERS</strong></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>t\textsuperscript{MAXCHG} Charge safety timer</td>
<td>Programmable range</td>
</tr>
<tr>
<td>t\textsuperscript{PRECHG} Precharge safety timer</td>
<td>0.1 x t\textsuperscript{MAXCHG}</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>SYS OUTPUT</strong></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>t\textsuperscript{ONMIN} Minimum ON time</td>
<td>V\textsubscript{IN} = 3.6 V, V\textsubscript{OUT} = 2 V, I\textsubscript{OUT} = 0 mA</td>
</tr>
<tr>
<td>t\textsuperscript{OFFMIN} Minimum OFF time</td>
<td>V\textsubscript{IN} = 4.2 V</td>
</tr>
<tr>
<td>t\textsuperscript{START_SW} SW start up time</td>
<td>V\textsubscript{IN} = 5 V, from write on EN\textsubscript{SW_OUT} until output starts to rise</td>
</tr>
<tr>
<td>t\textsuperscript{START_SYS} SYS output time to start switching</td>
<td>From insertion of BAT &gt; V\textsubscript{BUVLO} or V\textsubscript{IN} &gt; V\textsubscript{UVLO}</td>
</tr>
<tr>
<td>t\textsuperscript{SOFTSTART} Softstart time with reduced current limit</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>LS/LDO OUTPUT</strong></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>t\textsuperscript{ON_LDO} Turn ON time</td>
<td>100 mA load</td>
</tr>
<tr>
<td>t\textsuperscript{OFF_LDO} Turn OFF time</td>
<td>100 mA load</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>PUSHBUTTON TIMER</strong></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>t\textsuperscript{WAKE1} Push button timer wake 1</td>
<td>Programmable Range for wake1 function</td>
</tr>
<tr>
<td>t\textsuperscript{WAKE2} Push button timer wake 2</td>
<td>Programmable Range for wake2 function</td>
</tr>
<tr>
<td>t\textsuperscript{RESET} Push button timer reset</td>
<td>Programmable Range for reset function</td>
</tr>
<tr>
<td>t\textsuperscript{RESET_D} Reset pulse duration</td>
<td></td>
</tr>
<tr>
<td>t\textsuperscript{DD} Detection delay (from MR, input to RESET)</td>
<td>For 0s condition</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>BATTERY-PACK NTC MONITOR</strong></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>t\textsuperscript{DGL(TS)} Deglitch time on TS change</td>
<td>Applies to V\textsubscript{(HOT)}, V\textsubscript{(WARM)}, V\textsubscript{(COOL)}, and V\textsubscript{(COLD)}</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>I2C INTERFACE</strong></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>t\textsuperscript{WATCHDOG} I2C interface reset timer for host</td>
<td></td>
</tr>
<tr>
<td>t\textsuperscript{I2CRESET} I2C interface inactive reset timer</td>
<td></td>
</tr>
<tr>
<td>t\textsuperscript{I2C_ACTIVEBAT} Transition time required to enable the I2C interface from HiZ to Active BAT</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>INPUT PIN</strong></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>t\textsuperscript{CD_DGL} Deglitch for CD</td>
<td>CD rising/falling</td>
</tr>
</tbody>
</table>
After delay of several ms, switching starts and SYS starts to rise.
Charging enabled.

VBAT rises.

IBAT = ICHRG

VBAT = \( V_{BATREG} \)

No SYS Load

SYS Load Applied

Conditions: PGB_MRS = 0, TE = 1, SW_LDO = 1, VINDPM_ON = 0, PG and INT pulled up to SYS, EN_INT = 1

Figure 1. Typical Start-Up Timing and Operation
Device enters Active Battery Mode after valid /MR

Figure 2. Battery Operation and Sleep Mode

Conditions: SW_LDO = 1, MRREC = 1, PG and INT pulled up to SYS, ISYS = 10 µA, EN_INT = 1
8.7 Typical Characteristics

Figure 3. Active BAT, I_Q

Figure 4. Hi-Z BAT, I_Q

Figure 5. Ship Mode BAT, I_Q

Figure 6. Blocking FET R_DS(ON) vs Temperature

Figure 7. Battery Discharge FET R_DS(ON) vs Temperature

Figure 8. V_{BATREG} Accuracy vs Temperature
Typical Characteristics (continued)

![Figure 9. ILIM Accuracy vs Input Current](image)
![Figure 10. Charge Current Accuracy vs Charge Current](image)

![Figure 11. Pre-Charge Accuracy vs Pre-Charge Current](image)

![Figure 12. R_DS(ON) of High Side MOSFET vs Temperature](image)

![Figure 13. R_DS(ON) of Low Side MOSFET vs Temperature](image)

![Figure 14. LS/LDO PSRR vs Frequency](image)
9 Detailed Description

9.1 Overview
The following sections describe in detail the functions provided by the BQ25120. These include linear charger, PWM output, configurable LS/LDO output, Push-button input, reset timer, functional modes, battery monitor, I^2C configurability and functions, and safety features.

9.2 Functional Block Diagram
9.3 Feature Description

9.3.1 Ship Mode

Ship Mode is the lowest quiescent current state for the device. Ship Mode latches off the device and BAT FET until $V_{IN} > V_{UVLO}$ or the MR button is depressed for $t_{WAKE}$ and released. To enter Ship Mode, CD must be pulled high. If the EN_SHIPMODE is written to a 1 while the input is connected, it must first be removed to enter ship mode. This allows the end product with minimal load on the battery, and the end user can enable the device by plugging it into the adapter or by toggling the MR button. The battery voltage must be above the maximum programmable BUVLO threshold in order to exit Ship mode with a MR button press when $V_{IN}$ is not present. The EN_SHIPMODE bit can be cleared using the I2C interface as well while the input is valid. The following list shows the events that are active during Ship Mode:

1. VIN_UV Comparator
2. MR Input (No clock or delay in this mode for lowest power consumption)

9.3.2 High Impedance Mode

High Impedance mode is the lowest quiescent current state while operating from the battery. During Hi-Z mode the SYS output is powered by BAT, the MR input is active, and the LSCTRL input is active. All other circuits are in a low power or sleep state. The LS/LDO output can be enabled in Hi-Z mode with the LSCTRL input. If the LS/LDO output has been enabled through I2C prior to entering Hi-Z mode, it will stay enabled. The CD pin is used to put the device in a high-impedance mode when battery is present and $V_{IN} < V_{UVLO}$. Drive CD high to enable the device and enter active battery operation when $V_{IN}$ is not valid. When the HZ_MODE bit is written by the host, the I2C interface is disabled if only battery is present. To resume I2C, the CD pin must be toggled. The functionality is shown in Table 1.

<table>
<thead>
<tr>
<th>CD, State</th>
<th>$V_{IN} &lt; V_{UVLO}$</th>
<th>$V_{IN} &gt; V_{UVLO}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>Hi-Z</td>
<td>Charge Enabled</td>
</tr>
<tr>
<td>H</td>
<td>Active Battery</td>
<td>Charge Disabled</td>
</tr>
</tbody>
</table>

9.3.3 Active Battery Only Connected

When the battery above $V_{BATUVLO}$ is connected with no input source, the battery discharge FET is turned on. After the battery rises above $V_{BATUVLO}$ and the deglitch time is reached, the SYS output starts to rise. The current from PMID and SYS is not regulated, but is protected by a short circuit current limit. If the short circuit limit is reached for the deglitch time ($t_{DGL_SC}$), the battery discharge FET is turned off for the recovery time ($t_{REC_SC}$). After the recovery time, the battery FET is turned on to test if the short has been removed. If it has not, the FET turns off and the process repeats until the short is removed. This process protects the internal FET from over current. During this event PMID will likely droop and cause SYS to go out of regulation.

To provide designers the most flexibility in optimizing their system, an adjustable BATUVLO is provided. When the voltage drops below the $V_{BATUVLO}$ threshold, the battery discharge FET is turned off. Deeper discharge of the battery enables longer times between charging, but may shorten the battery life. The BATUVLO is adjustable with a fixed 100-mV hysteresis.

If a valid $V_{IN}$ is connected during active battery mode, $V_{IN} > V_{UVLO}$, the supplement and battery discharge FET is turned on when the battery voltage is above the minimum $V_{BATUVLO}$.

Drive CD high or write the CE register to disable charge when $V_{IN} > V_{UVLO}$ is present. CD is internally pulled down. When exiting this mode, charging resumes if $V_{IN}$ is present, CD is low and charging is enabled.

All HOST interfaces (CD, SDA/SCL, INT, RESET and LSCTRL) are active no later than 5 ms after SYS reaches the programmed level.
9.3.4 Voltage Based Battery Monitor

The device implements a simple voltage battery monitor which can be used to determine the depth of discharge. Prior to entering High-Z mode, the device will initiate a VBMON reading. The host can read the latched value for the no-load battery voltage, or initiate a reading using VBMON_READ to see the battery voltage under a known load. The register will be updated and can be read 2ms after a read is initiated. The VBMON voltage threshold is readable with 2% increments with ±1.5% accuracy between 60% and 100% of VBATREG using the VBMON_TH registers. Reading the value during charge is possible, but for the most accurate battery voltage indication, it is recommended to disable charge, initiate a read, and then re-enable charge.

A typical discharge profile for a Li-Ion battery is shown in Table 2. The specific battery to be used in the application should be fully characterized to determine the thresholds that will indicate the appropriate battery status to the user. Two typical examples are shown below, assuming the VBMON reading is taken with no load on the battery.

This function enables a simple 5-bar status indicator with the following typical performance with different VBATREG settings:

<table>
<thead>
<tr>
<th>VBATREG</th>
<th>BATTERY FULL</th>
<th>95% to 65% REMAINING CAPACITY</th>
<th>65% to 35% REMAINING CAPACITY</th>
<th>35% to 5% REMAINING CAPACITY</th>
<th>BATTERY EMPTY</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.35 V</td>
<td>VBMON &gt; 90%</td>
<td>VBMON = 88%</td>
<td>VBMON = 86%</td>
<td>VBMON = 84%</td>
<td>VBMON &lt; 82%</td>
</tr>
<tr>
<td>4.2 V</td>
<td>VBMON &gt; 98%</td>
<td>VBMON = 94% or 96%</td>
<td>VBMON = 90% or 92%</td>
<td>VBMON = 86% or 88%</td>
<td>VBMON &lt; 84%</td>
</tr>
</tbody>
</table>

![Figure 15. Voltage Battery Monitor](image-url)
9.3.5 Sleep Mode

The device enters the low-power sleep mode if the voltage \( V_{IN} \) falls below the sleep-mode entry threshold and \( V_{IN} \) is higher than the undervoltage lockout threshold. In sleep mode, the input is isolated from the battery. This feature prevents draining the battery during the absence of \( V_{IN} \). When \( V_{IN} < V_{(BAT)} + V_{SLP} \), the device turns the battery discharge FET on, sends a 128-µs pulse on the INT output, and the FAULT bits of the register are updated over \( I^2C \). Once \( V_{IN} > V_{(BAT)} + V_{SLP} \), the device initiates a new charge cycle. The FAULT bits are not cleared until they are read over \( I^2C \) and the sleep condition no longer exists.

9.3.6 Input Voltage Based Dynamic Power Management (\( V_{IN(DPM)} \))

During the normal charging process, if the input power source is not able to support the programmed or default charging current and System load, the supply voltage decreases. Once the supply drops to \( V_{IN(DPM)} \), the input DPM current and voltage loops will reduce the input current through the blocking FETs, to prevent the further drop of the supply. The \( V_{IN(DPM)} \) threshold is programmable through the \( I^2C \) register from 4.2 V to 4.9 V in 100-mV steps. It can be disabled completely as well. When the device enters this mode, the charge current may be lower than the set value and the \( V_{INDPM} \) STAT bit is set. If the 2X timer is set, the safety timer is extended while \( V_{IN(DPM)} \) is active. Additionally, termination is disabled.

9.3.7 Input Overvoltage Protection and Undervoltage Status Indication

The input overvoltage protection protects the device and downstream components connected to PMID, SYS, and BAT against damage from overvoltage on the input supply. When \( V_{IN} > V_{OVP} \) an OVP fault is determined to exist. During the OVP fault, the device turns the battery discharge FET on, sends a single 128-µs pulse on INT, and the FAULT bits are updated over \( I^2C \). Once the OVP fault is removed, after the deglitch time, \( t_{DGL_OVP} \), STAT and FAULT bits are cleared and the device returns to normal operation. The FAULT bits are not cleared until they are read in from \( I^2C \) after the OVP condition no longer exists. The OVP threshold for the device is set to operate from standard USB sources.

The input under-voltage status indication is used to notify the host or other device when the input voltage falls below a desired threshold. When \( V_{IN} < V_{UVLO} \), after the deglitch time \( t_{DGL_UVLO} \), a UVLO fault is determined to exist. During the \( V_{IN} \) UVLO fault, the device sends a single 128-µs pulse on INT, and the STAT and FAULT bits are updated over \( I^2C \). The FAULT bits are not cleared until they are read in from \( I^2C \) after the UVLO condition no longer exists.

9.3.8 Battery Charging Process and Charge Profile

When a valid input source is connected (\( V_{IN} > V_{UVLO} \) and \( V_{(BAT)} + V_{SLP} < V_{IN} < V_{OVP} \)), the CE bit in the control register determines whether a charge cycle is initiated. When the CE bit is 1 and a valid input source is connected, the battery discharge FET is turned off, and the output at SYS is regulated depending on the output configuration. A charge cycle is initiated when the CE bit is written to a 0. Alternatively, the CD input can be used to enable and disable charge.

The device supports multiple battery chemistries for single-cell applications. Charging is done through the internal battery MOSFET. There are several loops that influence the charge current: constant current loop (CC), constant voltage loop (CV), input current limit, \( V_{DPPM} \), and \( V_{IN(DPM)} \). During the charging process, all loops are enabled and the one that is dominant takes control.

The charge current is regulated to \( I_{CHARGE} \) until the voltage between BAT and GND reaches the regulation voltage. The voltage between BAT and GND is regulated to \( V_{BATREG} \) (CV Mode) while the charge current naturally tapers down. When termination is enabled, the device monitors the charging current during the CV mode, and once the charge current tapers down to the termination threshold, \( I_{TERM} \), and the battery voltage is above the recharge threshold, the device terminates charge, and turns off the battery charging FET. Termination is disabled when any loop is active other than CV.
9.3.9 Dynamic Power Path Management Mode

With a valid input source connected, the power-path management circuitry monitors the input voltage and current continuously. The current into IN is shared at PMID between charging the battery and powering the system load at PMID, SYS, and LS/LDO. If the sum of the charging and load currents exceeds the preset maximum input current, the input DPM loop reduces input current. If PMID drops below the DPPM voltage threshold, the charging current is reduced by the DPPM loop through the BATFET. If PMID continues to drop after BATFET charging current is reduced to zero, the part enters supplement mode when PMID falls below the supplement mode threshold. Battery termination is disabled while in DPPM mode.

9.3.10 Battery Supplement Mode

While in DPPM mode, if the charging current falls to zero and the system load current increases beyond the programmed input current limit, the voltage at PMID reduces further. When the PMID voltage drops below the battery voltage by $V_{(BSUP1)}$, the battery supplements the system load. The battery stops supplementing the system load when the voltage on the PMID pin rises above the battery voltage by $V_{(BSUP2)}$. During supplement mode, the battery supplement current is not regulated, however, the short-circuit protection circuit is active. Battery termination is disabled while in supplement mode.

9.3.11 Default Mode

The default mode is used when there is no host, or $I^C$ communication is not available. If the externally programmable pins, ILIM, ISET, and ITERM have resistors connected, that is considered the default mode. If they are tied to GND, the default register settings are used. The default mode can be entered by connecting a valid power source to $V_{IN}$ or the RESET bit is written. Default mode is exited by writing to the $I^C$ interface.

9.3.12 Termination and Pre-Charge Current Programming by External Components (IPRETERM)

The termination current threshold is user programmable through an external resistor or through registers over $I^C$. Set the termination current using the IPRETERM pin by connecting a resistor from IPRETERM to GND. The termination can be set between 5% and 20% of the programmed output current set by ISET, using Table 3 for guidance:

<table>
<thead>
<tr>
<th>IPRE CHARGE and ITERM</th>
<th>KKIIPRETERM</th>
<th>RIPRETERM (STANDARD 1% VALUES)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>MIN</td>
<td>TYP (% of ISET)</td>
<td>MAX</td>
<td>MIN</td>
</tr>
<tr>
<td>5</td>
<td>180</td>
<td>200</td>
<td>220</td>
</tr>
<tr>
<td>10</td>
<td>180</td>
<td>200</td>
<td>220</td>
</tr>
<tr>
<td>15</td>
<td>180</td>
<td>200</td>
<td>220</td>
</tr>
<tr>
<td>20</td>
<td>180</td>
<td>200</td>
<td>220</td>
</tr>
</tbody>
</table>

Using the $I^C$ register, the termination current can be programmed with a minimum of 500 µA and a maximum of 37 mA.

The pre-charge current is not independently programmable through the external resistor, and is set at the termination current. The pre-charge and termination currents are programmable using the IPRETERM registers. If no IPRETERM resistor is connected and the pin is tied to GND, the default values in the IPRETERM registers are used. The external value can be used in host mode by configuring the IPRETERM registers. If the external ICHG setting will be used after being in Host mode, the IPRETERM registers should be set to match the desired external threshold for the highest ICHG accuracy.

Termination is disabled when any loop other than CV is active.
9.3.13 Input Current Limit Programming by External Components (ILIM)

The input current limit threshold is user programmable through an external resistor or through registers over I²C. Set the input current limit using the ILIM pin by connecting a resistor from ILIM to GND using Table 4 for guidance. If no ILIM resistor is connected and the pin is tied to GND, the default ILIM register value is used. The external value is not valid once the device enters host mode.

Table 4. ILIM Resistor Settings

<table>
<thead>
<tr>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>KILIM</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>RILIM (STANDARD 1% VALUES)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.048469388</td>
<td>0.051020408</td>
<td>0.053571429</td>
<td>190</td>
<td>200</td>
<td>210</td>
<td>3920</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>0.09047619</td>
<td>0.095238695</td>
<td>0.1</td>
<td>190</td>
<td>200</td>
<td>210</td>
<td>2100</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>0.146153846</td>
<td>0.153846154</td>
<td>0.161538462</td>
<td>190</td>
<td>200</td>
<td>210</td>
<td>1300</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>0.19</td>
<td>0.2</td>
<td>0.21</td>
<td>190</td>
<td>200</td>
<td>210</td>
<td>1000</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>0.285714286</td>
<td>0.30075188</td>
<td>0.315789474</td>
<td>190</td>
<td>200</td>
<td>210</td>
<td>665</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>0.380761523</td>
<td>0.400801603</td>
<td>0.420841683</td>
<td>190</td>
<td>200</td>
<td>210</td>
<td>499</td>
<td>Ω</td>
<td></td>
</tr>
</tbody>
</table>

The device has register programmable input current limits from 50 mA to 400 mA in 50-mA steps. The device is USB-IF compliant for inrush current testing, assuming that the input capacitance to the device is selected to be small enough to prevent a violation (<10 µF), as this current is not limited.

9.3.14 Charge Current Programming by External Components (ISET)

The fast charge current is user programmable through an external resistor or through registers over I²C. Set the fast charge current by connecting a resistor from ISET to GND. If no ISET resistor is connected and the pin is tied to GND, the default ISET register value is used. While charging, if the charge current is using the externally programmed value, the voltage at ISET reflects the actual charging current and can be used to monitor charge current. The current out of ISET is 1/100 (±10%) of the charge current. The charge current can be calculated by using Table 5 for guidance:

Table 5. ISET Resistor Settings

<table>
<thead>
<tr>
<th>ISET</th>
<th>KISET</th>
<th>RISET (STANDARD 1% VALUES)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>MIN</td>
<td>TYP</td>
<td>MAX</td>
<td></td>
</tr>
<tr>
<td>0.285714286</td>
<td>0.30075188</td>
<td>0.315789474</td>
<td>190</td>
</tr>
<tr>
<td>0.19</td>
<td>0.2</td>
<td>0.21</td>
<td>190</td>
</tr>
<tr>
<td>0.126666667</td>
<td>0.133333333</td>
<td>0.14</td>
<td>190</td>
</tr>
<tr>
<td>0.095</td>
<td>0.1</td>
<td>0.105</td>
<td>190</td>
</tr>
<tr>
<td>0.06462585</td>
<td>0.068027211</td>
<td>0.071428571</td>
<td>190</td>
</tr>
<tr>
<td>0.048469388</td>
<td>0.051020408</td>
<td>0.053571429</td>
<td>190</td>
</tr>
<tr>
<td>0.031456954</td>
<td>0.033112583</td>
<td>0.034768212</td>
<td>190</td>
</tr>
<tr>
<td>0.025956284</td>
<td>0.027322404</td>
<td>0.028888525</td>
<td>190</td>
</tr>
<tr>
<td>0.019</td>
<td>0.02</td>
<td>0.021</td>
<td>190</td>
</tr>
<tr>
<td>0.012666667</td>
<td>0.013333333</td>
<td>0.014</td>
<td>190</td>
</tr>
<tr>
<td>0.0095</td>
<td>0.01</td>
<td>0.0105</td>
<td>190</td>
</tr>
<tr>
<td>0.006462585</td>
<td>0.006802721</td>
<td>0.007142857</td>
<td>190</td>
</tr>
<tr>
<td>0.004846939</td>
<td>0.005102041</td>
<td>0.005357143</td>
<td>190</td>
</tr>
</tbody>
</table>
9.3.15 Safety Timer and Watchdog Timer

At the beginning of the charge cycle, the device starts the safety timer. If charging has not terminated before the programmed safety time, \( t_{\text{MAXCHG}} \), expires, the device enters idle mode and charging is disabled. The pre-charge safety time, \( t_{\text{PRECHG}} \), is 10% of \( t_{\text{MAXCHG}} \). When a safety timer fault occurs, a single 128 \( \mu \)s pulse is sent on the INT pin and the STAT and FAULT bits of the status registers are updated over I\(^2\)C. The CD pin or power must be toggled in order to clear the safety timer fault. The safety timer duration is programmable using the TMR bits. When the safety timer is active, changing the safety timer duration resets the safety timer. The device also contains a 2X_TIMER bit that enables the 2X timer function to prevent premature safety timer expiration when the charge current is reduced by a load on PMID, SYS, LS/LDO or a NTC condition. When \( t_{\text{2X_TIMER}} \) function is enabled, the timer is allowed to run at half speed when any loop is active other than CC or CV.

In addition to the safety timer, the device contains a 50-second watchdog timer that monitors the host through the I\(^2\)C interface. Once any I\(^2\)C transaction is performed on the I\(^2\)C interface, a watchdog timer is started. The watchdog timer is reset by any transaction by the host using the I\(^2\)C interface. If the watchdog timer expires without a reset from the I\(^2\)C interface, all registers except MRRESET_VIN and MRREC are reset to the default values.

9.3.16 External NTC Monitoring (TS)

The I\(^2\)C interface allows the user to easily implement the JEITA standard for systems where the battery pack thermistor is monitored by the host. Additionally, the device provides a flexible voltage based TS input for monitoring the battery pack NTC thermistor. The voltage at TS is monitored to determine that the battery is at a safe temperature during charging.

To satisfy the JEITA requirements, four temperature thresholds are monitored: the cold battery threshold, the cool battery threshold, the warm battery threshold, and the hot battery threshold. These temperatures correspond to the \( V_{(COLD)} \), \( V_{(COOL)} \), \( V_{(WARM)} \), and \( V_{(HOT)} \) threshold in the Electrical Characteristics. Charging and timers are suspended when \( V_{(TS)} < V_{(HOT)} \) or \( > V_{(COLD)} \). When \( V_{(COOL)} < V_{(TS)} < V_{(COLD)} \), the charging current is reduced to half of the programmed charge current. When \( V_{(HOT)} < V_{(TS)} < V_{(WARM)} \), the battery regulation voltage is reduced by 140 mV the programmed charge current.

The TS function is voltage based for maximum flexibility. Connect a resistor divider from \( V_{\text{IN}} \) to GND with TS connected to the center tap to set the threshold. The connections are shown in Figure 16. The resistor values are calculated using Equation 1 and Equation 2. To disable the TS function, pull TS above TS\(_{\text{OFF}} \) threshold.
Figure 16. TS Circuit

\[ R_{\text{LO}} = \frac{V_{\text{IN}} \times R_{\text{COLD}} \times R_{\text{HOT}}} {R_{\text{HOT}} \times \left( \frac{V_{\text{IN}}}{V_{\text{HOT}}} - 1 \right) - R_{\text{COLD}} \times \left( \frac{V_{\text{IN}}}{V_{\text{COLD}}} - 1 \right)} \]

\[ R_{\text{HI}} = \frac{1}{\left( \frac{V_{\text{IN}}}{V_{\text{COLD}}} - 1 \right)} \times \left( \frac{1}{R_{\text{LO}}} + \frac{1}{R_{\text{COLD}}} \right) \]

Where
- \( R_{\text{HOT}} \) = the NTC resistance at the hot temperature
- \( R_{\text{COLD}} \) = the NTC resistance at the cold temperature

The warm and cool thresholds are not independently programmable. The cool and warm NTC resistances for a selected resistor divider are calculated using Equation 3 and Equation 4.

\[ R_{\text{COOL}} = \frac{R_{\text{LO}} \times R_{\text{HI}} \times 0.57} {R_{\text{LO}} - R_{\text{LO}} \times 0.57 - R_{\text{HI}} \times 0.57} \]

\[ R_{\text{WARM}} = \frac{R_{\text{LO}} \times R_{\text{HI}} \times 0.38} {R_{\text{LO}}} - \left( R_{\text{LO}} \times 0.38 - R_{\text{HI}} \times 0.38 \right) \]
9.3.17 Thermal Protection

During the charging process, to prevent overheating in the device, the junction temperature of the die, \(T_J\), is monitored. When \(T_J\) reaches \(T_{(SHUTDOWN)}\) the device stops charging, disables the PMID output, disables the SYS output, and disables the LS/LDO output. During the time that \(T_{(SHUTDOWN)}\) is exceeded, the safety timer is reset and the watchdog timer continues to operate if in host mode. The charge cycle resumes when \(T_J\) falls below \(T_{(SHUTDOWN)}\) by \(T_{(HYS)}\).

To avoid reaching thermal shutdown, ensure that the system power dissipation is under the limits of the device. The power dissipated by the device can be calculated using Equation 5.

\[
P_{\text{DISS}} = P_{(\text{BLOCK})} + P_{(\text{SYS})} + P_{(\text{LS/LDO})} + P_{(\text{BAT})}
\]

(5)

Where

- \(P_{(\text{BLOCK})} = (V_{\text{IN}} - V_{(\text{PMID})}) \times I_{\text{IN}}\)
- \(P_{(\text{SYS})} = I_{\text{SYS}}^2 \times R_{\text{DS(ON_HS)}}\)
- \(P_{(\text{LS/LDO})} = (V_{(\text{INLS})} - V_{(\text{LS/LDO})}) \times I_{(\text{LS/LDO})}\)
- \(P_{(\text{BAT})} = (V_{(\text{PMID})} - V_{(\text{BAT})}) \times I_{(\text{BAT})}\)

9.3.18 Typical Application Power Dissipation

The die junction temperature, \(T_J\), can be estimated based on the expected board performance using Equation 6.

\[
T_J = T_A + \theta_{JA} \times P_{\text{DISS}}
\]

(6)

The \(\theta_{JA}\) is largely driven by the board layout. For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report SPRA953. Under typical conditions, the time spent in this state is short.

9.3.19 Status Indicators (PG and INT)

The device contains two open-drain outputs that signal its status and are valid only after the device has completed start-up into a valid state. If the part starts into a fault, interrupts will not be sent. The PG output signals when a valid input source is connected. PG pulls to GND when \(V_{\text{IN}}\) is above \(V_{\text{UVLO}}\). PG is high-impedance when the input power is not within specified limits. Connect PG to the desired logic voltage rail using a 1-kΩ to 100-kΩ resistor, or use with an LED for visual indication.

The PG pin can be configured as a MR shifted (MRS) output when the PGB_MRS bit is set to 1. PG is high-impedance when the MR input is not low, and PG pulls to GND when the MR input is below \(V_{\text{OL(TH_MRS)}}\). Connect PG to the desired logic voltage rail using a 1-kΩ to 100-kΩ resistor.

When enabled through OTP, the PG pin also functions as an OVP/UVP indicator. When the device is below \(V_{\text{SLP}}\) or \(V_{\text{IN(DPM)}}\) (if enabled), a single 128us pulse is sent on PG to notify the host, repeating once per minute. When the device has an input voltage greater than \(V_{\text{BAT}} + 1\) V and \(V_{\text{IN}}\) is less than \(V_{\text{OVP}}\), two consecutive 128us pulses are sent on PG, to notify the host, repeating once per minute. The PG pin does not function as an input power good indicator in this mode.

The INT pin is pulled low during charging when the EN_INT bit is set to 1 and interrupts are pulled high. When EN_INT is set to 0, charging status is not indicated on the INT pin. When charge is complete or disabled, INT is high impedance. The charge status is valid whether it is the first charge or recharge. When a fault occurs, a 128 μs pulse (interrupt) is sent on INT to notify the host.

9.3.20 Chip Disable (CD)

The device contains a CD input that is used to disable the device and place it into a high impedance mode when only battery is present. In this case, when CD is low, PMID and SYS remain active, and the battery discharge FET is turned on. If the LS/LDO output has been enabled prior to pulling CD low, it will stay on. The LSCTRL pin can also enable/disable the LS/LDO output when the CD pin is pulled low. The CD pin has an internal pull-down.

If \(V_{\text{IN}}\) is present and the CD input is pulled low, charge is enabled and all other functions remain active. If \(V_{\text{IN}}\) is present and the CD input is pulled high, charge is disabled.
9.3.21 Buck (PWM) Output

The device integrates a low quiscent current switching regulator with DCS control allowing high efficiency down to 10-µA load currents. DCS control combines the advantages of hysteretic and voltage mode control. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors. During PWM mode, it operates in continuous conduction mode, with a frequency up to 2 MHz. If the load current decreases, the converter enters a power save mode to maintain high efficiency down to light loads. In this mode, the device generates a single switching pulse to ramp up the inductor current and recharge the output capacitor, followed by a sleep period where most of the internal circuits are shut down to achieve a low quiescent current. The duration of the sleep period depends on the load current and the inductor peak current.

The output voltage is programmable using the SYS_SEL and SYS_VOUT bits in the SYS VOUT control register.

The SW output is enabled using the EN_SYS_OUT bit in the register. This bit is for testing and debug only and not intended to be used in the final system. When the device is enabled, the internal reference is powered up and the device enters softstart, starts switching, and ramps up the output voltage. When SW is disabled, the output is in shutdown mode in a low quiescent state. The device provides automatic output voltage discharge so the output voltage will ramp up from zero once the device in enabled again. Once SYS has been disabled, either VIN needs to be connected or the MR button must be held low for the tRESET duration to re-enable SYS.

The output is optimized for operation with a 2.2-µH inductor and 10-µF output capacitor. Table 6 shows the recommended LC output filter combinations.

<table>
<thead>
<tr>
<th>INDUCTOR VALUE (µH)</th>
<th>OUTPUT CAPACITOR VALUE (µF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.2</td>
<td>4.7</td>
</tr>
<tr>
<td></td>
<td>10</td>
</tr>
<tr>
<td></td>
<td>22</td>
</tr>
</tbody>
</table>

Table 6. Recommended Output Filter

The inductor value affects the peak-to-peak ripple current, the PWM-to-PFM transition point where the part enters and exits Pulse Frequency Modulation to lower the power consumed at low loads, the output voltage ripple and the efficiency. The selected inductor must be selected for its DC resistance and saturation current. The inductor ripple current (∆IL) can be estimated according to Equation 7.

\[ ∆I_L = V_{OUT} \times (1-(V_{OUT}/V_{IN}))/\left(\frac{L}{f}\right) \]  

Use Equation 8 to calculate the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current. As the size of the inductor decreases, the saturation “knee” must be carefully considered to ensure that the inductance does not decrease during higher load condition or transient. This is recommended because during a heavy load transient the inductor current rises above the calculated value. A more conservative way is to select the inductor saturation current above the high-side MOSFET switch current.

\[ I_{L}(max) = I_{OUT}(max) + ∆I_L / 2 \]  

Where
- F = Switching Frequency
- L = Inductor Value
- ∆IL = Peak to Peak inductor ripple current
- IL(max) = Maximum Inductor current

In DC/DC converter applications, the efficiency is affected by the inductor AC resistance and by the inductor DCR value.

Table 7 shows recommended inductor series from different suppliers.

<table>
<thead>
<tr>
<th>INDUCTANCE (µH)</th>
<th>DCR (Ω)</th>
<th>DIMENSIONS (mm²)</th>
<th>INDUCTOR TYPE</th>
<th>SUPPLIER (1)</th>
<th>COMMENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.2</td>
<td>0.300</td>
<td>1.6 x 0.8 x 0.8</td>
<td>MDT1608CH2R2N</td>
<td>TOKO</td>
<td>Smallest size, 75mA max</td>
</tr>
<tr>
<td>2.2</td>
<td>0.170</td>
<td>1.6 x 0.8 x 0.8</td>
<td>GLFR1608T2R2M</td>
<td>TDK</td>
<td>Smallest size, 150mA max</td>
</tr>
</tbody>
</table>

(1) See Third-party Products Disclaimer
The PWM allows the use of small ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. At light load currents, the converter operates in Power Save Mode and the output voltage ripple is dependent on the output capacitor value and the PFM peak inductor current. Because the PWM converter has a pulsating input current, a low ESR input capacitor is required on PMID for the best voltage filtering to ensure proper function of the device and to minimize input voltage spikes. For most applications a 10-µF capacitor value is sufficient. The PMID capacitor can be increased to 22 µF for better input voltage filtering.

Table 8 shows the recommended input/output capacitors.

### Table 7. Inductor Series (continued)

<table>
<thead>
<tr>
<th>INDUCTANCE (µH)</th>
<th>DCR (Ω)</th>
<th>DIMENSIONS (mm³)</th>
<th>INDUCTOR TYPE</th>
<th>SUPPLIER (1)</th>
<th>COMMENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.2</td>
<td>0.245</td>
<td>2.0 x 1.2 x 1.0</td>
<td>MDT2012CH2R2N</td>
<td>TOKO</td>
<td>Small size, high efficiency</td>
</tr>
<tr>
<td>2.2</td>
<td>0.23</td>
<td>2.0 x 1.2 x 1.0</td>
<td>MIPSZ2012 2R2</td>
<td>TDK</td>
<td></td>
</tr>
<tr>
<td>2.2</td>
<td>0.225</td>
<td>2.0 x 1.6 x 1.0</td>
<td>74438343022</td>
<td>Wurth</td>
<td></td>
</tr>
<tr>
<td>2.2</td>
<td>0.12</td>
<td>2.5 x 2.0 x 1.2</td>
<td>MIPS2520 2R2</td>
<td>TDK</td>
<td></td>
</tr>
<tr>
<td>2.2</td>
<td>0.145</td>
<td>3.3 x 3.3 x 1.4</td>
<td>LPS3314</td>
<td>Coicraft</td>
<td></td>
</tr>
</tbody>
</table>

The output voltage is programmable using the LS_LDO bits in the register. The LS/LDO voltage is calculated using Equation 9.

\[
LS/LDO = 0.8 \text{ V} + LS\_LDO\_CODE \times 100 \text{ mV}
\]  

(9)

If a value greater than 3.3 V is written, the setting goes to pass-through mode where \(LS/LDO = \text{VINLS} - V_{\text{DROPOUT}}\). Table 9 summarizes the control of the LS/LDO output based on the \(I^2C\) or LSCTRL pin setting:

### Table 8. Capacitors

<table>
<thead>
<tr>
<th>CAPACITANCE (µF)</th>
<th>SIZE</th>
<th>CAPACITOR TYPE</th>
<th>SUPPLIER(1)</th>
<th>COMMENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>0603</td>
<td>GRM188R60J106ME84</td>
<td>Murata</td>
<td>Recommended</td>
</tr>
<tr>
<td>10</td>
<td>0402</td>
<td>CL05A106MP5NUNC</td>
<td>Samsung EMA</td>
<td>Smallest size</td>
</tr>
</tbody>
</table>

(1) See Third-party Products Disclaimer

### 9.3.22 Load Switch / LDO Output and Control

The device integrates a low Iq load switch which can also be used as a regulated output. The LSCTRL pin can be used to turn the load on or off. Activating LSCTRL continuously holds the switch in the on state so long as there is not a fault. The signal is active HI and has a low threshold making it capable of interfacing with low voltage signals. To limit voltage drop or voltage transients, a small ceramic capacitor must be placed close to VINLS. Due to the body diode of the PMOS switch, it is recommended to have the capacitor on VINLS ten times larger than the output capacitor on LS/LDO.

The output voltage is programmable using the LS_LDO bits in the register. The LS/LDO voltage is calculated using Equation 9.

\[
LS/LDO = 0.8 \text{ V} + LS\_LDO\_CODE \times 100 \text{ mV}
\]  

(9)

If a value greater than 3.3 V is written, the setting goes to pass-through mode where \(LS/LDO = \text{VINLS} - V_{\text{DROPOUT}}\). Table 9 summarizes the control of the LS/LDO output based on the \(I^2C\) or LSCTRL pin setting:

### Table 9. LS/LDO Output Control

<table>
<thead>
<tr>
<th>I²C LS_LDO_EN</th>
<th>PIN LSCTRL</th>
<th>I²C V_LDO &gt; 3.3</th>
<th>LS/LDO Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Pulldown</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Pulldown</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>V_LDO</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>V_LDO</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>V_LDO</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>V_LDO</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>V_LDO</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>V_LDO</td>
</tr>
</tbody>
</table>
If the output of the LDO is less than the programmed $V_{\text{(SYS)}}$ voltage, connect VINLS to SYS. If the output of the LDO is greater than the programmed $V_{\text{SYS}}$ voltage, connect VINLS to PMID.

The current capability of the LDO depends on the VINLS input voltage and the programmed output voltage. The full 100-mA output current for 0.8-V output voltage can be achieved when $V_{\text{(VINLS)}} > 3.25 \, \text{V}$. The full 100-mA output current for 3.3-V output voltage can be achieved when $V_{\text{(VINLS)}} > 3.6 \, \text{V}$.

When the LSLDO output is disabled with LSCTRL or through the register, an internal pull-down discharges the output.

### 9.3.23 Manual Reset Timer and Reset Output (MR and RESET)

The MR input has an internal pull-up to BAT, and MR is functional only when BAT is present or when VIN is valid, stable, and charge is enabled. If MR input is asserted during a transient condition while VIN ramps up the IC may incorrectly turn off the SYS buck output, therefore MR should not be asserted during this condition in order to avoid unwanted shutdown of SYS output rail. The input conditions can be adjusted by using MRWAKE bits for the wake conditions and MRRESET bits for the reset conditions. When a wake condition is met, a 128-µs pulse is sent on INT to notify the host, and the WAKE1 and/or WAKE2 bits are updated on $I^2$C. The MR_WAKE bits and RESET_FAULT bits are not cleared until the Push-button Control Register is read from $I^2$C.

When a MR reset condition is met, a 128us pulse is sent on INT to notify the host and a RESET signal is asserted. A reset pulse occurs with duration of $t_{\text{RESET.D}}$ only one time after each valid MRRESET condition. The MR pin must be released (go high) and then driven low for the MRWAKE period before RESET asserts again. After RESET is asserted with battery only present, the device enters either Ship mode or Hi-Z mode depending on MRREC register settings. After RESET is asserted with a valid $V_{\text{IN}}$ present, the device resumes operation prior to the MR button press. If SYS was disabled prior to RESET, the SYS output is re-enabled if recovering into Hi-Z or Active Battery.

The MRRESET_VIN register can be configured to have RESET asserted by a button press only, or by a button press and $V_{\text{IN}}$ present ($V_{\text{UVLO}} + V_{\text{SLP}} < V_{\text{IN}} < V_{\text{OVP}}$).
## 9.4 Device Functional Modes

### Table 10. Modes and Functions

<table>
<thead>
<tr>
<th>FUNCTION</th>
<th>READY (PRIOR TO I²C) AND AFTER RESET</th>
<th>HOST MODE READY (AFTER I²C)</th>
<th>CHARGE</th>
<th>SHIP MODE</th>
<th>HIGH_Z</th>
<th>ACTIVE BATTERY</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOVP</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>VUVLO</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>VBATUVLO</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>VINDPM</td>
<td>OTP or registers</td>
<td>OTP or registers</td>
<td>If enabled</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>SYS</td>
<td>OTP or registers</td>
<td>OTP or registers</td>
<td>If enabled</td>
<td>No</td>
<td>If enabled</td>
<td>If enabled</td>
</tr>
<tr>
<td>LS/LDO</td>
<td>OTP or registers</td>
<td>OTP or registers</td>
<td>If enabled</td>
<td>No</td>
<td>If enabled</td>
<td>If enabled</td>
</tr>
<tr>
<td>BATFET</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>TS</td>
<td>Yes (VIN Valid)</td>
<td>Yes (VIN Valid)</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>IPRETERM</td>
<td>External</td>
<td>OTP, registers, or external</td>
<td>OTP, registers, or external</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>ISET</td>
<td>External</td>
<td>OTP, registers, or external</td>
<td>OTP, registers, or external</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>ILIM</td>
<td>External</td>
<td>OTP, registers, or external</td>
<td>OTP, registers, or external</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>VR input</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>LSCTRL input</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>RESET output</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>INT output</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>I²C interface</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>CD input</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>PG output</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>If enabled</td>
</tr>
<tr>
<td>VBMN</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
</tbody>
</table>

### Table 11. Fault and Status Condition Responses

<table>
<thead>
<tr>
<th>FAULT or STATUS</th>
<th>ACTIONS</th>
<th>CHARGER BEHAVIOR</th>
<th>SYS BEHAVIOR</th>
<th>LS/LDO BEHAVIOR</th>
<th>TS BEHAVIOR</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN_OV</td>
<td>Update VIN_OV status, Update STAT to fault, interrupt on INT, PG shown not good</td>
<td>Disabled</td>
<td>Enabled through BAT</td>
<td>Enabled through BAT</td>
<td>Disabled</td>
</tr>
<tr>
<td>VIN_UV</td>
<td>Update VIN_UV status, Update STAT to fault, interrupt on INT, PG shown not good</td>
<td>Disabled</td>
<td>Enabled through BAT</td>
<td>Enabled through BAT</td>
<td>Disabled</td>
</tr>
<tr>
<td>VIN_ILIM</td>
<td>Update charge in progress status, interrupt on INT, input current is limited</td>
<td>Enabled, input current limited</td>
<td>Enabled (if enabled)</td>
<td>Enabled (if enabled)</td>
<td>Enabled</td>
</tr>
<tr>
<td>OVER_TEMP</td>
<td></td>
<td>Disabled</td>
<td>Disabled</td>
<td>Disabled</td>
<td>Disabled</td>
</tr>
<tr>
<td>BAT_UVLO</td>
<td>Update BAT_UVLO status, Update STAT to fault, interrupt on INT</td>
<td>Pre-charge</td>
<td>Enabled (if enabled) and VIN Valid</td>
<td>Enabled (if VIN Valid)</td>
<td>Enabled if VIN Valid</td>
</tr>
<tr>
<td>SW_SYS_SHORT</td>
<td></td>
<td>Enabled</td>
<td>Current Limit</td>
<td>Enabled</td>
<td>Enabled</td>
</tr>
<tr>
<td>LS_LDO_OCP</td>
<td></td>
<td>Enabled</td>
<td>Enabled (if enabled)</td>
<td>Current Limit</td>
<td>Enabled</td>
</tr>
<tr>
<td>TIMER fault</td>
<td></td>
<td>Disabled</td>
<td>Enabled (if enabled)</td>
<td>Enabled</td>
<td>Disabled</td>
</tr>
<tr>
<td>VINDPM</td>
<td></td>
<td>Enabled, input current reduced</td>
<td>Enabled (if enabled)</td>
<td>Enabled (if enabled)</td>
<td>Enabled</td>
</tr>
</tbody>
</table>
**Table 11. Fault and Status Condition Responses (continued)**

<table>
<thead>
<tr>
<th>FAULT or STATUS</th>
<th>ACTIONS</th>
<th>CHARGER BEHAVIOR</th>
<th>SYS BEHAVIOR</th>
<th>LS/LDO BEHAVIOR</th>
<th>TS BEHAVIOR</th>
</tr>
</thead>
<tbody>
<tr>
<td>TS_FAULT COLD or HOT</td>
<td>Update TS_FAULT to COLD OR HOT, Update STAT to fault, interrupt on INT</td>
<td>Disabled</td>
<td>Enabled (if enabled)</td>
<td>Enabled (if enabled)</td>
<td>Enabled</td>
</tr>
<tr>
<td>TS_FAULT COOL</td>
<td>Update TS_FAULT to COOL, Update STAT to fault, interrupt on INT</td>
<td>Reduce ICHG to ½</td>
<td>Enabled (if enabled)</td>
<td>Enabled (if enabled)</td>
<td>Enabled</td>
</tr>
<tr>
<td>TS_FAULT WARM</td>
<td>Update TS_FAULT to WARM, Update STAT to fault, interrupt on INT</td>
<td>Reduce VBATREG by 140 mV</td>
<td>Enabled (if enabled)</td>
<td>Enabled (if enabled)</td>
<td>Enabled</td>
</tr>
<tr>
<td>Charge Done</td>
<td>Update STAT to Charge Done, interrupt on INT</td>
<td>Disabled, monitor for VBAT falling below VRCHG</td>
<td>Enabled (if enabled)</td>
<td>Enabled (if enabled)</td>
<td>Enabled</td>
</tr>
</tbody>
</table>

**Comments about naming convention**

"/CE" or "HZ_MODE" -> Register name: event caused by user / configuration

"/" -> Not

"♀" -> Event caused by external influence

"Event\textsuperscript{condition}" -> describes the event with a specific condition

---

**Figure 17. State Diagram**
Figure 18. Change State Diagram

9.5 Programming

9.5.1 Serial Interface Description

The device uses an I²C compatible interface to program and read many parameters. I²C is a 2-wire serial interface developed by NXP. The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open drain I/O terminals, SDA and SCL. A master device, usually a microcontroller or digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The device works as a slave and supports the following data transfer modes, as defined in the I²C BUS Specification: standard mode (100 kbps) and fast mode (400kbps). The interface adds flexibility to the battery management solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. The I²C circuitry is powered from the battery in active battery mode. The battery voltage must stay above V(BATUVLO) when no V(IN) is present to maintain proper operation.

The data transfer protocol for standard and fast modes is exactly the same; therefore, they are referred to as the F/S-mode in this document. The device only supports 7-bit addressing. The device 7-bit address is 6A (8-bit shifted address is D4).
Programming (continued)

To avoid I²C hang-ups, a timer (tI₂CRESET) runs during I²C transactions. If the SDA line is held low longer than tI₂CRESET, any additional commands are ignored and the I²C engine is reset. The timeout is reset with START and repeated START conditions and stops when a valid STOP condition is sent.

9.5.2 F/S Mode Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 19. All I²C-compatible devices should recognize a start condition.

![Figure 19. Start Stop Condition](image)

The master then generates the SCL pulses, and transmits the address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 20). All I²C-compatible devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates and acknowledge (see Figure 21) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting the acknowledge, the master knows that communication link with a slave has been established.

![Figure 20. Bit Transfer on the Serial Interface](image)
Programming (continued)

The master generates further SCL cycles to either transmit data to the slave (R/W bit 0) or receive data from the slave (R/W bit 1). In either case, the receiver needs to acknowledge the data sent by the transmitter. An acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary. To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 22). This releases the bus and stops the communication link with the addressed slave. All I²C compatible devices must recognize the STOP condition. Upon the receipt of a STOP condition, all devices know that the bus is released, and wait for a START condition followed by a matching address. If a transaction is terminated prematurely, the master needs to send a STOP condition to prevent the slave I²C logic from remaining in an incorrect state. Attempting to read data from register addresses not listed in this section results in 0xFFh being read out.

Figure 21. Acknowledge on the I²C Bus

Figure 22. Bus Protocol
9.6 Register Maps

9.6.1 Status and Ship Mode Control Register

Memory location 0x00h, Reset State: xx0x xxx1 (bq25120)

**Figure 23. Status and Ship Mode Control Register**

<table>
<thead>
<tr>
<th>7 (MSB)</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0 (LSB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>x</td>
<td>x</td>
<td>0</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>1</td>
</tr>
</tbody>
</table>

R = Write Only

**Table 12. Status and Ship Mode Control Register**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>B7 (MSB)</td>
<td>STAT_1</td>
<td>R</td>
<td>x</td>
<td>00 - Ready</td>
</tr>
<tr>
<td></td>
<td>STAT_0</td>
<td>R</td>
<td>x</td>
<td>01 - Charge in Progress</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10 - Charge done</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>11 - Fault</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Status is current status only.</td>
</tr>
<tr>
<td>B5</td>
<td>EN_SHIPMODE</td>
<td>Write Only</td>
<td>0</td>
<td>0 – Normal Operation</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 – Ship Mode Enabled</td>
</tr>
<tr>
<td>B4</td>
<td>RESETFAULT</td>
<td>R</td>
<td>x</td>
<td>1 – RESET fault. Indicates when the device meets the RESET conditions, and is cleared after I²C read.</td>
</tr>
<tr>
<td>B3</td>
<td>TIMER</td>
<td>R</td>
<td>x</td>
<td>1 – Safety timer fault. Continues to show fault after an I²C read unless the CD pin or power have been toggled.</td>
</tr>
<tr>
<td>B2</td>
<td>VINDPM_STAT</td>
<td>R</td>
<td>x</td>
<td>0 – VIN_DPM is not active</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 – VIN_DPM is active</td>
</tr>
<tr>
<td>B1</td>
<td>CD_STAT</td>
<td>R</td>
<td>x</td>
<td>0 – CD low, IC enabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 – CD high, IC disabled</td>
</tr>
<tr>
<td>B0 (LSB)</td>
<td>SYS_EN_STAT</td>
<td>R</td>
<td>x</td>
<td>1 – SW enabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 – SW disabled</td>
</tr>
</tbody>
</table>
9.6.2 Faults and Faults Mask Register

Memory location 0x01h, Reset State: xxxx 0000 (bq25120)

**Figure 24. Faults and Faults Mask Register**

<table>
<thead>
<tr>
<th>Bit (MSB)</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0 (LSB)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>R</td>
<td>R</td>
<td>R</td>
<td>R</td>
<td>R</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
</tr>
</tbody>
</table>

**Table 13. Faults and Faults Mask Register**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>B7 (MSB)</td>
<td>VIN_OV</td>
<td>R</td>
<td>x</td>
<td>1 - VIN overvoltage fault. VIN_OV continues to show fault after an I2C read as long as OV exists</td>
</tr>
<tr>
<td>B6</td>
<td>VIN_UV</td>
<td>R</td>
<td>x</td>
<td>1 - VIN undervoltage fault. VIN_UV is set when the input falls below V_{SLP}. VIN_UV fault shows only one time. Once read, VIN_UV clears until the the UVLO event occurs.</td>
</tr>
<tr>
<td>B5</td>
<td>BAT_UVLO</td>
<td>R</td>
<td>x</td>
<td>1 - BAT_UVLO fault. BAT_UVLO continues to show fault after an I2C read as long as BAT_UVLO conditions exist.</td>
</tr>
<tr>
<td>B4</td>
<td>BAT_OCP</td>
<td>R</td>
<td>x</td>
<td>1 - BAT_OCP fault. BAT_OCP is cleared after I2C read.</td>
</tr>
<tr>
<td>B3</td>
<td>VIN_OV_M</td>
<td>R/W</td>
<td>0</td>
<td>1 - Mask VIN overvoltage fault</td>
</tr>
<tr>
<td>B2</td>
<td>VIN_UV_M</td>
<td>R/W</td>
<td>0</td>
<td>1 - Mask VIN undervoltage fault</td>
</tr>
<tr>
<td>B1</td>
<td>BAT_UVLO_M</td>
<td>R/W</td>
<td>0</td>
<td>1 - Mask BAT UVLO fault</td>
</tr>
<tr>
<td>B0 (LSB)</td>
<td>BAT_OCP_M</td>
<td>R/W</td>
<td>0</td>
<td>1 - Mask BAT_OCP fault</td>
</tr>
</tbody>
</table>
9.6.3 TS Control and Faults Masks Register

Memory location 0x02h, Reset State: 1xxx 1000 (bq25120)

![Figure 25. TS Control and Faults Masks Register (02)](image)

Table 14. TS Control and Faults Masks Register, Memory Location 0010

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>TS_EN</td>
<td>R/W</td>
<td>1</td>
<td>0 – TS function disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 – TS function enabled</td>
</tr>
<tr>
<td>6</td>
<td>TS_FAULT1</td>
<td>R</td>
<td>x</td>
<td>TS Fault mode:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>00 – Normal, No TS fault</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>01 – TS temp &lt; T_COLD or TS temp &gt; T_HOT (Charging suspended)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10 – T_COLD &gt; TS temp &gt; T_COLD (Charging current reduced by half)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>11 – T_WARM &lt; TS temp &lt; T_HOT (Charging voltage reduced by 140 mV)</td>
</tr>
<tr>
<td>5</td>
<td>TS_FAULT0</td>
<td>R</td>
<td>x</td>
<td>0 – No TS OFF fault</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 – TS OFF fault indicated, and charge has stopped (if enabled in OTP_EN_TS_OPEN)</td>
</tr>
<tr>
<td>4</td>
<td>TS_FAULT_OPEN</td>
<td>R</td>
<td>x</td>
<td>0 – Disable INT function (INT only shows faults and does not show charge status)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 – Enable INT function (INT shows faults and charge status)</td>
</tr>
<tr>
<td>3</td>
<td>EN_INT</td>
<td>R/W</td>
<td>1</td>
<td>0 – Mask Wake Condition from MR</td>
</tr>
<tr>
<td>2</td>
<td>WAKE_M</td>
<td>R/W</td>
<td>0</td>
<td>1 – Mask RESET condition from MR</td>
</tr>
<tr>
<td>1</td>
<td>RESET_M</td>
<td>R/W</td>
<td>0</td>
<td>1 – Mask Timer fault (safety)</td>
</tr>
<tr>
<td>0</td>
<td>TIMER_M</td>
<td>R/W</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>
9.6.4 Fast Charge Control Register

Memory location 0x03h, Reset State: 0001 0100 (bq25120)

**Figure 26. Fast Charge Control Register**

<table>
<thead>
<tr>
<th>7 (MSB)</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0 (LSB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
</tr>
</tbody>
</table>

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 15. Fast Charge Control Register**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>B7 (MSB)</td>
<td>ICHRG_RANGE</td>
<td>R/W</td>
<td>0</td>
<td>0 – to select charge range from 5 mA to 35 mA, ICHRG bits are 1-mA steps</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 – to select charge range from 40 mA to 300 mA, ICHRG bits are 10-mA steps</td>
</tr>
<tr>
<td>B6</td>
<td>ICHRG_4</td>
<td>R/W</td>
<td>0</td>
<td>Charge current 16 mA or 160 mA</td>
</tr>
<tr>
<td>B5</td>
<td>ICHRG_3</td>
<td>R/W</td>
<td>0</td>
<td>Charge current 8 mA or 80 mA</td>
</tr>
<tr>
<td>B4</td>
<td>ICHRG_2</td>
<td>R/W</td>
<td>1</td>
<td>Charge current 4 mA or 40 mA</td>
</tr>
<tr>
<td>B3</td>
<td>ICHRG_1</td>
<td>R/W</td>
<td>0</td>
<td>Charge current 2 mA or 20 mA</td>
</tr>
<tr>
<td>B2</td>
<td>ICHRG_0</td>
<td>R/W</td>
<td>1</td>
<td>Charge current 1 mA or 10 mA</td>
</tr>
<tr>
<td>B1</td>
<td>CE</td>
<td>R/W</td>
<td>0</td>
<td>0 – Charger enabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 – Charger is disabled</td>
</tr>
<tr>
<td>B0 (LSB)</td>
<td>HZ_MODE</td>
<td>R/W</td>
<td>0</td>
<td>0 – Not high impedance mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 – High impedance mode</td>
</tr>
</tbody>
</table>

ICHRG_RANGE and ICHRG bits are used to set the charge current. The ICHRG is calculated using the following equation: If ICHRG_RANGE is 0, then ICHRG = 5 mA + ICHRG_CODE x 1 mA. If ICHRG_RANGE is 1, then ICHRG = 40 mA + ICHRG_CODE x 10 mA. If a value greater than 35 mA (ICHRG_RANGE = 0) or 300 mA (ICHRG_RANGE = 1) is written, the setting goes to 35 mA or 300 mA respectively except if the ICHRG bits are all 1 (that is, 11111), then the externally programmed value is used. The PRETERM bits must also be set prior to writing all 1s to ensure the external ISET current is used as well as the proper termination and pre-charge values are used. For IPRETERM = 5%, set the IPRETERM bits to 000001, for IPRETERM = 10%, set the IPRETERM bits to 000010, for IPRETERM = 15%, set the IPRETERM bits to 000100, and for IPRETERM = 20%, set the IPRETERM bits to 001000. The default is programmed by the external resistor on ISET, or if not populated and tied to GND, by OTP.
9.6.5 Termination/Pre-Charge and I²C Address Register

Memory location 0x04h, Reset State: 0000 1110 (bq25120)

![Figure 27. Termination/Pre-Charge and I²C Address Register](image)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>B7 (MSB)</td>
<td>IPRETERM_RANGE</td>
<td>R/W</td>
<td>0</td>
<td>0 – to select termination range from 500 µA to 5 mA, IPRETERM bits are 500-µA steps</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 – to select charge range from 6 mA to 37 mA, IPRETERM bits are 1-mA steps</td>
</tr>
<tr>
<td>B6</td>
<td>IPRETERM_4</td>
<td>R/W</td>
<td>0</td>
<td>Termination current 8 mA or 16 mA</td>
</tr>
<tr>
<td>B5</td>
<td>IPRETERM_3</td>
<td>R/W</td>
<td>0</td>
<td>Termination current 4 mA or 8 mA</td>
</tr>
<tr>
<td>B4</td>
<td>IPRETERM_2</td>
<td>R/W</td>
<td>0</td>
<td>Termination current 2 mA or 4 mA</td>
</tr>
<tr>
<td>B3</td>
<td>IPRETERM_1</td>
<td>R/W</td>
<td>1</td>
<td>Termination current 1 mA or 2 mA</td>
</tr>
<tr>
<td>B2</td>
<td>IPRETERM_0</td>
<td>R/W</td>
<td>1</td>
<td>Termination current 500 µA or 1 mA</td>
</tr>
<tr>
<td>B1</td>
<td>TE</td>
<td>R/W</td>
<td>1</td>
<td>0 – Disable charge current termination</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 – Enable charge current termination</td>
</tr>
<tr>
<td>B0 (LSB)</td>
<td></td>
<td>R/W</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. Termination/Pre-Charge and I²C Address Register

9.6.6 Battery Voltage Control Register

Memory location 0x05h, Reset State: 0111 1000 (bq25120)

![Figure 28. Battery Voltage Control Register](image)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>B7 (MSB)</td>
<td>VBREG_6</td>
<td>R/W</td>
<td>0</td>
<td>Battery Regulation Voltage: 640 mV</td>
</tr>
<tr>
<td>B6</td>
<td>VBREG_5</td>
<td>R/W</td>
<td>1</td>
<td>Battery Regulation Voltage: 320 mV</td>
</tr>
<tr>
<td>B5</td>
<td>VBREG_4</td>
<td>R/W</td>
<td>1</td>
<td>Battery Regulation Voltage: 160 mV</td>
</tr>
<tr>
<td>B4</td>
<td>VBREG_3</td>
<td>R/W</td>
<td>1</td>
<td>Battery Regulation Voltage: 80 mV</td>
</tr>
<tr>
<td>B3</td>
<td>VBREG_2</td>
<td>R/W</td>
<td>1</td>
<td>Battery Regulation Voltage: 40 mV</td>
</tr>
<tr>
<td>B2</td>
<td>VBREG_1</td>
<td>R/W</td>
<td>0</td>
<td>Battery Regulation Voltage: 20 mV</td>
</tr>
<tr>
<td>B1</td>
<td>VBREG_0</td>
<td>R/W</td>
<td>0</td>
<td>Battery Regulation Voltage: 10 mV</td>
</tr>
<tr>
<td>B0 (LSB)</td>
<td></td>
<td>R/W</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 17. Battery Voltage Control Register

VBREG Bits: Use VBREG bits to set the battery regulation threshold. The $V_{BATREG}$ is calculated using the following equation: $V_{BATREG} = 3.6 \, V + VBREGCode \times 10 \, mV$. The charge voltage range is from 3.6 V to 4.65 V. If a value greater than 4.65 V is written, the setting goes to 4.65 V. Default is programmed by OTP.
9.6.7 SYS VOUT Control Register

Memory location 0x06h, Reset State: 1010 1010 (bq25120)

**Figure 29. SYS VOUT Control Register**

<table>
<thead>
<tr>
<th>Bit (MSB)</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>EN_SYS_OUT</td>
<td>R/W</td>
<td>1</td>
<td>0 – Disable SW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 – Enable SW (When disabled, output is pulled low)</td>
</tr>
<tr>
<td>6</td>
<td>SYS_SEL1</td>
<td>R/W</td>
<td>0</td>
<td>00 – 1.1 V and 1.2 V selection</td>
</tr>
<tr>
<td>5</td>
<td>SYS_SEL2</td>
<td>R/W</td>
<td>1</td>
<td>01 – 1.3 V through 2.8 V selection</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10 – Not Valid</td>
</tr>
<tr>
<td>4</td>
<td>SYS_SEL3</td>
<td>R/W</td>
<td>0</td>
<td>11 – 1.8 V through 3.3 V selection</td>
</tr>
<tr>
<td>3</td>
<td>SYS_VOUT_3</td>
<td>R/W</td>
<td>0</td>
<td>OUT Voltage: 800 mV step if SYS_SEL is 01 or 11</td>
</tr>
<tr>
<td>2</td>
<td>SYS_VOUT_2</td>
<td>R/W</td>
<td>1</td>
<td>OUT Voltage: 400 mV step if SYS_SEL is 01 or 11</td>
</tr>
<tr>
<td>1</td>
<td>SYS_VOUT_1</td>
<td>R/W</td>
<td>0</td>
<td>OUT Voltage: 200 mV step if SYS_SEL is 01 or 11</td>
</tr>
<tr>
<td>0 (LSB)</td>
<td>SYS_VOUT_0</td>
<td>R/W</td>
<td>1</td>
<td>OUT Voltage: 100 mV step if SYS_SEL is 01 or 11</td>
</tr>
</tbody>
</table>

**Table 19. SYS_SEL Codes**

<table>
<thead>
<tr>
<th>SYS_SEL</th>
<th>SYS_VOUT</th>
<th>TYP</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>0000</td>
<td>1.1</td>
<td>V</td>
</tr>
<tr>
<td>00</td>
<td>0001</td>
<td>1.2</td>
<td>V</td>
</tr>
<tr>
<td>00</td>
<td>0010</td>
<td>1.25</td>
<td>V</td>
</tr>
<tr>
<td>00</td>
<td>0011</td>
<td>1.333</td>
<td>V</td>
</tr>
<tr>
<td>00</td>
<td>0100</td>
<td>1.417</td>
<td>V</td>
</tr>
<tr>
<td>00</td>
<td>0101</td>
<td>1.5</td>
<td>V</td>
</tr>
<tr>
<td>00</td>
<td>0110</td>
<td>1.583</td>
<td>V</td>
</tr>
<tr>
<td>00</td>
<td>0111</td>
<td>1.667</td>
<td>V</td>
</tr>
<tr>
<td>00</td>
<td>1000</td>
<td>1.75</td>
<td>V</td>
</tr>
<tr>
<td>00</td>
<td>1001</td>
<td>1.833</td>
<td>V</td>
</tr>
<tr>
<td>00</td>
<td>1010</td>
<td>1.917</td>
<td>V</td>
</tr>
<tr>
<td>00</td>
<td>1011</td>
<td>2</td>
<td>V</td>
</tr>
<tr>
<td>00</td>
<td>1100</td>
<td>2.083</td>
<td>V</td>
</tr>
<tr>
<td>00</td>
<td>1101</td>
<td>2.167</td>
<td>V</td>
</tr>
<tr>
<td>00</td>
<td>1110</td>
<td>2.25</td>
<td>V</td>
</tr>
<tr>
<td>00</td>
<td>1111</td>
<td>2.333</td>
<td>V</td>
</tr>
<tr>
<td>01</td>
<td>0000</td>
<td>1.3</td>
<td>V</td>
</tr>
<tr>
<td>01</td>
<td>0001</td>
<td>1.4</td>
<td>V</td>
</tr>
<tr>
<td>01</td>
<td>0010</td>
<td>1.5</td>
<td>V</td>
</tr>
<tr>
<td>01</td>
<td>0011</td>
<td>1.6</td>
<td>V</td>
</tr>
<tr>
<td>01</td>
<td>0100</td>
<td>1.7</td>
<td>V</td>
</tr>
<tr>
<td>01</td>
<td>0101</td>
<td>1.8</td>
<td>V</td>
</tr>
<tr>
<td>01</td>
<td>0110</td>
<td>1.9</td>
<td>V</td>
</tr>
<tr>
<td>SYS_SEL</td>
<td>SYS_VOUT</td>
<td>TYP</td>
<td>UNIT</td>
</tr>
<tr>
<td>---------</td>
<td>----------</td>
<td>------</td>
<td>------</td>
</tr>
<tr>
<td>01</td>
<td>0111</td>
<td>2</td>
<td>V</td>
</tr>
<tr>
<td>01</td>
<td>1000</td>
<td>2.1</td>
<td>V</td>
</tr>
<tr>
<td>01</td>
<td>1001</td>
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<td>V</td>
</tr>
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<tr>
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<td>V</td>
</tr>
<tr>
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<td>1110</td>
<td>2.7</td>
<td>V</td>
</tr>
<tr>
<td>01</td>
<td>1111</td>
<td>2.8</td>
<td>V</td>
</tr>
<tr>
<td>10</td>
<td>0000</td>
<td>1.5</td>
<td>V</td>
</tr>
<tr>
<td>10</td>
<td>0001</td>
<td>1.583</td>
<td>V</td>
</tr>
<tr>
<td>10</td>
<td>0010</td>
<td>1.667</td>
<td>V</td>
</tr>
<tr>
<td>10</td>
<td>0011</td>
<td>1.75</td>
<td>V</td>
</tr>
<tr>
<td>10</td>
<td>0100</td>
<td>1.833</td>
<td>V</td>
</tr>
<tr>
<td>10</td>
<td>0101</td>
<td>1.917</td>
<td>V</td>
</tr>
<tr>
<td>10</td>
<td>0110</td>
<td>2</td>
<td>V</td>
</tr>
<tr>
<td>10</td>
<td>0111</td>
<td>2.083</td>
<td>V</td>
</tr>
<tr>
<td>10</td>
<td>1000</td>
<td>2.167</td>
<td>V</td>
</tr>
<tr>
<td>10</td>
<td>1001</td>
<td>2.25</td>
<td>V</td>
</tr>
<tr>
<td>10</td>
<td>1010</td>
<td>2.333</td>
<td>V</td>
</tr>
<tr>
<td>10</td>
<td>1011</td>
<td>2.417</td>
<td>V</td>
</tr>
<tr>
<td>10</td>
<td>1100</td>
<td>2.5</td>
<td>V</td>
</tr>
<tr>
<td>10</td>
<td>1101</td>
<td>2.583</td>
<td>V</td>
</tr>
<tr>
<td>10</td>
<td>1110</td>
<td>2.667</td>
<td>V</td>
</tr>
<tr>
<td>10</td>
<td>1111</td>
<td>2.75</td>
<td>V</td>
</tr>
<tr>
<td>11</td>
<td>0000</td>
<td>1.8</td>
<td>V</td>
</tr>
<tr>
<td>11</td>
<td>0001</td>
<td>1.9</td>
<td>V</td>
</tr>
<tr>
<td>11</td>
<td>0010</td>
<td>2</td>
<td>V</td>
</tr>
<tr>
<td>11</td>
<td>0011</td>
<td>2.1</td>
<td>V</td>
</tr>
<tr>
<td>11</td>
<td>0100</td>
<td>2.2</td>
<td>V</td>
</tr>
<tr>
<td>11</td>
<td>0101</td>
<td>2.3</td>
<td>V</td>
</tr>
<tr>
<td>11</td>
<td>0110</td>
<td>2.4</td>
<td>V</td>
</tr>
<tr>
<td>11</td>
<td>0111</td>
<td>2.5</td>
<td>V</td>
</tr>
<tr>
<td>11</td>
<td>1000</td>
<td>2.6</td>
<td>V</td>
</tr>
<tr>
<td>11</td>
<td>1001</td>
<td>2.7</td>
<td>V</td>
</tr>
<tr>
<td>11</td>
<td>1010</td>
<td>2.8</td>
<td>V</td>
</tr>
<tr>
<td>11</td>
<td>1011</td>
<td>2.9</td>
<td>V</td>
</tr>
<tr>
<td>11</td>
<td>1100</td>
<td>3</td>
<td>V</td>
</tr>
<tr>
<td>11</td>
<td>1101</td>
<td>3.1</td>
<td>V</td>
</tr>
<tr>
<td>11</td>
<td>1110</td>
<td>3.2</td>
<td>V</td>
</tr>
<tr>
<td>11</td>
<td>1111</td>
<td>3.3</td>
<td>V</td>
</tr>
</tbody>
</table>
9.6.8 Load Switch and LDO Control Register

Memory location 0x07h, Reset State: 0111 110x (bq25120)

**Figure 30. Load Switch and LDO Control Register**

<table>
<thead>
<tr>
<th>7 (MSB)</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0 (LSB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/R</td>
</tr>
</tbody>
</table>

**LEGEND:** R/W = Read/Write; R = Read only; -n = value after reset

**Table 20. Load Switch and LDO Control Register**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>B7</td>
<td>EN_LS_LDO</td>
<td>R/W</td>
<td>0</td>
<td>0 – Disable LS/LDO 1 – Enable LS/LDO</td>
</tr>
<tr>
<td>B6</td>
<td>LS_LDO_4</td>
<td>R/W</td>
<td>1</td>
<td>LS/LDO Voltage: 1600 mV</td>
</tr>
<tr>
<td>B5</td>
<td>LS_LDO_3</td>
<td>R/W</td>
<td>1</td>
<td>LS/LDO Voltage: 800 mV</td>
</tr>
<tr>
<td>B4</td>
<td>LS_LDO_2</td>
<td>R/W</td>
<td>1</td>
<td>LS/LDO Voltage: 400 mV</td>
</tr>
<tr>
<td>B3</td>
<td>LS_LDO_1</td>
<td>R/W</td>
<td>1</td>
<td>LS/LDO Voltage: 200 mV</td>
</tr>
<tr>
<td>B2</td>
<td>LS_LDO_0</td>
<td>R/W</td>
<td>1</td>
<td>LS/LDO Voltage: 100 mV</td>
</tr>
<tr>
<td>B1</td>
<td>MRRESET_VIN</td>
<td>R/W</td>
<td>x</td>
<td>0 – Reset sent when MR Reset time is met 1 – Reset sent when MR Reset time is met and V_{UVLO} + V_{SLP} &lt; V_{OVP}</td>
</tr>
</tbody>
</table>

**LS_LDO Bits:** Use LS_LDO bits to set the LS/LDO output. The LS/LDO voltage is calculated using the following equation: LS/LDO = 0.8 V + LS_LDO_CODE x 100 mV. If a value greater than 3.3 V is written, the setting goes to pass-through mode where LS/LDO = VINLS - V_{DROPOUT}. The LS_LDO output can only be changed when the EN_LS_LDO and LSCTRL pin has disabled the output.
### 9.6.9 Push-button Control Register

Memory location 0x08h, Reset State: 0110 10xx (bq25120)

**Figure 31. Push-button Control Register**

<table>
<thead>
<tr>
<th>7 (MSB)</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0 (LSB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R</td>
</tr>
</tbody>
</table>

**Table 21. Push-button Control Register**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>B7 (MSB)</td>
<td>MRWAKE1</td>
<td>R/W</td>
<td>0</td>
<td>Timer adjustment for WAKE1: 0 – 50 ms &lt; MR, 1 – 500 ms &lt; MR</td>
</tr>
<tr>
<td>B6</td>
<td>MRWAKE2</td>
<td>R/W</td>
<td>1</td>
<td>Timer adjustment for WAKE2: 0 – 1000 ms &lt; MR, 1 – 1500 ms &lt; MR</td>
</tr>
<tr>
<td>B5</td>
<td>MRREC</td>
<td>R/W</td>
<td>1</td>
<td>0 – After Reset, device enters Ship mode, 1 – After Reset, device enters Hi-Z Mode</td>
</tr>
<tr>
<td>B4</td>
<td>MRRESET_1</td>
<td>R/W</td>
<td>0</td>
<td>Timer adjustment for reset: 00 – 4 s ± 10%, 01 – 8 s ± 10%, 10 – 10 s ± 10%, 11 – 14 s ± 10%</td>
</tr>
<tr>
<td>B3</td>
<td>MRRESET_0</td>
<td>R/W</td>
<td>1</td>
<td>Timer adjustment for reset: 00 – 4 s ± 10%, 01 – 8 s ± 10%, 10 – 10 s ± 10%, 11 – 14 s ± 10%</td>
</tr>
<tr>
<td>B2</td>
<td>PGB_MR</td>
<td>R/W</td>
<td>0</td>
<td>0 – Output functions as PG, 1 – Output functions as voltage shifted push-button (MR) input</td>
</tr>
<tr>
<td>B1</td>
<td>WAKE1</td>
<td>R</td>
<td>x</td>
<td>1 – WAKE1 status. Indicates when the device meets the WAKE1 conditions, and is cleared after I^2C read.</td>
</tr>
<tr>
<td>B0 (LSB)</td>
<td>WAKE2</td>
<td>R</td>
<td>x</td>
<td>1 – WAKE2 status. Indicates when the device meets the WAKE2 conditions, and is cleared after I^2C read.</td>
</tr>
</tbody>
</table>

**LEGEND:** R/W = Read/Write; R = Read only; -n = value after reset.
9.6.10 ILIM and Battery UVLO Control Register

Memory location 0x09h, Reset State: 0000 1010 (bq25120)

![Figure 32. ILIM and Battery UVLO Control Register](image)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>B7 (MSB)</td>
<td>RESET</td>
<td>Write only</td>
<td>0</td>
<td>Write: 1 – Reset all registers to default values 0 – No effect  Read: Always get 0</td>
</tr>
<tr>
<td>B6</td>
<td>R/W</td>
<td></td>
<td>0</td>
<td>N/A</td>
</tr>
<tr>
<td>B5</td>
<td>INLIM_2</td>
<td>R/W</td>
<td>0</td>
<td>Input Current Limit: 200 mA</td>
</tr>
<tr>
<td>B4</td>
<td>INLIM_1</td>
<td>R/W</td>
<td>0</td>
<td>Input Current Limit: 100 mA</td>
</tr>
<tr>
<td>B3</td>
<td>INLIM_0</td>
<td>R/W</td>
<td>1</td>
<td>Input Current Limit: 50 mA</td>
</tr>
<tr>
<td>B2</td>
<td>BUVLO_2</td>
<td>R/W</td>
<td>0</td>
<td>000, 001, 010: BUVLO = 3 V 011: BUVLO = 2.8 V 100: BUVLO = 2.6 V</td>
</tr>
<tr>
<td>B1</td>
<td>BUVLO_1</td>
<td>R/W</td>
<td>1</td>
<td>101: BUVLO = 2.4 V 110: BUVLO = 2.2 V 111: BUVLO = Disabled</td>
</tr>
<tr>
<td>B0 (LSB)</td>
<td>BUVLO_0</td>
<td>R/W</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

INLIM Bits: Use INLIM bits to set the input current limit. The \( I_{(INLIM)} \) is calculated using the following equation: \( I_{(INLIM)} = 50 \text{ mA} + I_{(INLIM, CODE)} \times 50 \text{ mA} \). The default is programmed by the external resistor on ILIM, or if not populated and tied to GND, by OTP.

9.6.11 Voltage Based Battery Monitor Register

Memory location 0x0Ah, Reset State: 0xxx xxxx (bq25120)

![Figure 33. Voltage Based Battery Monitor Register](image)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>B7 (MSB)</td>
<td>VBMON_READ</td>
<td>R/W</td>
<td>0</td>
<td>Write 1 to initiate a new VBATREG reading. Read always 0.</td>
</tr>
<tr>
<td>B6</td>
<td>VBMON_RANGE_1</td>
<td>R</td>
<td>x</td>
<td>11 – 90% to 100% of VBATREG</td>
</tr>
<tr>
<td>B5</td>
<td>VBMON_RANGE_0</td>
<td>R</td>
<td>x</td>
<td>10 – 80% to 90% of VBATREG</td>
</tr>
<tr>
<td>B4</td>
<td>VBMON_TH_2</td>
<td>R</td>
<td>x</td>
<td>01 – 70% to 80% of VBATREG</td>
</tr>
<tr>
<td>B3</td>
<td>VBMON_TH_1</td>
<td>R</td>
<td>x</td>
<td>00 – 60% to 70% of VBATREG</td>
</tr>
<tr>
<td>B2</td>
<td>VBMON_TH_0</td>
<td>R</td>
<td>x</td>
<td>111 – Above 8% of VBMON_RANGE</td>
</tr>
<tr>
<td>B1</td>
<td>R</td>
<td>x</td>
<td>N/A</td>
<td></td>
</tr>
<tr>
<td>B0 (LSB)</td>
<td>R</td>
<td>x</td>
<td>N/A</td>
<td></td>
</tr>
</tbody>
</table>

The VBMON registers are used to determine the battery voltage. Before entering a low power state, the device will determine the voltage level by starting at VBMON_RANGE 11 (90% to 100%), and if VBMON_TH of 000 is read, then it will move to VBMON_RANGE 10 (80% to 90%) and continue until a non 000 value of VBMON_TH is found. If this does not happen, then VBMON_RANGE and VBMON_TH will be written with 00 000. The VBMON_READ bit can be used to initiate a new reading by writing a 1 to it. Example: A reading of 10 011 indicated a VBAT voltage of between 84% and 86% of the VBATREG setting.
9.6.12 **VIN_DPM and Timers Register**

Memory location 0x0Bh, Reset State: 0100 1010 (bq25120)

**Figure 34. VIN_DPM and Timers Register**

<table>
<thead>
<tr>
<th>7 (MSB)</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0 (LSB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
</tr>
</tbody>
</table>

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 24. VIN_DPM and Timers Register**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>B7 (MSB)</td>
<td>VINDPM_ON</td>
<td>R/W</td>
<td>0</td>
<td>0 - enable VINDPM</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 - disable VINDPM</td>
</tr>
<tr>
<td>B6</td>
<td>VINDPM_2</td>
<td>R/W</td>
<td>1</td>
<td>Input V_{IN,DPM} voltage: 400 mV</td>
</tr>
<tr>
<td>B5</td>
<td>VINDPM_1</td>
<td>R/W</td>
<td>0</td>
<td>Input V_{IN,DPM} voltage: 200 mV</td>
</tr>
<tr>
<td>B4</td>
<td>VINDPM_0</td>
<td>R/W</td>
<td>0</td>
<td>Input V_{IN,DPM} voltage: 100 mV</td>
</tr>
<tr>
<td>B3</td>
<td>2XTMR_EN</td>
<td>R/W</td>
<td>1</td>
<td>0 – Timer is not slowed at any time</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 – Timer is slowed by 2x when in any control other than CC or CV</td>
</tr>
<tr>
<td>B2</td>
<td>TMR_1</td>
<td>R/W</td>
<td>0</td>
<td>Safety Timer Time Limit</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>00 – 30 minute fast charge</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>01 – 3 hour fast charge</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10 – 9 hour fast charge</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>11 – Disable safety timers</td>
</tr>
<tr>
<td>B1</td>
<td>TMR_0</td>
<td>R/W</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>B0 (LSB)</td>
<td></td>
<td>0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The VINDPM threshold is set using the following equation: \( \text{VINDPM} = 4.2 + \text{VINDPM_CODE} \times 100 \text{ mV} \)
10 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information
A typical design is shown in Figure 35. This design uses the BQ25120 with external resistors for ILIM, IPRETERM, and ISET. These are not needed if these values are set with a host controller through I2C commands. This design also shows the TS resistors, which is also optional.

When powering up in default mode the battery voltage is the default for the part (4.2 V), the SYS output is the default (1.8 V). External resistors set the charge current to 40 mA, the termination current to 10% (4 mA), and the input current limit to 100 mA. If the I2C interface is used the part goes to the internal default settings until changed by the host.

10.2 Typical Application

Figure 35. Typical Application Circuit
Typical Application (continued)

10.2.1 Design Requirements
This application is for a low power system that has varying loads from less than 10 mA up to 300 mA. It must work with a valid adaptor or USB power input. Below are some of the key components that are needed in normal operation. For this example, the fast charge current is 50 mA, input current limit is 400 mA and the pre-charge and termination current is 10% of the fast charge current.

- Supply voltage = 3.4 V to 20 V
- Fast charge current is default to 10 mA with ISET pin shorted to ground. To program the fast charge current, connect an external resistor from ISET to ground.
- Input current limit is default to 100 mA with ILIM pin shorted to ground. To program the input current limit, connect an external resistor from ILIM to ground.
- Termination current threshold is default to 2 mA with IPRETERM pin shorted to ground. To program the input current limit, connect an external resistor from IPRETERM to ground.
- A 2.2-µH inductor is needed between SW pin and SYS pin for PWM output.
- TS- Battery temperature sense needs a NTC connected on TS pin.

10.2.2 Detailed Design Procedure
See Figure 35 for an example of the application diagram.

10.2.2.1 Default Settings
- Connect ISET, ILIM and IPRETERM pins to ground to program fast charge current to 10mA, input current limit to 100mA and pre-charge/termination current to 2 mA.
- BAT_UVLO = 3 V.
- VSYS = 1.8 V
- LS/LDO is LS
- VBREG = 4.2 V
- VIN_DPM is enabled and VIN_DPM Threshold = 4.6 V.
- Safety Timer = 3 hr
- If the function is not needed, connect TS to the center tab of the resistor divider between VIN and the ground. (pull up resistor = 14 kΩ, pull down resistor = 14.3 kΩ)

10.2.2.2 Choose the Correct Inductance and Capacitance
Refer to the Buck (PWM) Output section for the detailed procedure to determine the optimal inductance and capacitance for the buck output.

10.2.2.3 Calculations

10.2.2.3.1 Program the Fast Charge Current (ISET)

\[
R_{ISET} = \frac{K_{ISET}}{I_{CHG}}
\]  

\[
K_{ISET} = 200 \text{ A} \Omega \text{ from the Specifications table}
\]  

\[
R_{ISET} = 200 \text{ A} \Omega / 0.05\text{A} = 4 \text{ kΩ}
\]  

Select the closest standard value, which in this case is 4.99 kΩ. Connect this resistor between ISET pin and GND.

10.2.2.3.2 Program the Input Current Limit (ILIM)

\[
R_{ILIM} = \frac{K_{ILIM}}{I_{MAX}}
\]  

\[
K_{ILIM} = 200 \text{ A} \Omega \text{ from the Specifications table}
\]  

\[
R_{ILIM} = 200 \text{ A} \Omega / 0.4\text{A} = 500 \text{ Ω}
\]  

Select the closest standard value, which in this case is 499 Ω. Connect this resistor between ILIM pin and GND.
Typical Application (continued)

10.2.2.3.3 Program the Pre-charge/termination Threshold (IPRETERM)

According to Table 3, the RIPRETERM is 4990 Ω for 10% termination threshold. Therefore, connect a 4.99 kΩ resistor between IPRETERM pin and GND.

10.2.2.3.4 TS Resistors (TS)

The voltage at TS is monitored to determine that the battery is at a safe temperature during charging. This device uses JEITA temperature profile which has four temperature thresholds. Refer to Specifications for the detailed thresholds number.

The TS circuit is shown in Figure 16. The resistor values can be calculated using Equation 1 and Equation 2.
Typical Application (continued)

10.2.3 Application Performance Curves

10.2.3.1 Charger Curves

Figure 36. Battery Connected to $V_{(BAT)}$

Figure 37. Power Supply Connected to $V_{IN}$

Figure 38. Entering DPPM Mode

Figure 39. Exiting DPPM Mode

Figure 40. Entering Battery Supplement Mode

Figure 41. Exiting Battery Supplement Mode
Typical Application (continued)

**Figure 42. Charger On/Off Using CD**

**Figure 43. OVP Fault**
Typical Application (continued)

10.2.3.2 SYS Output Curves

![Efficiency vs Load Current graph for 1.2 V SYS](image1)

Figure 44. 1.2 V<sub>SYS</sub> System Efficiency

![Efficiency vs Load Current graph for 1.5 V SYS](image2)

Figure 45. 1.5 V<sub>SYS</sub> System Efficiency

![Efficiency vs Load Current graph for 1.8 V SYS](image3)

Figure 46. 1.8 V<sub>SYS</sub> System Efficiency

![Efficiency vs Load Current graph for 2.5 V SYS](image4)

Figure 47. 2.5 V<sub>SYS</sub> System Efficiency

![Efficiency vs Load Current graph for 3.3 V SYS](image5)

Figure 48. 3.3 V<sub>SYS</sub> System Efficiency

![Load Regulation graph for 1.2 V SYS](image6)

Figure 49. 1.2 V<sub>SYS</sub> Load Regulation
Typical Application (continued)

Figure 50. 1.5 \( \text{V}_{\text{SYS}} \) Load Regulation

Figure 51. 1.8 \( \text{V}_{\text{SYS}} \) Load Regulation

Figure 52. 2.5 \( \text{V}_{\text{SYS}} \) Load Regulation

Figure 53. 3.3 \( \text{V}_{\text{SYS}} \) Load Regulation

Figure 54. 1.2 \( \text{V}_{\text{SYS}} \) Line Regulation

Figure 55. 1.5 \( \text{V}_{\text{SYS}} \) Line Regulation
Typical Application (continued)

**Figure 56. 1.8 V\textsubscript{SYS} Line Regulation**

**Figure 57. 2.1 V\textsubscript{SYS} Line Regulation**

**Figure 58. 3.3 V\textsubscript{SYS} Line Regulation**

**Figure 59. 1.8 V\textsubscript{SYS} Switching Frequency vs Load Current**

**Figure 60. Light Load Operation Showing SW**

**Figure 61. Light Load Operation Showing SW**
Typical Application (continued)

\[ I_{LOAD} = \text{1 mA} \]

Figure 62. Light Load Operation Showing SW

\[ I_{LOAD} = \text{10 mA} \]

Figure 63. Light Load Operation Showing SW

\[ I_{LOAD} = \text{100 mA} \]

Figure 64. Light Load Operation Showing SW

\[ I_{LOAD} = \text{200 mA} \]

Figure 65. Light Load Operation Showing SW

\[ I_{LOAD} = \text{300 mA} \]

Figure 66. Light Load Operation Showing SW

\[ V_{SYS} = \text{1.2 V} \]

Figure 67. 1.2 V_{SYS} Load Transient, 0 to 50 mA
Typical Application (continued)

Figure 68. 1.8 $V_{SYS}$ Load Transient, 0 to 50 mA

Figure 69. 2.1 $V_{SYS}$ Load Transient, 0 to 50 mA

Figure 70. 2.5 $V_{SYS}$ Load Transient, 0 to 50 mA

Figure 71. 3.3 $V_{SYS}$ Load Transient, 0 to 50 mA

Figure 72. 1.2 $V_{SYS}$ Load Transient, 0 to 200 mA

Figure 73. 1.8 $V_{SYS}$ Load Transient, 0 to 200 mA
Typical Application (continued)

V_{SYS} = 2.1 \text{ V}

**Figure 74. 2.1 V_{SYS} Load Transient, 0 to 200 mA**

V_{SYS} = 2.5 \text{ V}

**Figure 75. 2.5 V_{SYS} Load Transient, 0 to 200 mA**

V_{SYS} = 3.3 \text{ V}

**Figure 76. 3.3 V_{SYS} Load Transient, 0 to 200 mA**

**Figure 77. Startup Showing SS on SYS in PWM Mode**

**Figure 78. Short Circuit and Recovery for SYS**
Typical Application (continued)

10.2.3.3 Load Switch and LDO Curves

Figure 79. Short Circuit and Recovery for LS

![Short Circuit and Recovery for LS](image)

Figure 80. Startup Showing SS on LS/LDO Output

![Startup Showing SS on LS/LDO Output](image)

V_{LSLDO} = 0.8 V

Figure 81. 0.8 V_{LSLDO} Load Transient, 0 to 10 mA

![0.8 V_{LSLDO} Load Transient, 0 to 10 mA](image)

V_{LSLDO} = 1.2 V

Figure 82. 1.2 V_{LSLDO} Load Transient, 0 to 10 mA

![1.2 V_{LSLDO} Load Transient, 0 to 10 mA](image)

V_{LSLDO} = 1.8 V

Figure 83. 1.8 V_{LSLDO} Load Transient, 0 to 10 mA

![1.8 V_{LSLDO} Load Transient, 0 to 10 mA](image)

V_{LSLDO} = 2.5 V

Figure 84. 2.5 V_{LSLDO} Load Transient, 0 to 10 mA

![2.5 V_{LSLDO} Load Transient, 0 to 10 mA](image)
Typical Application (continued)

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Figure</th>
<th>Load Transient, 0 to 10 mA</th>
<th>Load Transient, 0 to 100 mA</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3 V</td>
<td>Figure 85</td>
<td>3.3 V LSLDO Load Transient</td>
<td>0 to 10 mA</td>
</tr>
<tr>
<td>0.8 V</td>
<td>Figure 86</td>
<td>0.8 V LSLDO Load Transient</td>
<td>0 to 100 mA</td>
</tr>
<tr>
<td>1.2 V</td>
<td>Figure 87</td>
<td>1.2 V LSLDO Load Transient</td>
<td>0 to 100 mA</td>
</tr>
<tr>
<td>1.8 V</td>
<td>Figure 88</td>
<td>1.8 V LSLDO Load Transient</td>
<td>0 to 100 mA</td>
</tr>
<tr>
<td>2.5 V</td>
<td>Figure 89</td>
<td>2.5 V LSLDO Load Transient</td>
<td>0 to 100 mA</td>
</tr>
<tr>
<td>3.3 V</td>
<td>Figure 90</td>
<td>3.3 V LSLDO Load Transient</td>
<td>0 to 100 mA</td>
</tr>
</tbody>
</table>
 Typical Application (continued)

10.2.3.4  LS/LDO Output Curves

![Figure 91. Startup Showing SS on LS/LDO in LDO Mode](image1)

![Figure 92. Short Circuit and Recovery for LDO](image2)
Typical Application (continued)

10.2.3.5 Timing Waveforms Curves

Figure 93. Show \( \overline{PG} \) and \( \overline{INT} \) Timing (ViN Insertion)

Figure 94. Show \( \overline{PG} \) and \( \overline{INT} \) Timing (ViN Removal)

Figure 95. PG Functions as Shifted MR Output

Figure 96. PG Functions as Shifted MR Output

Figure 97. Show MR Timing

Figure 98. Show MR Timing
Typical Application (continued)

![Figure 99. RESET Timing](image)
RESET = 4 s

![Figure 100. RESET Timing](image)
RESET = 8 s

![Figure 101. RESET Timing](image)
RESET = 14 s

![Figure 102. RESET Timing and Enter Ship Mode](image)

11 Power Supply Recommendations

It is recommended to use a power supply that is capable of delivering 5 V at the input current limit set by the BQ25120.
12 Layout

12.1 Layout Guidelines

- Keep the core components of the system close to each other and the device.
- Keep the PMID, IN, and SYS caps as close to their respective pins as possible. Place the bypass caps for PMID, SYS, and LSLDO close to the pins.
- Place the GNDs of the PMID and IN caps close to each other.
- Don’t route so the power planes are interrupted.

12.2 Layout Example

![bq25120 Layout](image-url)
13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

TI's publication of information regarding third-party products or services does not constitute an endorsement regarding the suitability of such products or services or a warranty, representation or endorsement of such products or services, either alone or in combination with any TI product or service.

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

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<tr>
<th>PARTS</th>
<th>PRODUCT FOLDER</th>
<th>SAMPLE &amp; BUY</th>
<th>TECHNICAL DOCUMENTS</th>
<th>TOOLS &amp; SOFTWARE</th>
<th>SUPPORT &amp; COMMUNITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>BQ25120</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
<tr>
<td>BQ25121</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
</tbody>
</table>

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on "Alert me" to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI’s views; see TI’s Terms of Use.

**TI E2E™ Online Community**  
*TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support**  
*TI's Design Support*  
Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.5 Trademarks

E2E is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.7 Glossary

**SLYZ022 — TI Glossary.**

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>BQ25120YFPR</td>
<td>NRND</td>
<td>DSBGA</td>
<td>YFP</td>
<td>25</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>SNAGCU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>BQ25120</td>
<td></td>
</tr>
<tr>
<td>BQ25120YFPT</td>
<td>NRND</td>
<td>DSBGA</td>
<td>YFP</td>
<td>25</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>SNAGCU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>BQ25120</td>
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<tr>
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<td>DSBGA</td>
<td>YFP</td>
<td>25</td>
<td>3000</td>
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<td>SNAGCU</td>
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<td>BQ25121</td>
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</tr>
<tr>
<td>BQ25121YFPT</td>
<td>NRND</td>
<td>DSBGA</td>
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<td>250</td>
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<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>BQ25121</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE:** Product device recommended for new designs.
- **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead/Ball Finish:** Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
**TAPE AND REEL INFORMATION**

*All dimensions are nominal*

<table>
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<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
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### TAPE AND REEL BOX DIMENSIONS

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*All dimensions are nominal*
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.
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