

TPS77001, TPS77012, TPS77015, TPS77018, TPS77025
 TPS77027, TPS77028, TPS77030, TPS77033, TPS77050
ULTRALOW-POWER 50-mA LOW-DROPOUT LINEAR REGULATORS

SLVS210D – JUNE 1999 – REVISED MAY 2001

- 50-mA Low-Dropout Regulator
- Available in 1.2-V, 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3.0-V, 3.3-V, and 5-V Fixed-Output and Adjustable Versions
- Only 17 μA Quiescent Current at 50 mA
- 1 μA Quiescent Current in Standby Mode
- Dropout Voltage Typically 35 mV at 50 mA
- Over Current Limitation
- -40°C to 125°C Operating Junction Temperature Range
- 5-Pin SOT-23 (DBV) Package



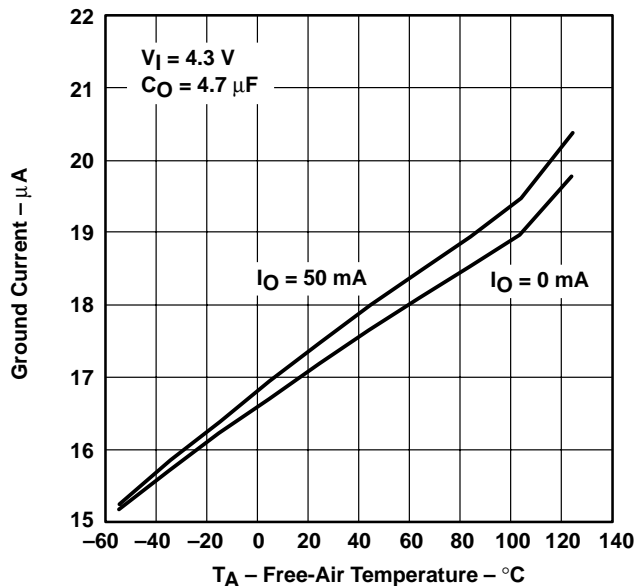
description

The TPS770xx family of low-dropout (LDO) voltage regulators offers the benefits of low dropout voltage, ultralow-power operation, and miniaturized packaging. These regulators feature low dropout voltages and ultralow quiescent current compared to conventional LDO regulators. Offered in a 5-terminal small outline integrated-circuit SOT-23 package, the TPS770xx series devices are ideal for micropower operations and where board space is at a premium.

A combination of new circuit design and process innovation has enabled the usual PNP pass transistor to be replaced by a PMOS pass element. Because the PMOS pass element behaves as a low-value resistor, the dropout voltage is very low — typically 35 mV at 50 mA of load current (TPS77050) — and is directly proportional to the load current. Since the PMOS pass element is a voltage-driven device, the quiescent current is ultralow (28 μA maximum) and is stable over the entire range of output load current (0 mA to 50 mA). Intended for use in portable systems such as laptops and cellular phones, the ultralow-dropout voltage feature and ultralow-power operation result in a significant increase in system battery operating life.

The TPS770xx also features a logic-enabled sleep mode to shut down the regulator, reducing quiescent current to 1 μA typical at $T_J = 25^{\circ}\text{C}$. The TPS770xx is offered in 1.2-V, 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3.0-V, 3.3-V, and 5-V fixed-voltage versions and in a variable version (programmable over the range of 1.2 V to 5.5 V).

TPS77033
 GROUND CURRENT
 vs
 FREE-AIR TEMPERATURE



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2001, Texas Instruments Incorporated

**TPS77001, TPS77012, TPS77015, TPS77018, TPS77025
 TPS77027, TPS77028, TPS77030, TPS77033, TPS77050
 ULTRALOW-POWER 50-mA LOW-DROPOUT LINEAR REGULATORS**

SLVS210D – JUNE 1999 – REVISED MAY 2001

AVAILABLE OPTIONS

T _J	VOLTAGE	PACKAGE	PART NUMBER		SYMBOL
-40°C to 125°C	Variable 1.2V to 5.5V	SOT-23 (DBV)	TPS77001DBVT†	TPS77001DBVR‡	PCPI
	1.2 V		TPS77012DBVT†	TPS77012DBVR‡	PCQI
	1.5 V		TPS77015DBVT†	TPS77015DBVR‡	PCRI
	1.8 V		TPS77018DBVT†	TPS77018DBVR‡	PCSI
	2.5 V		TPS77025DBVT†	TPS77025DBVR‡	PCTI
	2.7 V		TPS77027DBVT†	TPS77027DBVR‡	PCUI
	2.8 V		TPS77028DBVT†	TPS77028DBVR‡	PCVI
	3.0 V		TPS77030DBVT†	TPS77030DBVR‡	PCWI
	3.3 V		TPS77033DBVT†	TPS77033DBVR‡	PCXI
	5.0 V		TPS77050DBVT†	TPS77050DBVR‡	PCYI

† The DBVT indicates tape and reel of 250 parts.

‡ The DBVR indicates tape and reel of 3000 parts.

functional block diagram

TPS77001



TPS77012/15/18/25/27/28/30/33/50



**TPS77001, TPS77012, TPS77015, TPS77018, TPS77025
TPS77027, TPS77028, TPS77030, TPS77033, TPS77050
ULTRALOW-POWER 50-mA LOW-DROPOUT LINEAR REGULATORS**

SLVS210D – JUNE 1999 – REVISED MAY 2001

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
GND	2		Ground
$\overline{\text{EN}}$	3	I	Enable input
FB	4	I	Feedback voltage (TPS77001 only)
IN	1	I	Input supply voltage
NC	4		No connection (Fixed options only)
OUT	5	O	Regulated output voltage

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Input voltage range (see Note 1)	–0.3 V to 13.5 V
Voltage range at EN	–0.3 V to $V_I + 0.3$ V
Voltage on OUT, FB	7 V
Peak output current	Internally limited
ESD rating, HBM	2 kV
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	–40°C to 150°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A \leq 25^\circ\text{C}$ POWER RATING	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
Low K [‡]	DBV	65.8 °C/W	259 °C/W	3.9 mW/°C	386 mW	212 mW	154 mW
High K [§]	DBV	65.8 °C/W	180 °C/W	5.6 mW/°C	555 mW	305 mW	222 mW

[‡] The JEDEC Low K (1s) board design used to derive this data was a 3 inch x 3 inch, two layer board with 2 ounce copper traces on top of the board.

[§] The JEDEC High K (2s2p) board design used to derive this data was a 3 inch x 3 inch, multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Input voltage, V_I (see Note 2)	2.7		10	V
Output voltage range, V_O	1.2		5.5	V
Continuous output current, I_O (see Note 3)	0		50	mA
Operating junction temperature, T_J	–40		125	°C

NOTES: 2. To calculate the minimum input voltage for your maximum output current, use the following formula:

$$V_I(\text{min}) = V_O(\text{max}) + V_{\text{DO}}(\text{max load})$$

3. Continuous output current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.



**TPS77001, TPS77012, TPS77015, TPS77018, TPS77025
 TPS77027, TPS77028, TPS77030, TPS77033, TPS77050
 ULTRALOW-POWER 50-mA LOW-DROPOUT LINEAR REGULATORS**

SLVS210D – JUNE 1999 – REVISED MAY 2001

**electrical characteristics over recommended operating free-air temperature range,
 $V_I = V_O(\text{typ}) + 1 \text{ V}$, $I_O = 50 \text{ mA}$, $\overline{\text{EN}} = 0\text{V}$, $C_O = 4.7 \mu\text{F}$ (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage (10 μA to 50 mA load) (see Note 4)	TPS77001	$1.2 \text{ V} \leq V_O \leq 5.5 \text{ V}$, $T_J = 25^\circ\text{C}$		V_O		
		$1.2 \text{ V} \leq V_O \leq 5.5 \text{ V}$, $T_J = -40^\circ\text{C}$ to 125°C	$0.97V_O$		$1.03V_O$	
	TPS77012	$T_J = 25^\circ\text{C}$, $2.7 \text{ V} < V_{\text{IN}} < 10 \text{ V}$		1.224		
		$T_J = -40^\circ\text{C}$ to 125°C , $2.7 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	1.187		1.261	
	TPS77015	$T_J = 25^\circ\text{C}$, $2.7 \text{ V} < V_{\text{IN}} < 10 \text{ V}$		1.5		
		$T_J = -40^\circ\text{C}$ to 125°C , $2.7 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	1.455		1.545	
	TPS77018	$T_J = 25^\circ\text{C}$, $2.8 \text{ V} < V_{\text{IN}} < 10 \text{ V}$		1.8		
		$T_J = -40^\circ\text{C}$ to 125°C , $2.8 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	1.746		1.854	
	TPS77025	$T_J = 25^\circ\text{C}$, $3.5 \text{ V} < V_{\text{IN}} < 10 \text{ V}$		2.5		
		$T_J = -40^\circ\text{C}$ to 125°C , $3.5 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	2.425		2.575	
	TPS77027	$T_J = 25^\circ\text{C}$, $3.7 \text{ V} < V_{\text{IN}} < 10 \text{ V}$		2.7		
		$T_J = -40^\circ\text{C}$ to 125°C , $3.7 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	2.619		2.781	
	TPS77028	$T_J = 25^\circ\text{C}$, $3.8 \text{ V} < V_{\text{IN}} < 10 \text{ V}$		2.8		
		$T_J = -40^\circ\text{C}$ to 125°C , $3.8 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	2.716		2.884	
	TPS77030	$T_J = 25^\circ\text{C}$, $4.0 \text{ V} < V_{\text{IN}} < 10 \text{ V}$		3.0		
		$T_J = -40^\circ\text{C}$ to 125°C , $4.0 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	2.910		3.090	
	TPS77033	$T_J = 25^\circ\text{C}$, $4.3 \text{ V} < V_{\text{IN}} < 10 \text{ V}$		3.3		
		$T_J = -40^\circ\text{C}$ to 125°C , $4.3 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	3.201		3.399	
TPS77050	$T_J = 25^\circ\text{C}$, $6.0 \text{ V} < V_{\text{IN}} < 10 \text{ V}$		5.0			
	$T_J = -40^\circ\text{C}$ to 125°C , $6.0 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	4.850		5.150		
Quiescent current (GND current) (see Note 4)	$\overline{\text{EN}} = 0\text{V}$, $T_J = 25^\circ\text{C}$ $0 \text{ mA} < I_O < 50\text{mA}$		17		μA	
		$\overline{\text{EN}} = 0\text{V}$, $T_J = -40^\circ\text{C}$ to 125°C $I_O = 50\text{mA}$			28	
Output voltage line regulation ($\Delta V_O/V_O$) (see Notes 4 and 5)	$V_O + 1 \text{ V} < V_I \leq 10 \text{ V}$, $T_J = 25^\circ\text{C}$ $V_O + 1 \text{ V} < V_I \leq 10 \text{ V}$, $T_J = -40^\circ\text{C}$ to 125°C		0.04		$\%/V$	
					0.1	
Load regulation	$\overline{\text{EN}} = 0\text{V}$, $T_J = 25^\circ\text{C}$ $I_O = 0$ to 50 mA		8		mV	
Output noise voltage	$\text{BW} = 300 \text{ Hz}$ to 50 kHz , $C_O = 10 \mu\text{F}$, $T_J = 25^\circ\text{C}$		190		μV_{rms}	
Output current limit	$V_O = 0\text{V}$, See Note 4		350	750	mA	
Standby current	$\overline{\text{EN}} = V_I$, $2.7 < V_I < 10 \text{ V}$ $T_J = -40^\circ\text{C}$ to 125°C		1		μA	
					2	

NOTES: 4. Minimum IN operating voltage is 2.7 V or $V_O(\text{typ}) + 1 \text{ V}$, whichever is greater. Maximum IN voltage 10 V, minimum output current 10 μA , maximum output current 50 mA.

5. If $V_O \leq 1.8 \text{ V}$ then $V_{\text{Imin}} = 2.7 \text{ V}$, $V_{\text{Imax}} = 10 \text{ V}$:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O(V_{\text{Imax}} - 2.7 \text{ V})}{100} \times 1000$$

If $V_O \geq 2.5 \text{ V}$ then $V_{\text{Imin}} = V_O + 1 \text{ V}$, $V_{\text{Imax}} = 10 \text{ V}$:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O(V_{\text{Imax}} - (V_O + 1 \text{ V}))}{100} \times 1000$$



**TPS77001, TPS77012, TPS77015, TPS77018, TPS77025
TPS77027, TPS77028, TPS77030, TPS77033, TPS77050
ULTRALOW-POWER 50-mA LOW-DROPOUT LINEAR REGULATORS**

SLVS210D – JUNE 1999 – REVISED MAY 2001

electrical characteristics over recommended operating free-air temperature range, $V_I = V_O(\text{typ}) + 1\text{ V}$, $I_O = 50\text{ mA}$, $\overline{\text{EN}} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}$ (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FB input current		FB = 1.224 V (TPS77001)		-1		1	μA
High level enable input voltage		$2.7\text{ V} < V_I < 10\text{ V}$		1.7			V
Low level enable input voltage		$2.7\text{ V} < V_I < 10\text{ V}$				0.9	V
Power supply ripple rejection		$f = 1\text{ kHz}$, $T_J = 25^\circ\text{C}$,	$C_O = 10\text{ }\mu\text{F}$, See Note 4		60		dB
Input current (EN)		$\overline{\text{EN}} = 0\text{ V}$		-1	0	1	μA
		$\overline{\text{EN}} = V_I$		-1		1	μA
Dropout voltage (see Note 6)	TPS77028	$I_O = 50\text{ mA}$,	$T_J = 25^\circ\text{C}$		60		mV
		$I_O = 50\text{ mA}$	$T_J = -40^\circ\text{C}$ to 125°C			125	
	TPS77030	$I_O = 50\text{ mA}$,	$T_J = 25^\circ\text{C}$		57		
		$I_O = 50\text{ mA}$	$T_J = -40^\circ\text{C}$ to 125°C			115	
	TPS77033	$I_O = 50\text{ mA}$,	$T_J = 25^\circ\text{C}$		48		
		$I_O = 50\text{ mA}$	$T_J = -40^\circ\text{C}$ to 125°C			100	
	TPS77050	$I_O = 50\text{ mA}$,	$T_J = 25^\circ\text{C}$		35		
		$I_O = 50\text{ mA}$	$T_J = -40^\circ\text{C}$ to 125°C			85	

NOTES: 4. Minimum IN operating voltage is 2.7 V or $V_O(\text{typ}) + 1\text{ V}$, whichever is greater. Maximum IN voltage 10 V, minimum output current 10 μA , maximum output current 50 mA.

6. IN voltage equals $V_O(\text{Typ}) - 100\text{mV}$; TPS77001 output voltage set to 3.3 V nominal with external resistor divider. TPS77012, TPS77015, TPS77018, TPS77025, and TPS77027 dropout voltage limited by input voltage range limitations.

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
V_O	Output voltage	vs Output current
		vs Free-air temperature
	Ground current	vs Free-air temperature
	Output spectral noise density	vs Frequency
Z_O	Output impedance	vs Frequency
V_{DO}	Dropout voltage	vs Free-air temperature
	Ripple rejection	vs Frequency
	LDO startup time	
	Line transient response	
	Load transient response	
	Equivalent series resistance (ESR)	vs Output current
		vs Added ceramic capacitance



TYPICAL CHARACTERISTICS

TPS77025
 OUTPUT VOLTAGE
 vs
 OUTPUT CURRENT

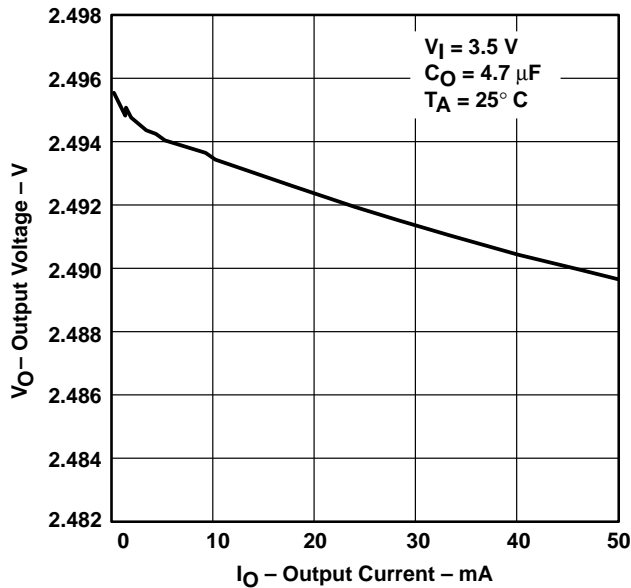


Figure 1

TPS77015
 OUTPUT VOLTAGE
 vs
 OUTPUT CURRENT

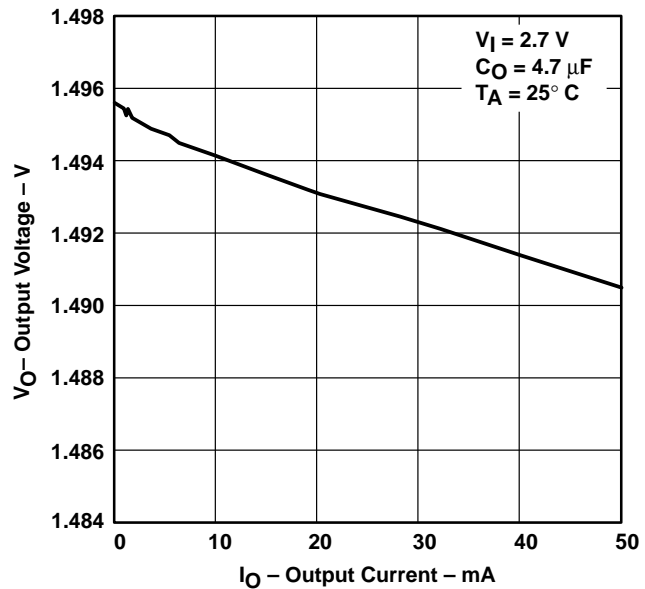


Figure 2

TPS77033
 OUTPUT VOLTAGE
 vs
 OUTPUT CURRENT

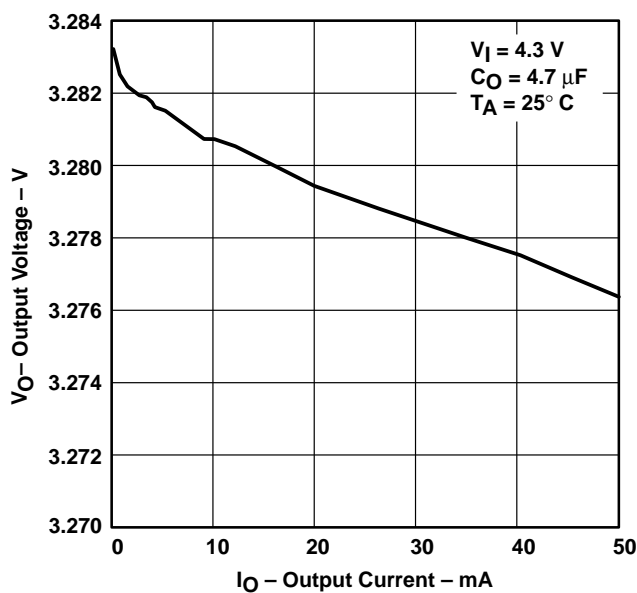


Figure 3

TPS77015
 OUTPUT VOLTAGE
 vs
 FREE-AIR TEMPERATURE

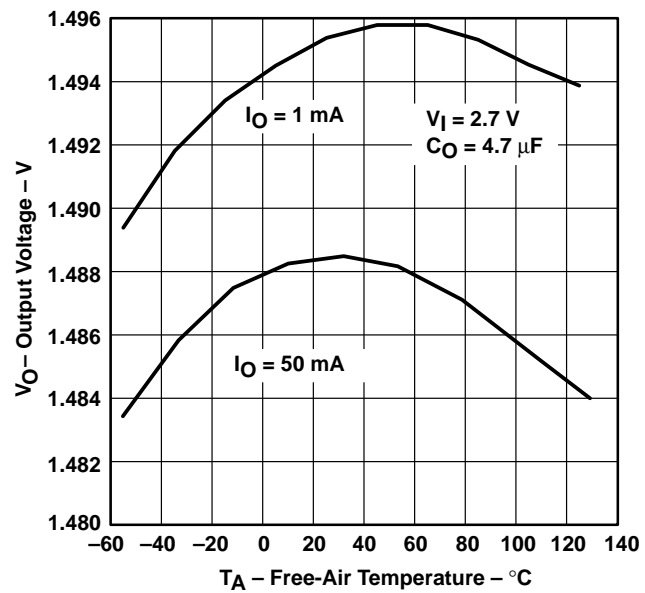


Figure 4

TYPICAL CHARACTERISTICS

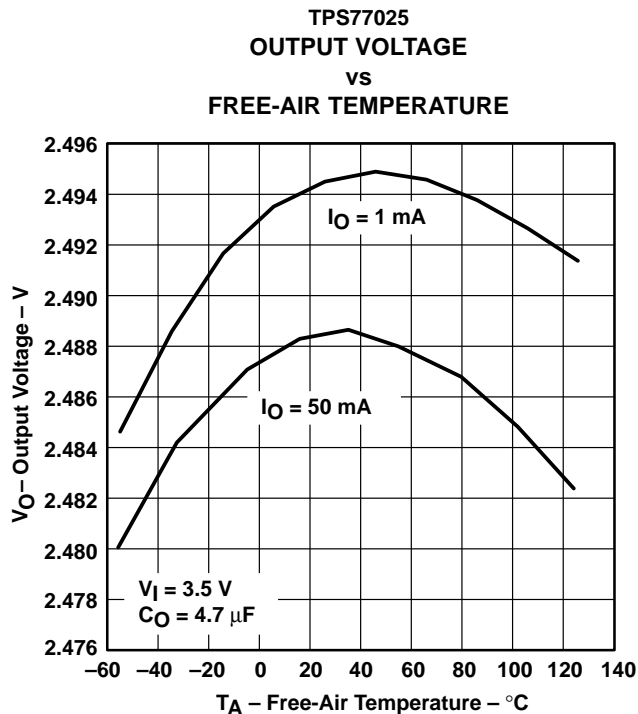


Figure 5

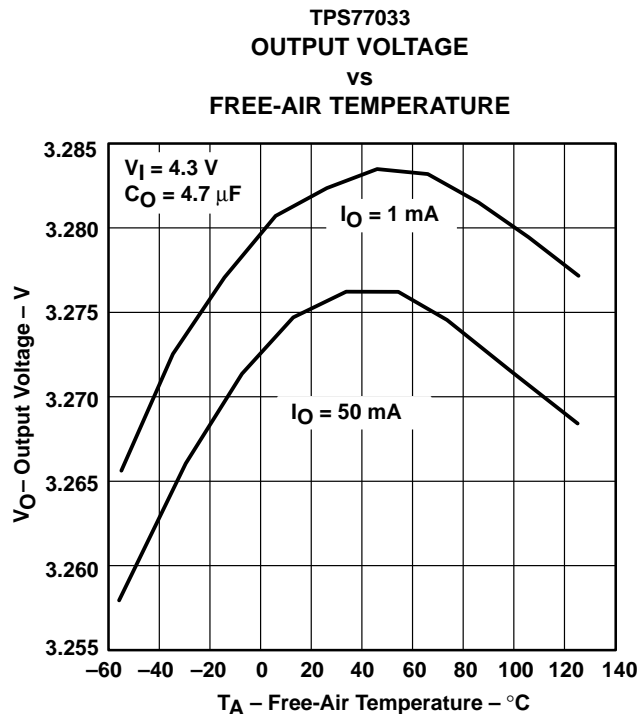


Figure 6

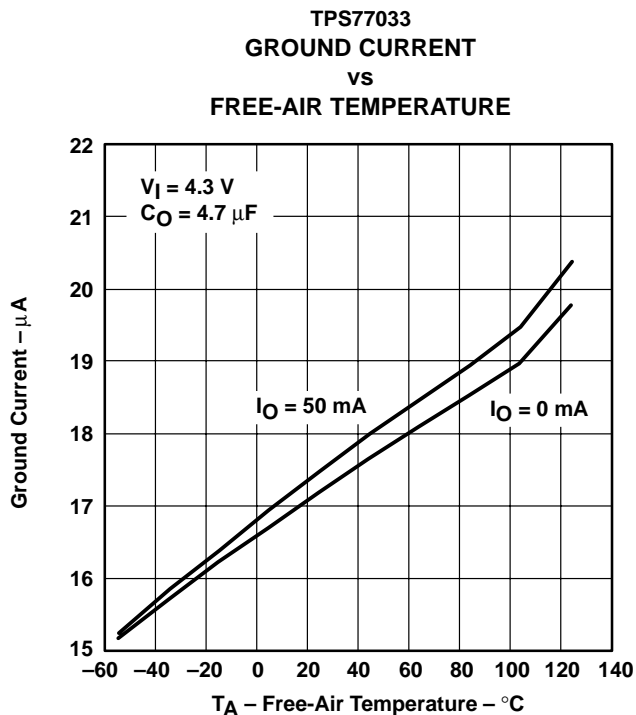


Figure 7

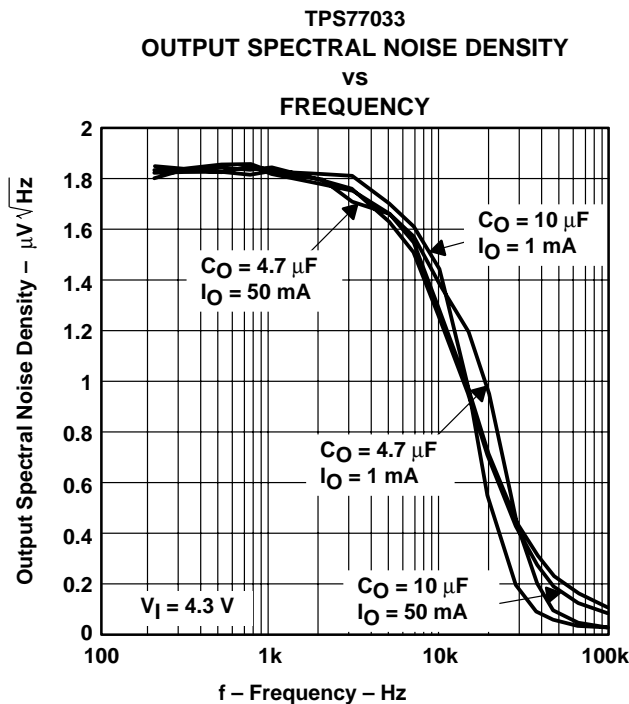


Figure 8

TYPICAL CHARACTERISTICS

OUTPUT IMPEDANCE
 VS
 FREQUENCY

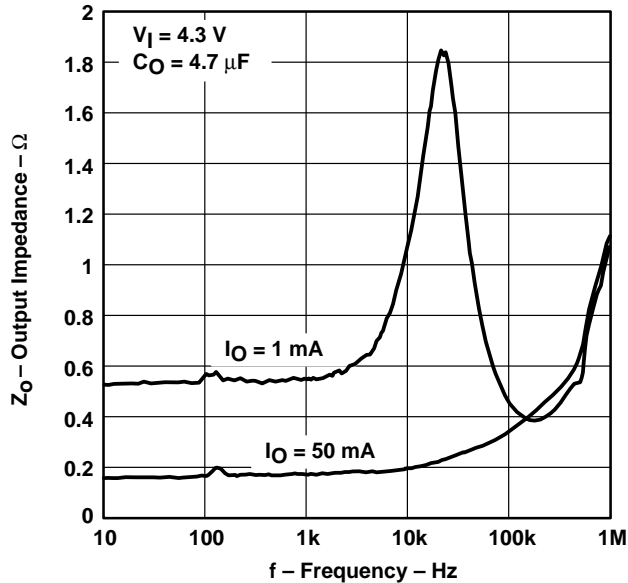


Figure 9

TPS77033
 DROPOUT VOLTAGE
 VS
 FREE-AIR TEMPERATURE

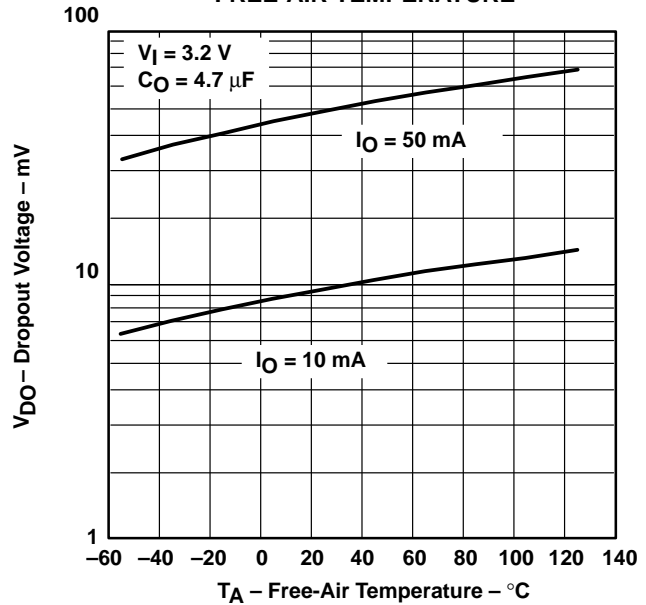


Figure 10

TPS77033
 RIPPLE REJECTION
 VS
 FREQUENCY

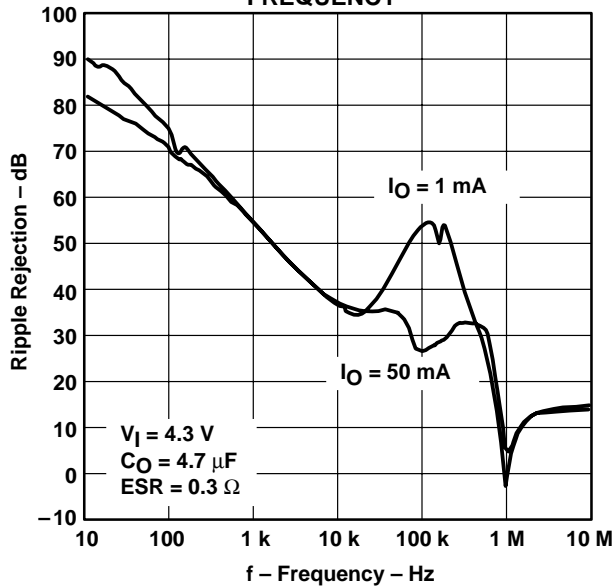


Figure 11

LDO STARTUP TIME

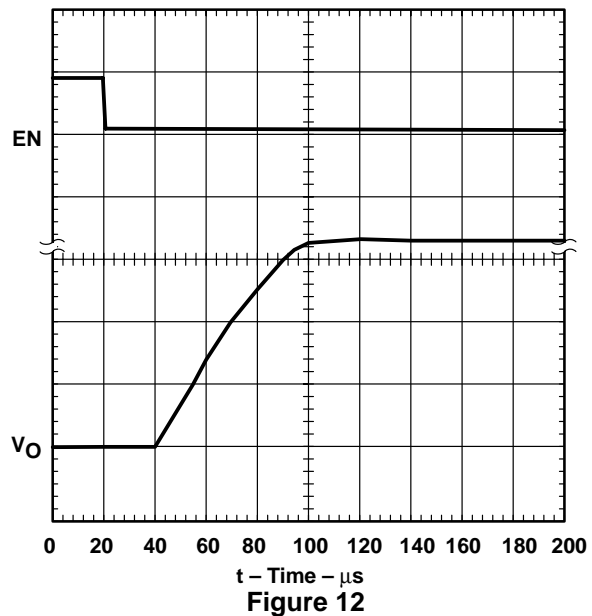


Figure 12

TPS77001, TPS77012, TPS77015, TPS77018, TPS77025
 TPS77027, TPS77028, TPS77030, TPS77033, TPS77050
 ULTRALOW-POWER 50-mA LOW-DROPOUT LINEAR REGULATORS

SLVS210D – JUNE 1999 – REVISED MAY 2001

TYPICAL CHARACTERISTICS

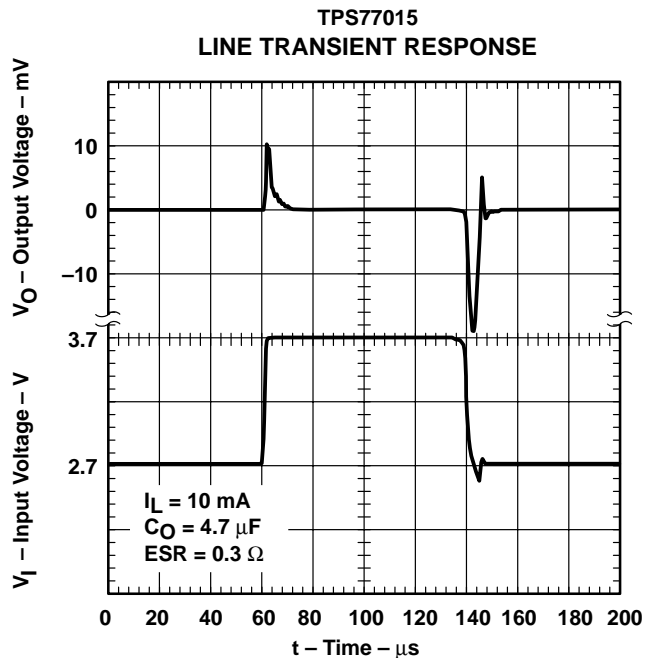


Figure 13

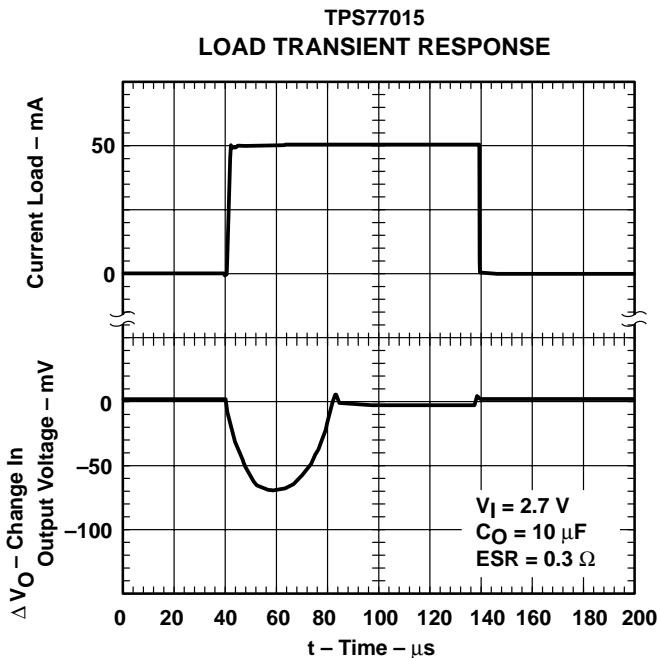


Figure 14

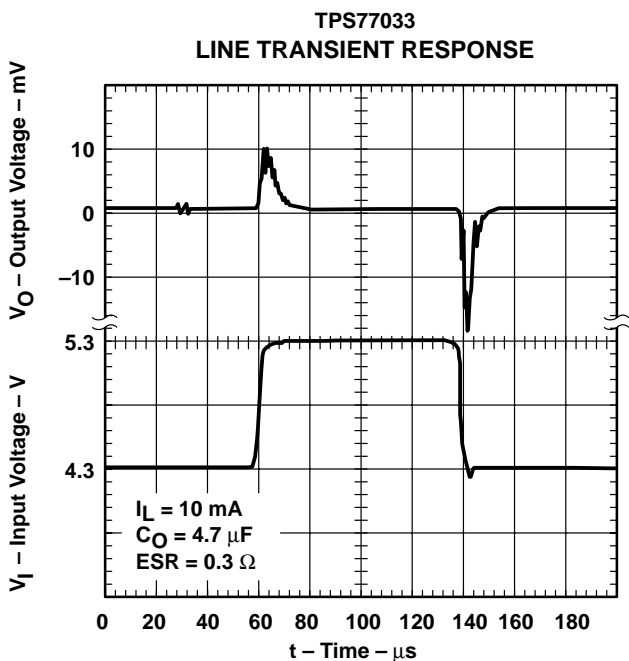


Figure 15

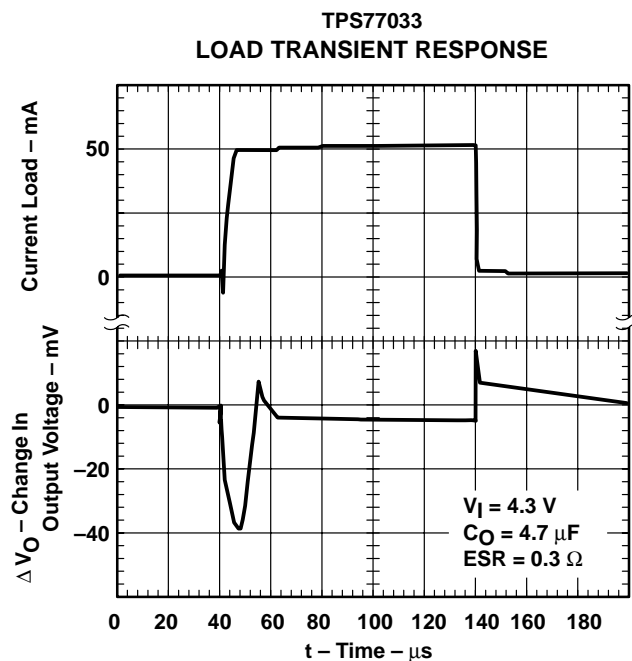


Figure 16

TYPICAL CHARACTERISTICS

TPS77033
 TYPICAL REGIONS OF STABILITY
 EQUIVALENT SERIES RESISTANCE (ESR)[†]
 VS
 OUTPUT CURRENT

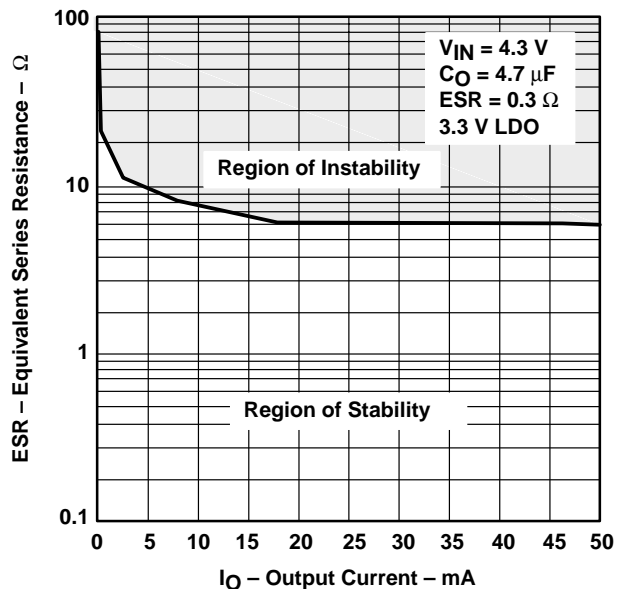


Figure 17

TPS77033
 TYPICAL REGIONS OF STABILITY
 EQUIVALENT SERIES RESISTANCE (ESR)
 VS
 ADDED CERAMIC CAPACITANCE

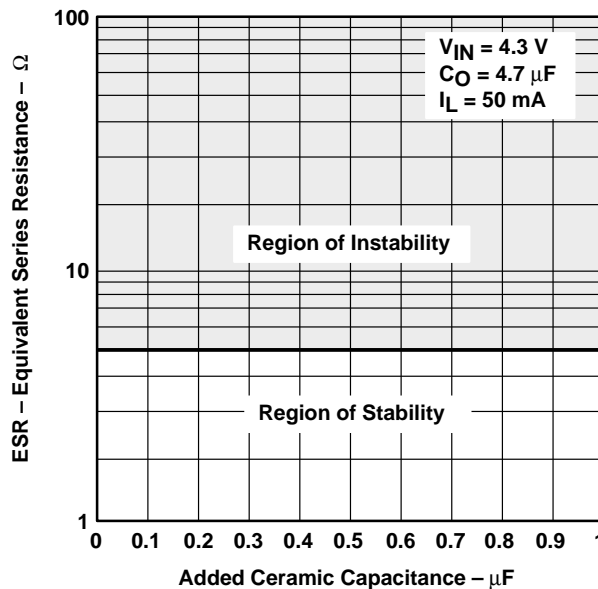


Figure 18

TPS77033
 TYPICAL REGIONS OF STABILITY
 EQUIVALENT SERIES RESISTANCE (ESR)[†]
 VS
 OUTPUT CURRENT

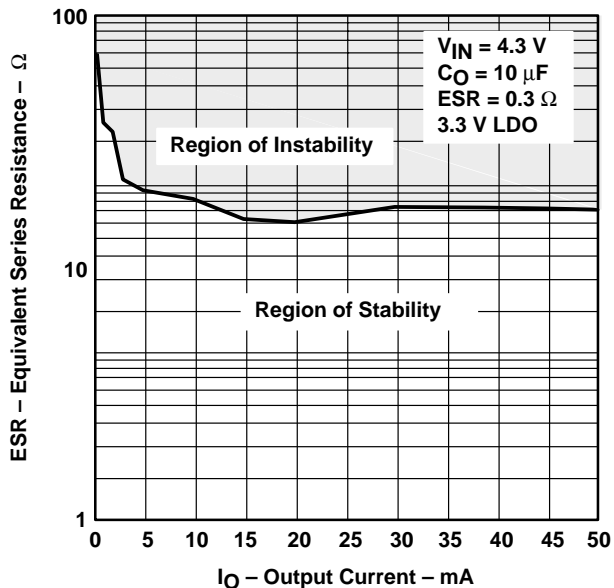


Figure 19

TPS77033
 TYPICAL REGIONS OF STABILITY
 EQUIVALENT SERIES RESISTANCE (ESR)
 VS
 ADDED CERAMIC CAPACITANCE

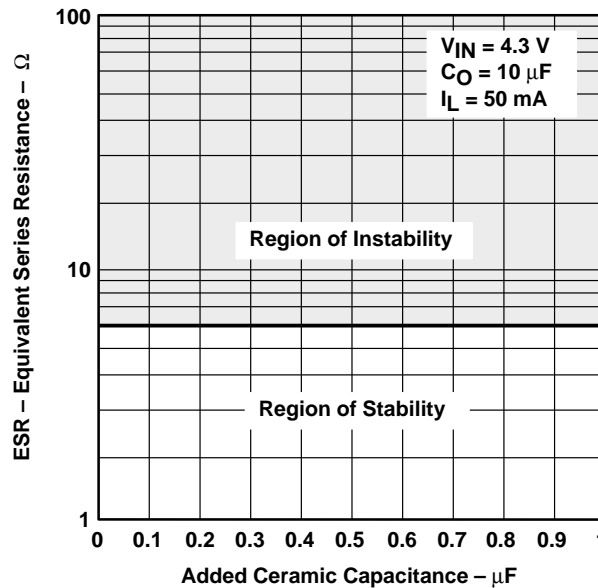


Figure 20

APPLICATION INFORMATION

The TPS770xx family of low-dropout (LDO) regulators have been optimized for use in battery-operated equipment. They feature extremely low dropout voltages, low quiescent current (17 μA nominally), and enable inputs to reduce supply currents to less than 1 μA when the regulators are turned off.

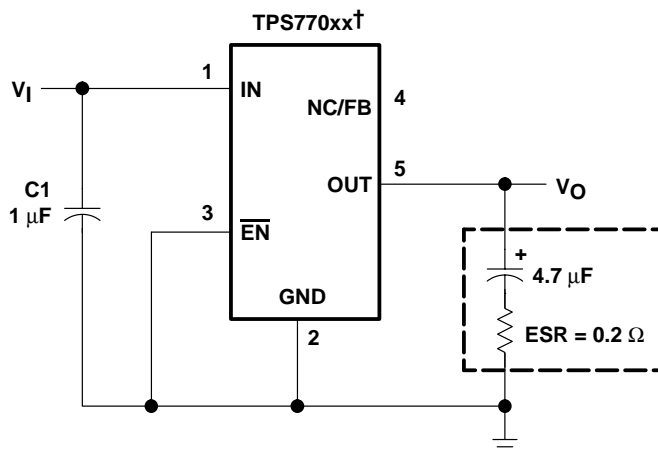
device operation

The TPS770xx uses a PMOS pass element to dramatically reduce both dropout voltage and supply current over more conventional PNP-pass-element LDO designs. The PMOS pass element is a voltage-controlled device and, unlike a PNP transistor, it does not require increased drive current as output current increases. Supply current in the TPS770xx is essentially constant from no load to maximum load.

Current limiting and thermal protection prevent damage by excessive output current and/or power dissipation. The device switches into a constant-current mode at approximately 350 mA; further load reduces the output voltage instead of increasing the output current. The thermal protection shuts the regulator off if the junction temperature rises above approximately 165°C. Recovery is automatic when the junction temperature drops approximately 25°C below the high temperature trip point. The PMOS pass element includes a back gate diode that conducts reverse current when the input voltage level drops below the output voltage level.

A voltage of 1.7 V or greater on the EN input will disable the TPS770xx internal circuitry, reducing the supply current to 1 μA . A voltage of less than 0.9 V on the EN input will enable the TPS770xx and will enable normal operation to resume. The EN input does not include any deliberate hysteresis, and it exhibits an actual switching threshold of approximately 1.5 V.

A typical application circuit is shown in Figure 21.



† TPS77012, TPS77015, TPS77018, TPS77025, TPS77027,
 TPS77028, TPS77030, TPS77033, TPS77050 (fixed-voltage options).

Figure 21. Typical Application Circuit

**TPS77001, TPS77012, TPS77015, TPS77018, TPS77025
TPS77027, TPS77028, TPS77030, TPS77033, TPS77050
ULTRALOW-POWER 50-mA LOW-DROPOUT LINEAR REGULATORS**

SLVS210D – JUNE 1999 – REVISED MAY 2001

APPLICATION INFORMATION

external capacitor requirements

Although not required, a 0.047- μ F or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS770xx, is recommended to improve transient response and noise rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like all low dropout regulators, the TPS770xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 4.7 μ F. The ESR (equivalent series resistance) of the capacitor should be between 0.2 Ω and 10 Ω . to ensure stability. Capacitor values larger than 4.7 μ F are acceptable, and allow the use of smaller ESR values. Capacitances less than 4.7 μ F are not recommended because they require careful selection of ESR to ensure stability. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Most of the commercially available 4.7 μ F surface-mount solid tantalum capacitors, including devices from Sprague, Kemet, and Nichico, meet the ESR requirements stated above. Multilayer ceramic capacitors may have very small equivalent series resistances and may thus require the addition of a low value series resistor to ensure stability.

CAPACITOR SELECTION

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
T494B475K016AS	KEMET	4.7 μ F	1.5 Ω	1.9 × 3.5 × 2.8
195D106x0016x2T	SPRAGUE	10 μ F	1.5 Ω	1.3 × 7.0 × 2.7
695D106x003562T	SPRAGUE	10 μ F	1.3 Ω	2.5 × 7.6 × 2.5
TPSC475K035R0600	AVX	4.7 μ F	0.6 Ω	2.6 × 6.0 × 3.2

† Size is in mm. ESR is maximum resistance in Ohms at 100 kHz and $T_A = 25^\circ\text{C}$. Contact manufacturer for minimum ESR values.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

APPLICATION INFORMATION

output voltage programming

The output voltage of the TPS77001 adjustable regulator is programmed using an external resistor divider as shown in Figure 22. The output voltage is calculated using:

$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \tag{1}$$

where

$$V_{ref} = 1.224 \text{ V typ (the internal reference voltage)}$$

Resistors R1 and R2 should be chosen for approximately 7- μ A divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 169 k Ω to set the divider current at 7 μ A and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \tag{2}$$

**OUTPUT VOLTAGE
PROGRAMMING GUIDE**

OUTPUT VOLTAGE (V)	DIVIDER RESISTANCE (k Ω) [‡]	
	R1	R2
2.5	174	169
3.3	287	169
3.6	324	169
4.0	383	169
5.0	523	169

[‡] 1% values shown.

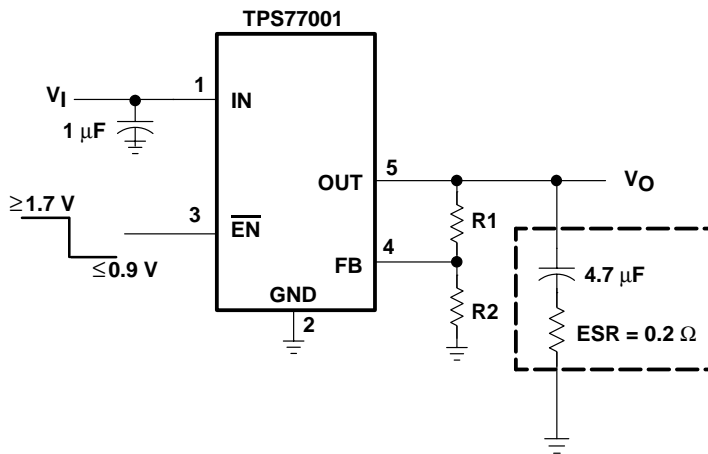


Figure 22. TPS77001 Adjustable LDO Regulator Programming

APPLICATION INFORMATION

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D , which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

Where:

T_{Jmax} is the maximum allowable junction temperature

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, see the dissipation rating table.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = (V_I - V_O) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

regulator protection

The TPS770xx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS770xx features internal current limiting and thermal protection. During normal operation, the TPS770xx limits output current to approximately 350 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds approximately 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below approximately 140°C, regulator operation resumes.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS77001DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		PCPI	Samples
TPS77001DBVT	LIFEBUY	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		PCPI	
TPS77012DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		PCQI	Samples
TPS77012DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		PCQI	Samples
TPS77015DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		PCRI	Samples
TPS77015DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		PCRI	Samples
TPS77018DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		PCSI	Samples
TPS77025DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		PCTI	Samples
TPS77025DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		PCTI	Samples
TPS77027DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		PCUI	Samples
TPS77027DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		PCUI	Samples
TPS77028DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		PCVI	Samples
TPS77030DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		PCWI	Samples
TPS77030DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		PCWI	Samples
TPS77030DBVT	LIFEBUY	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		PCWI	
TPS77030DBVTG4	LIFEBUY	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		PCWI	
TPS77033DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCXI	Samples
TPS77033DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCXI	Samples
TPS77033DBVT	LIFEBUY	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCXI	
TPS77033DBVTG4	LIFEBUY	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PCXI	
TPS77050DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		PCYI	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS77050DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		PCYI	Samples
TPS77050DBVT	LIFEBUY	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		PCYI	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS77001DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS77001DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS77012DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS77012DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS77012DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS77012DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS77015DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS77015DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS77018DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS77025DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS77027DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS77027DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS77028DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS77030DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS77030DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS77033DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS77033DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS77050DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS77050DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS77001DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS77001DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS77012DBVR	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS77012DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS77012DBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
TPS77012DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS77015DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS77015DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS77018DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS77025DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS77027DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS77027DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS77028DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS77030DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS77030DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS77033DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS77033DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS77050DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS77050DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

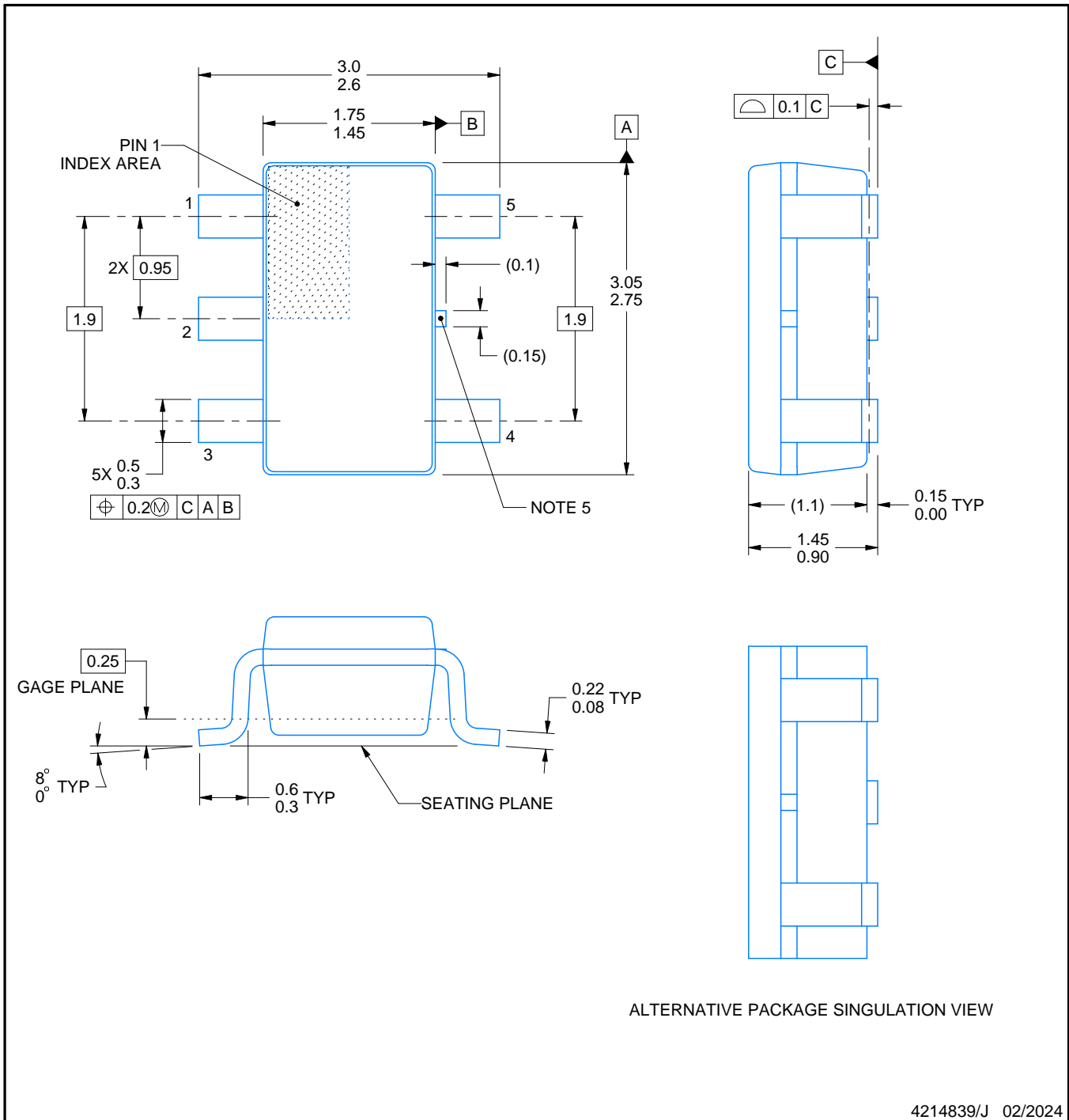
DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/J 02/2024

NOTES:

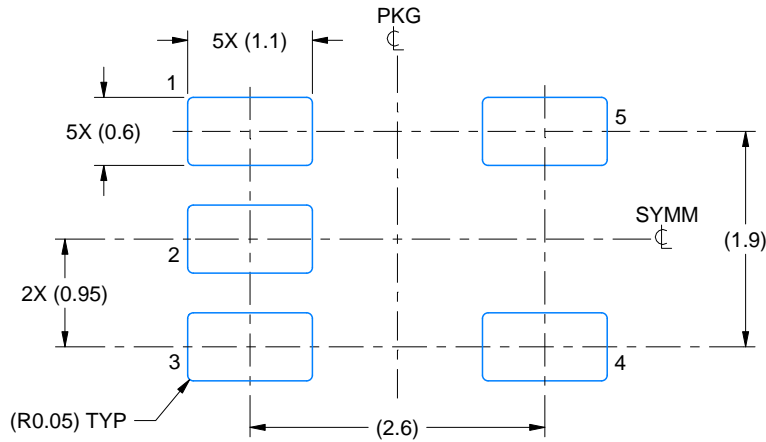
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated