Technical Documents

# TPS6505x 6-Channel Power-Management IC With Two Step-Down Converters and Four Low-Input Voltage LDOs 

## 1 Features

- Up To 95\% Efficiency
- Output Current for DC-DC Converters:
- TPS65050, TPS65054: $2 \times 0.6 \mathrm{~A}$
- TPS65051, TPS65052 and TPS65056: DCDC1 $=1 \mathrm{~A} ; \mathrm{DCDC} 2=0.6 \mathrm{~A}$
- Output Voltages for DC-DC Converters
- Externally Adjustable and Fixed Versions Available
- Digital Voltage Selection for the DCDC2
- $V_{1}$ Range for DC-DC Converters From 2.5 V to 6 V
- $2.25-\mathrm{MHz}$ Fixed-Frequency Operation
- Power Save Mode at Light Load Current
- $180^{\circ}$ Out-of-Phase Operation
- Output Voltage Accuracy in PWM Mode $\pm 1 \%$
- Total Typical $32-\mu \mathrm{A}$ Quiescent Current for Both DC-DC Converters
- 100\% Duty Cycle for Lowest Dropout
- Two General-Purpose $400-\mathrm{mA}$, High PSRR LDOs
- Two General-Purpose 200-mA, High PSRR LDOs
- $V_{1}$ range for LDOs From 1.5 V to 6.5 V
- Digital Voltage Selection for the LDOs


## 2 Applications

- Cell Phones, Smart Phones
- WLAN
- PDAs, Pocket PCs
- OMAPTM and Low-Power TMS320 ${ }^{\text {TM }}$ DSP Supply
- Samsung S3C24xx Application Processor Supply
- Portable Media Players


## 3 Description

The TPS6505x family of devices are integrated power-management ICs for applications powered by one Li-lon or Li-Polymer cell, which require multiple power rails. The TPS6505x devices provide two highly efficient, $2.25-\mathrm{MHz}$ step-down converters targeted at providing the core voltage and I/O voltage in a processor-based system. Both step-down converters enter a low-power mode at light load for maximum efficiency across the widest possible range of load currents. For low noise applications, the devices can be forced into fixed-frequency PWM mode by pulling the MODE pin high. The TPS6505x devices also integrate two $400-\mathrm{mA}$ LDO and two 200mA LDO voltage regulators. Each LDO operates with an input voltage range from 1.5 V to 6.5 V , allowing them to be supplied from one of the step-down converters or directly from the main battery.

| Device Information $^{(1)}$ |  |  |
| :--- | :---: | :---: |
| PART NUMBER PACKAGE BODY SIZE (NOM) <br> TPS6505x VQFN $(32)$ $4.00 \mathrm{~mm} \times 4.00 \mathrm{~mm}$ |  |  |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram


An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

Changes from Revision A (August 2007) to Revision B Page

- Added Pin Configuration and Functions section, ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ..... 1
- Changed graph in Figure 27: should be PF_IN and PB_OUT not PB_IN and /RESPWRON ..... 23
Changes from Original (January 2007) to Revision A ..... Page
- Added quantities of 3000 parts to ordering information note ..... 3
- Added Output voltage range to absolute maximum ratings table ..... 5
- Changed LDO1/2 Output voltage range maximum value to 3.6 V ..... 5
- Changed Output voltage 2.8-V R5 resistor value to $360 \mathrm{k} \Omega$ in typical resistor values table. ..... 29


## 5 Device Options

| PART NUMBER | OPTION | OUTPUT CURRENT for DC-DC CONVERTERS | $\begin{gathered} \text { QFN }^{(1)} \\ \text { PACKAGE }^{(2)} \end{gathered}$ | PACKAGE MARKING |
| :---: | :---: | :---: | :---: | :---: |
| TPS65050 | LDO voltages according to Table 2 DC-DC converters externally adjustable | $2 \times 600 \mathrm{~mA}$ | RSM | 65050 |
| TPS65051 | LDO voltages externally adjustable DC-DC converters externally adjustable | $\begin{gathered} \text { DCDC1 }=1 \mathrm{~A} \\ \text { DCDC2 }=600 \mathrm{~mA} \end{gathered}$ |  | 65051 |
| TPS65052 | LDO voltages according to Table 2 DCDC1 $=3.3 \mathrm{~V} ; \operatorname{DCDC} 2=1 \mathrm{~V} / 1.3 \mathrm{~V}$ | $\begin{gathered} \text { DCDC1 }=1 \mathrm{~A} \\ \text { DCDC2 }=600 \mathrm{~mA} \end{gathered}$ |  | 65052 |
| TPS65054 | LDO voltages externally adjustable DCDC1 = externally adjustable DCDC2 $=1.3 \mathrm{~V} / 1.05 \mathrm{~V}$ | $2 \times 600 \mathrm{~mA}$ |  | 65054 |
| TPS65056 | LDO voltages externally adjustable $\begin{gathered} \mathrm{DCDC1}=3.3 \mathrm{~V} \\ \mathrm{DCDC} 2=1 \mathrm{~V} / 1.3 \mathrm{~V} \end{gathered}$ | $\begin{gathered} D C D C 1=1 \mathrm{~A} \\ \text { DCDC2 }=600 \mathrm{~mA} \end{gathered}$ |  | 65056 |

(1) The RSM package is available in tape and reel. Add the R suffix (TPS65050RSMR) to order quantities of 3000 parts per reel. Add the T suffix (TPS65050RSMT) to order quantities of 250 parts per reel.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

## 6 Pin Configuration and Functions



Pin Functions

| PIN |  |  |  |  |  | I/O | DESCRIPTION |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| NAME | TPS65050 | TPS65051 | TPS65052 | TPS65054 | TPS65056 |  |  |
| AGND | 2 | 2 | 2 | 2 | 2 | I | Analog GND, connect to PGND and PowerPAD™ |
| BP | 1 | 1 | 1 | 1 | 1 | 1 | Input for bypass capacitor for internal reference. |
| DEFDCDC2 | 17 | 17 | 17 | 17 | 17 | 1 | TPS65050 and TPS65051 devices: Feedback pin for converter 2. Connect DEFDCDC2 to the center of the external resistor divider. TPS65052 and TPS65056 devices: Select pin of converter 2 output voltage. <br> High = 1.3 V , Low $=1 \mathrm{~V}$ <br> TPS65054 device: Select pin of converter 2 output voltage. $\text { High }=1.05 \mathrm{~V} \text {, Low }=1.3 \mathrm{~V}$ |
| DEFLDO1 | 31 | - | 31 | - | - | I | Digital input, used to set the default output voltage of LDO1 to LDO4; LSB |
| DEFLDO2 | 6 | - | 6 | - | - | I | Digital input, used to set the default output voltage of LDO1 to LDO4. |
| DEFLDO3 | 9 | - | 9 | - | - | I | Digital input, used to set the default output voltage of LDO1 to LDO4. |
| DEFLDO4 | 13 | - | 13 | - | - | I | Digital input, used to set the default output voltage of LDO1 to LDO4; MSB |
| EN_DCDC1 | 25 | 25 | 25 | 25 | 25 | 1 | Enable Input for converter 1, active high |
| EN_DCDC2 | 26 | 26 | 26 | 26 | 26 | 1 | Enable Input for converter 2, active high |
| EN_LDO1 | 27 | 27 | 27 | 27 | 27 | I | Enable input for LDO1. Logic high enables the LDO, logic low disables the LDO. |
| EN_LDO2 | 28 | 28 | 28 | 28 | 28 | I | Enable input for LDO2. Logic high enables the LDO, logic low disables the LDO. |
| EN_LDO3 | 15 | 15 | 15 | 15 | 15 | I | Enable input for LDO3. Logic high enables the LDO, logic low disables the LDO. |
| EN_LDO4 | 16 | 16 | 16 | 16 | 16 | 1 | Enable input for LDO4. Logic high enables the LDO, logic low disables the LDO. |
| FB1 | - | 31 | - | 31 | 31 | 1 | Feedback input for the external voltage divider. |
| FB2 | - | 6 | - | 6 | 6 | 1 | Feedback input for the external voltage divider. |
| FB3 | - | 9 | - | 9 | 9 | 1 | Feedback input for the external voltage divider. |
| FB4 | - | 13 | - | 13 | 13 | 1 | Feedback input for the external voltage divider. |
| FB_DCDC1 | 24 | 24 | 24 | 24 | 24 | 1 | Input to adjust output voltage of converter 1 between 0.6 V and $\mathrm{V}_{1}$. Connect external resistor divider between VOUT1, this pin, and GND. |
| GND | 8 | - | - | - | - | - | Connect to GND |
| HYSTERESIS | -- | 8 | 8 | 8 | 8 | 1 | Input for hysteresis on reset threshold |
| L1 | 22 | 22 | 22 | 22 | 22 | 0 | Switch pin of converter 1. Connected to Inductor . |
| L2 | 20 | 20 | 20 | 20 | 20 | 0 | Switch Pin of converter 2. Connected to Inductor. |
| MODE | 32 | 32 | 32 | 32 | 32 | 1 | Select between Power Safe Mode and forced PWM Mode for DCDC1 and DCDC2. In Power Safe Mode, PFM is used at light loads, PWM for greater loads. If PIN is set to high level, forced PWM Mode is selected. If Pin has low level, then the device operates in Power Safe Mode. |
| PB_IN | 7 | - | - | - | - | 1 | Input for the pushbutton ON-OFF function |
| PB_OUT | 14 | - | - | - | - | O | Open-drain output. Active low after the supply voltage ( $\mathrm{V}_{\mathrm{CC}}$ ) exceeded the undervoltage lockout threshold. The pin can be toggled pulling PB_IN high. |
| PGND1 | 23 | 23 | 23 | 23 | 23 | 1 | GND for converter 1 |
| PGND2 | 19 | 19 | 19 | 19 | 19 | 1 | GND for converter 2 |
| RESET | -- | 14 | 14 | 14 | 14 | 0 | Open-drain active low reset output, 100-ms reset delay time. |
| THRESHOLD | -- | 7 | 7 | 7 | 7 | 1 | Reset input |
| $\mathrm{V}_{\mathrm{Cc}}$ | 3 | 3 | 3 | 3 | 3 | 1 | Power supply for digital and analog circuitry of DCDC1, DCDC2 and LDOs. This pin must be connected to the same voltage supply as VINDCDC1/2. |
| VDCDC2 | 18 | 18 | 18 | 18 | 18 | I | Feedback voltage sense input, connect directly to the output of converter 2. |
| VINDCDC1/2 | 21 | 21 | 21 | 21 | 21 | I | Input voltage for VDCDC1 and VDCDC2 step-down converter. This must be connected to the same voltage supply as $\mathrm{V}_{\mathrm{Cc}}$. |
| VINLDO1 | 29 | 29 | 29 | 29 | 29 | 1 | Input voltage for LDO1 |

## Pin Functions (continued)

| PIN |  |  |  |  | I/O |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: | :--- | :--- |
| NAME | TPS65050 | TPS65051 | TPS65052 | TPS65054 |  |  |  |
| VINLDO2 | 4 | 4 | 4 | 4 | 4 | I | Input voltage for LDO2 |
| VINLDO3/4 | 11 | 11 | 11 | 11 | 11 | I | Input voltage for LDO3 and LDO4 |
| VLDO1 | 30 | 30 | 30 | 30 | 30 | O | Output voltage of LDO1 |
| VLDO2 | 5 | 5 | 5 | 5 | 5 | O | Output voltage of LDO2 |
| VLDO3 | 10 | 10 | 10 | 10 | 10 | O | Output voltage of LDO3 |
| VLDO4 | 12 | 12 | 12 | 12 | 12 | O | Output voltage of LDO4 |
| PowerPAD ${ }^{\text {TM }}$ | - | - | - | - | - |  | Connect to GND |

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ${ }^{(1)}$

| $\mathrm{V}_{\mathbf{I}}$ |  | Input voltage range on all pins except AGND, PGND, and EN_LDO1 pins with <br> respect to AGND | MIN |
| :--- | :--- | :---: | :---: |
|  | Input voltage range on EN_LDO1 pins with respect to AGND | -0.3 | 7 |
| $\mathrm{I}_{\mathrm{I}}$ | Current at VINDCDC1/2, L1, PGND1, L2, PGND2 | -0.3 | $\mathrm{~V}_{\text {CC }}+0.5$ |
|  | Current at all other pins | 1800 | V |
| $\mathrm{~V}_{\mathrm{O}}$ | Output voltage range for LDO1, LDO2, LDO3, and LDO4 | mA |  |
|  | Continuous total power dissipation | -0.3 | 4000 |
| $\mathrm{~T}_{\mathrm{A}}$ | Operating free-air temperature | See Dissipation Ratings | mA |
| $\mathrm{T}_{\mathrm{J}}$ | Maximum junction temperature | -40 | 85 |
| $\mathrm{~T}_{\text {stg }}$ | Storage temperature |  | $\mathrm{V}^{\circ} \mathrm{C}$ |

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

| $\mathrm{V}_{(\text {(ESD })} \quad$ Electrostatic discharge |  |  | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ${ }^{(1)}$ |
| :--- | :--- | :---: | :---: |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|  |  | MIN | NOM MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: |
| $V_{1}$ | Input voltage range for step-down converters, VINDCDC1/2 | 2.5 | 6 | V |
|  | Output voltage range for step-down converter, VDCDC1 | 0.6 | VINDCDC1/2 | V |
| V | Output voltage range for step-down converter, VDCDC2 | 0.6 | VINDCDC1/2 | V |
| $V_{1}$ | Input voltage range for LDOs, VINLDO1, VINLDO2, VINLDO3/4 | 1.5 | 6.5 | V |
| $\mathrm{V}_{\mathrm{O}}$ | Output voltage range for LDO1, LDO2, LDO3 and LDO4 | 1 | 3.6 | V |
|  | Output current at L1 (DCDC1) for TPS65051, TPS65052 |  | 1000 | mA |
|  | Output current at L1 (DCDC1) for TPS65050, TPS65054 |  | 600 | mA |
| lo | Output current at L1 (DCDC2) |  | 600 | mA |
|  | Output current at VLDO1, VLDO2 |  | 400 | mA |
|  | Output current at VLDO3, VLDO4 |  | 200 | mA |

## Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

|  |  | MIN | NOM | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | Inductor at L1, L2 ${ }^{(1)}$ | 1.5 | 2.2 |  | $\mu \mathrm{H}$ |
|  | Output capacitor at VDCDC1, VDCDC2 ${ }^{(1)}$ | 10 | 22 |  | $\mu \mathrm{F}$ |
| Co | Output capacitor at VLDO1, VLDO2, VLDO3, VLDO4 ${ }^{(1)}$ | 2.2 |  |  | $\mu \mathrm{F}$ |
| C | Input capacitor at VCC ${ }^{(1)}$ | 1 |  |  | $\mu \mathrm{F}$ |
| C | Input capacitor at VINLDO1/2/3/4 ${ }^{(1)}$ | 2.2 |  |  | $\mu \mathrm{F}$ |
| $\mathrm{T}_{\mathrm{A}}$ | Operating ambient temperature range | -40 |  | 85 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{\mathrm{J}}$ | Operating junction temperature range | -40 |  | 125 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{R}_{\text {filter }}$ | Resistor from battery voltage to $\mathrm{V}_{\mathrm{CC}}$ used for filtering ${ }^{(2)}$ |  | 1 | 10 | $\Omega$ |

(1) See the Application and Implementation section of this data sheet for more details.
(2) Up to 2 mA can flow into $\mathrm{V}_{\mathrm{CC}}$ when both converters are running in PWM, this resistor causes the UVLO threshold to be shifted accordingly.

### 7.4 Thermal Information

| THERMAL METRIC ${ }^{(1)}$ |  | TPS6505x | UNIT |
| :---: | :---: | :---: | :---: |
|  |  | RSM [VQFN] |  |
|  |  | 32 PINS |  |
| $\mathrm{R}_{\text {өJA }}$ | Junction-to-ambient thermal resistance | 37.3 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {өJC(top) }}$ | Junction-to-case (top) thermal resistance | 30.4 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {өJB }}$ | Junction-to-board thermal resistance | 8 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\Psi_{\text {JT }}$ | Junction-to-top characterization parameter | 0.4 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\Psi_{\text {JB }}$ | Junction-to-board characterization parameter | 7.8 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {өJC(bot) }}$ | Junction-to-case (bottom) thermal resistance | 2.5 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

### 7.5 Electrical Characteristics

$\mathrm{V}_{\mathrm{CC}}=\mathrm{VINDCDC} 1 / 2=3.6 \mathrm{~V}, \mathrm{EN}=\mathrm{V}_{\mathrm{CC}}, \mathrm{MODE}=\mathrm{GND}, \mathrm{L}=2.2 \mu \mathrm{H}, \mathrm{C}_{\mathrm{O}}=10 \mu \mathrm{~F} . \mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$, typical values are at $\mathrm{T}_{\mathrm{A}}=$ $25^{\circ} \mathrm{C}$ (unless otherwise noted).

|  | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SUPPLY CURRENT |  |  |  |  |  |  |
| $V_{1}$ | Input voltage range at VINDCDC1/2 |  | 2.5 |  | 6 | V |
| $\mathrm{I}_{\mathrm{Q}}$ | Operating quiescent current Total current into $\mathrm{V}_{\mathrm{CC}}$, VINDCDC1/2, VINLDO1, VINLDO2, VINLDO3/4 | One converter, $\mathrm{I}_{\mathrm{O}}=0 \mathrm{~mA}$. <br> PFM mode enabled (Mode $=$ GND) device not switching, EN_DCDC1 $=V_{1}$ OR EN_DCDC2 $=V_{1}$; EN_LDO1 $=$ EN_LDO2 $=$ EN_LDO3/4 $=$ GND |  | 20 | 30 | $\mu \mathrm{A}$ |
|  |  | $\begin{aligned} & \text { Two converters, } I_{0}=0 \mathrm{~mA} \\ & \text { PFM mode enabled (Mode = } 0 \text { ) device not switching, } \\ & \text { EN_DCDC1 = V } / \text { AND EN_DCDC2 = V }{ }_{1} \text {; EN_LDO1 = } \\ & \text { EN_LDO2 = EN_LDO3/4 = GND } \end{aligned}$ |  | 32 | 40 | $\mu \mathrm{A}$ |
|  |  | $\begin{aligned} & \text { One converter, } \mathrm{I}_{\mathrm{O}}=0 \mathrm{~mA} . \\ & \text { PFM mode enabled (Mode }=\text { GND }) \text { device not } \\ & \text { switching, EN_DCDC1 = } \mathrm{V}_{1} \text { OR EN_DCDC2 }=\mathrm{V}_{1} \text {; } \\ & \text { EN_LDO1 = EN_LDO2 }=\text { EN_LDO3 }=E N \_L D O 4= \\ & V_{1} \end{aligned}$ |  | 180 | 250 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{Q}$ | Operating quiescent current into $\mathrm{V}_{\mathrm{CC}}$ | One converter, $\mathrm{I}_{\mathrm{O}}=0 \mathrm{~mA}$. <br> Switching with no load (Mode $=V_{1}$ ), PWM operation <br> EN_DCDC1 = $\mathrm{V}_{1}$ OR EN_DCDC2 = $\mathrm{V}_{1}$; EN_LDO1 = EN_LDO2 $=$ EN_LDO3/4 $=$ GND |  | 0.85 |  | mA |
|  |  | Two converters, $\mathrm{I}_{\mathrm{O}}=0 \mathrm{~mA}$ Switching with no load (Mode $=V_{1}$ ), PWM operation EN_DCDC1 = $\mathrm{V}_{1}$ AND EN_DCDC2 $=\mathrm{V}_{1}$; EN_LDO1 = EN_LDO2 $=$ EN_LDO3/4 = GND |  | 1.25 |  | mA |
| $\mathrm{I}_{(S D)}$ | Shutdown current | EN_DCDC1 = EN_DCDC2 = GND EN_LDO1 = EN_LDO2 $=\mathrm{EN}$ LDO3 $=\mathrm{EN}-\mathrm{LDO} 4=$ GND |  | 9 | 12 | $\mu \mathrm{A}$ |

## Electrical Characteristics (continued)

$\mathrm{V}_{\mathrm{CC}}=\mathrm{VINDCDC} 1 / 2=3.6 \mathrm{~V}, \mathrm{EN}=\mathrm{V}_{\mathrm{CC}}, \mathrm{MODE}=\mathrm{GND}, \mathrm{L}=2.2 \mu \mathrm{H}, \mathrm{C}_{\mathrm{O}}=10 \mu \mathrm{~F} . \mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$, typical values are at $\mathrm{T}_{\mathrm{A}}=$ $25^{\circ} \mathrm{C}$ (unless otherwise noted).

| PARAMETER |  |  | TEST CONDITIONS |  | MIN | TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {(UVLO) }}$ | Undervoltage lockout threshold for DCDC converters and LDOs |  | Voltage at $\mathrm{V}_{\mathrm{CC}}$ |  |  | 1.8 | 2 | V |
| EN_DCDC1, EN_DCDC2, DEFDCDC2, DEFLDO1, DEFLDO2, DEFLDO3, DEFLDO4, EN_LDO1, EN_LDO2, EN_LDO3, EN_LDO4 |  |  |  |  |  |  |  |  |
|  | High-level input voltage |  | MODE/DATA, EN_DCDC1, EN_DCDC2, DEFDCDC2, DEFLDO1, DEFLDO2, DEFLDO3, DEFLDO4, EN_LDO1, EN_LDO2, EN_LDO3, EN_LDO4 |  | 1.2 |  | $\mathrm{V}_{\text {CC }}$ | V |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage |  | MODE/DATA, EN_DCDC1, EN_DCDC2, DEFLDO1, DEFLDO2, DEFLDO3, DEFLDŌ4, EN LDO1, EN_LDO2, EN_LDO3, EN_LDO4, DEFDCDC2 |  | 0 |  | 0.4 | V |
| $\mathrm{I}_{1 \mathrm{~B}}$ | Input bias current |  | MODE/DATA = GND or $\mathrm{V}_{1}$ <br> MODE/DATA, EN_DCDC1, EN_DCDC2, DEFDCDC2, DEFLDO1, DEFLDO2, DEFLDO3, DEFLDO4, EN_LDO1, EN_LDO2, EN_LDO3, EN_LDO4 |  |  | 0.01 | 1 | $\mu \mathrm{A}$ |
|  |  |  | $\begin{aligned} & \text { TPS65051 and TPS65052 only } \\ & \text { V_FB_LDOx = } 1 \mathrm{~V} \\ & \text { FB_LDO1, FB_LDO2, FB_LDO3, FB_LDO4 } \end{aligned}$ |  |  |  | 100 | nA |
| POWER SWITCH |  |  |  |  |  |  |  |  |
| $\mathrm{r}_{\text {DS }}$ (on) | P-channel MOSFET on resistance |  | DCDC1 | VINDCDC1/2 $=3.6 \mathrm{~V}$ |  | 280 | 630 | $\mathrm{m} \Omega$ |
|  |  |  | VINDCDC1/2 $=2.5 \mathrm{~V}$ | 400 |  |  |  |
|  |  |  | DCDC2 | VINDCDC1/2 $=3.6 \mathrm{~V}$ |  | 280 | 630 |  |
|  |  |  | VINDCDC $1 / 2=2.5 \mathrm{~V}$ | 400 |  |  |  |
| $\mathrm{I}_{\mathrm{kg}}$ | P-channel leakage current |  |  | $\mathrm{VDCDCx}=\mathrm{V}_{(\mathrm{DS})}=6 \mathrm{~V}$ |  |  |  | 1 | $\mu \mathrm{A}$ |
| ${ }^{\text {d }}$ (on) | N-channel MOSFET on resistance |  | DCDC1 | VINDCDC1/2 $=3.6 \mathrm{~V}$ |  | 220 | 450 | $\mathrm{m} \Omega$ |
|  |  |  | VINDCDC1/2 $=2.5 \mathrm{~V}$ | 320 |  |  |  |  |
|  |  |  | DCDC2 | VINDCDC1/2 $=3.6 \mathrm{~V}$ |  | 220 | 450 |  |
|  |  |  | VINDCDC1/2 $=2.5 \mathrm{~V}$ | 320 |  |  |  |
| $\mathrm{I}_{\mathrm{kg}}$ | N-channel leakage current |  |  | $\mathrm{VDCDCx}=\mathrm{V}_{(\mathrm{DS})}=6 \mathrm{~V}$ |  |  | 7 | 10 | $\mu \mathrm{A}$ |
| $\mathrm{l}_{\text {(LIMF) }}$ | Forward current limit PMOS (High-Side) and NMOS (Low side) | DCDC1: | $\begin{aligned} & \text { TPS65050 } \\ & \text { TPS65054 } \end{aligned}$ | $2.5 \mathrm{~V} \leq \mathrm{VINDCDC} 1 / 2 \leq 6$ | 0.85 | 1 | 1.15 | A |
|  |  |  | $\begin{aligned} & \text { TPS65051, TPS65052, } \\ & \text { TPS65056 } \end{aligned}$ |  | 1.19 | 1.4 | 1.65 |  |
|  |  | DCDC2: | TPS65050-TPS65056 | $\begin{aligned} & 2.5 \mathrm{~V} \leq \mathrm{VINDCDC} 1 / 2 \leq 6 \\ & \mathrm{~V} \end{aligned}$ | 0.85 | 1 | 1.15 | A |
| Thermal shutdown |  |  | Increasing junction temperature |  | 150 |  |  | ${ }^{\circ} \mathrm{C}$ |
| Thermal shutdown hysteresis |  |  | Decreasing junction temperature |  | 20 |  |  | ${ }^{\circ} \mathrm{C}$ |
| OSCILLATOR |  |  |  |  |  |  |  |  |
| $\mathrm{f}_{\text {Sw }}$ | Oscillator frequency |  |  |  | 2.025 | 2.25 | 2.475 | MHz |
| OUTPUT |  |  |  |  |  |  |  |  |
| $\mathrm{V}_{\text {O }}$ | Output voltage range for DCDC1, DCDC2 |  | externally adjustable versions |  | 0.6 | $\begin{array}{r} \hline \text { VINDCDC } \\ 1 / 2 \end{array}$ |  | V |
|  | Output voltage for DCDC1 |  | TPS65052 and TPS65056 |  | 3.3 |  |  | V |
|  | Output voltage for DCDC2 |  | TPS65052, TPS65054 and TPS65056 |  | $\begin{array}{r} \text { set by } \\ \text { DEFDCDC2, } \\ \text { see Table } 3 \end{array}$ |  |  | mV |
| $\mathrm{V}_{\text {ref }}$ | Reference voltage |  | externally adjustable versions |  | 600 |  |  |  |
| $\mathrm{V}_{\mathrm{O}}$ | DC output voltage accuracy | $\begin{aligned} & \text { DCDC1, } \\ & \text { DCDC2 }^{(1)} \end{aligned}$ | $\begin{aligned} & \text { VINDCDC } 1 / 2=2.5 \mathrm{~V} \text { to } 6 \mathrm{~V} \\ & 0 \mathrm{~mA}<\mathrm{I}_{\mathrm{O}}=<\mathrm{I}_{\mathrm{O}}(\max ) \\ & \text { Mode }=\text { GND, PFM operation } \end{aligned}$ |  | -2\% | 0 | 2\% |  |
|  |  |  | $\begin{aligned} & \text { VINDCDC } 1 / 2=2.5 \mathrm{~V} \text { to } 6 \mathrm{~V} \\ & 0 \mathrm{~mA}<\mathrm{I}_{\mathrm{O}}=<\mathrm{I}_{(\text {(max })} \\ & \text { Mode }=\mathrm{V}_{\mathrm{l}} \text {, PWM operation } \end{aligned}$ |  | -1\% 0 |  | 1\% |  |

[^0]
## Electrical Characteristics (continued)

$\mathrm{V}_{\mathrm{CC}}=\mathrm{VINDCDC1/2}=3.6 \mathrm{~V}, \mathrm{EN}=\mathrm{V}_{\mathrm{CC}}, \mathrm{MODE}=\mathrm{GND}, \mathrm{L}=2.2 \mu \mathrm{H}, \mathrm{C}_{\mathrm{O}}=10 \mu \mathrm{~F} . \mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$, typical values are at $\mathrm{T}_{\mathrm{A}}=$ $25^{\circ} \mathrm{C}$ (unless otherwise noted).

|  | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\Delta \mathrm{V}_{\mathrm{O}}$ | Power save mode ripple voltage ${ }^{(2)}$ | $\begin{aligned} & \mathrm{I}_{\mathrm{O}}=1 \mathrm{~mA}, \mathrm{Mode}=\mathrm{GND}, \mathrm{~V}_{\mathrm{O}}=1.3 \mathrm{~V}, \\ & \text { Bandwith }=20 \mathrm{MHz} \end{aligned}$ |  | 25 |  | $m V_{\text {PP }}$ |
| $\mathrm{t}_{\text {Start }}$ | Start-up time | time from active EN to Start switching |  | 170 |  | $\mu \mathrm{s}$ |
| $\mathrm{t}_{\text {Ramp }}$ | VOUT Ramp up Time | time to ramp from 5\% to $95 \%$ of $\mathrm{V}_{\text {O }}$ |  | 750 |  | $\mu \mathrm{s}$ |
| $t_{\text {RESET_DEL }}$ <br> AY | RESET delay time | Input voltage at threshold pin rising | 80 | 100 | 120 | ms |
| $\mathrm{t}_{\text {PB_DB }}$ | PB-ONOFF debounce time |  | 26 | 32 | 38 | ms |
| $\mathrm{V}_{\text {OL }}$ | RESET, PB_OUT output low voltage | $\mathrm{I}_{\mathrm{OL}}=1 \mathrm{~mA}$, Vhysteresis $<1 \mathrm{~V}$, Vthreshold $<1 \mathrm{~V}$ |  |  | 0.2 | V |
| $\mathrm{l}_{\mathrm{OL}}$ | RESET, PB_OUT sink current |  |  | 1 |  | mA |
| $\mathrm{I}_{\text {leak }}$ | RESET, PB_OUT output leakage current | After PB_IN has been pulled high once; Vthreshold > 1 V and $\overline{\mathrm{V}}$ hysteresis $>1 \mathrm{~V}, \mathrm{~V}_{\mathrm{OH}}=6 \mathrm{~V}$ |  | 10 |  | nA |
| $\mathrm{V}_{\text {th }}$ | Vthreshold, Vhysteresis threshold |  | 0.98 | 1 | 1.02 | V |
| VLDO1, VLDO2, VLDO3 and VLDO4 Low Dropout Regulators |  |  |  |  |  |  |
| $V_{1}$ | Input voltage range for LDO1, LDO2, LDO3, LDO4 |  | 1.5 |  | 6.5 | V |
| $\mathrm{V}_{\mathrm{O}}$ | LDO1 output voltage range | TPS65050, TPS65052 only | 1.2 |  | 3.3 | V |
|  | LDO2 output voltage range | TPS65050, TPS65052 only | 1.8 |  | 3.3 |  |
|  | LDO3 output voltage range | TPS65050, TPS65052 only | 1.1 |  | 3.3 |  |
|  | LDO4 output voltage range | TPS65050, TPS65052 only | 1.2 |  | 2.85 |  |
| $\mathrm{V}_{(\mathrm{FB})}$ | Feedback voltage for FB_LDO1, FB_LDO2, FB_LDO3, and FB_LDO4 | TPS65051, TPS65054 and TPS65056 only |  | 1 |  | V |
| $\mathrm{I}_{0}$ | Maximum output current for LDO1, LDO2 |  | 400 |  |  | mA |
|  | Maximum output current for LDO3, LDO4 |  | 200 |  |  | mA |
| $\mathrm{I}_{(\mathrm{SC})}$ | LDO1 short-circuit current limit | VLDO1 = GND | 750 |  |  | mA |
|  | LDO2 short-circuit current limit | VLDO2 = GND | 850 |  |  | mA |
|  | LDO3 and LDO4 short-circuit current limit | VLDO3 = GND, VLDO4 = GND | 420 |  |  | mA |
|  | Dropout voltage at LDO1 | $\mathrm{I}_{\mathrm{O}}=400 \mathrm{~mA}, \mathrm{~V}$ INLDO $=3.4 \mathrm{~V}$ | 400 |  |  | mV |
|  | Dropout voltage at LDO2 | $\mathrm{I}_{\mathrm{O}}=400 \mathrm{~mA}, \mathrm{~V}$ INLDO $=1.8 \mathrm{~V}$ | 280 |  |  | mV |
|  | Dropout voltage at LDO3, LDO4 | $\mathrm{I}_{\mathrm{O}}=200 \mathrm{~mA}, \mathrm{~V}$ INLDO $=1.8 \mathrm{~V}$ | 280 |  |  | mV |
| $\mathrm{l}_{\mathrm{kg}}$ | Leakage current from VinLDOx to VLDOx | LDO enabled, $\mathrm{VINLDO}=6.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=1 \mathrm{~V}$, at $\mathrm{T}_{\mathrm{A}}=140^{\circ} \mathrm{C}$ | 3 |  |  | $\mu \mathrm{A}$ |
| $\mathrm{V}_{0}$ | Output voltage accuracy for LDO1, LDO2, LDO3, LDO4 | $\mathrm{l}_{0}=10 \mathrm{~mA}$ | -2\% |  | 1\% |  |
|  | Line regulation for LDO1, LDO2, LDO3, LDO4 | ```VINLDO1,2 = VLDO1,2 + 0.5 V (min. 2.5 V) to 6.5V, VINLDO3,4 = VLDO3,4 + 0.5 V (minimum 2.5 V) to 6.5 V, I}=10\textrm{mA``` | -1\% 1\% |  |  |  |
|  | Load regulation for LDO1, LDO2, LDO3, LDO4 | $\mathrm{I}_{\mathrm{O}}=0 \mathrm{~mA}$ to 400 mA for LDO1, LDO2 $\mathrm{I}_{\mathrm{O}}=0 \mathrm{~mA}$ to 200 mA for LDO3, LDO4 | -1\% |  | 1\% | $\mu \mathrm{s}$ |
|  | Regulation time for LDO1, LDO2, LDO3, LDO4 | Load change from 10\% to 90\% | 10 |  |  |  |
| PSRR | Power supply rejection ratio | $\mathrm{f}=10 \mathrm{kHz} ; \mathrm{l}_{\mathrm{O}}=50 \mathrm{~mA} ; \mathrm{V}_{\mathrm{I}}=\mathrm{V}_{\mathrm{O}}+1 \mathrm{~V}$ | 70 |  |  | dB |
| $\mathrm{R}_{\text {(DIS) }}$ | Internal discharge resistor at VLDO1, VLDO2, VLDO3, VLDO4 | active when LDO is disabled | 350 |  |  | R |
|  | Thermal shutdown | Increasing junction temperature | 140 |  |  | ${ }^{\circ} \mathrm{C}$ |
|  | Thermal shutdown hysteresis | Decreasing junction temperature | 20 |  |  | ${ }^{\circ} \mathrm{C}$ |

(2) In Power Save Mode, operation is typically entered at $\mathrm{I}_{\mathrm{PSM}}=\mathrm{V}_{\mathrm{I}} / 32 \Omega$.

### 7.6 Dissipation Ratings

| PACKAGE | $\mathbf{R}_{\boldsymbol{\theta J A}}{ }^{(1)}$ | POWER RATING <br> $\mathbf{T}_{\mathbf{A}} \leq \mathbf{2 5} 5^{\circ} \mathbf{C}$ | DERATING FACTOR <br> ABOVE $\mathbf{T}_{\mathbf{A}}=\mathbf{2 5} 5^{\circ} \mathbf{C}$ | POWER RATING <br> $\mathbf{T}_{\mathbf{A}}=70^{\circ} \mathbf{C}$ | POWER RATING <br> $\mathbf{T}_{\mathbf{A}}=85^{\circ} \mathbf{C}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| RSM | $58 \mathrm{~K} / \mathrm{W}$ | 1.7 W | $17 \mathrm{~mW} / \mathrm{K}$ | 0.95 W | 0.68 W |

(1) The thermal resistance junction to case of the RSM package is $4 \mathrm{~K} / \mathrm{W}$ measured on a high K board

### 7.7 Typical Characteristics

Table 1. Table of Graphs

|  |  | vs Output current |
| :--- | :--- | :--- |
| Efficiency converter 1 | vs Output current | FIGURE |
| Efficiency converter 2 | vs Output current | Figure 1 |
| Efficiency converter 1 | vs Output current | Figure 2 |
| Efficiency converter 2 | PWM/PFM mode = low | Figure 3 |
| Output voltage ripple | PWM mode = high | Figure 4 |
| Output voltage ripple |  | Figure 5 |
| DCDC1 start-up timing |  | Figure 6 |
| LDO1 to LDO4 start-up timing | PWM mode = high | Figure 7 |
| DCDC1 load transient response | PFM mode = low | Figure 8 |
| DCDC1 load transient response | PWM mode = high | Figure 9 |
| DCDC2 load transient response | PFM mode = low | Figure 10 |
| DCDC2 load transient response |  | Figure 11 |
| DCDC1 line transient response |  | Figure 12 |
| DCDC2 line transient response |  | Figure 13 |
| LDO1 load transient response |  | Figure 14 |
| LDO4 load transient response |  | Figure 15 |
| LDO1 line transient response | vs Frequency | Figure 16 |
| Power supply rejection ratio | Figure 17 |  |



Figure 1. Efficiency vs Output Current


Figure 3. Efficiency vs Output Current

t - Time $=2 \mu \mathrm{~s} / \mathrm{div}$
Figure 5. Output Voltage Ripple PWM/PFM Mode = LOW


Figure 2. Efficiency vs Output Current


Figure 4. Efficiency vs Output Current

t - Time $=500 \mathrm{~ns} / \mathrm{div}$
Figure 6. Output Voltage Ripple PWM Mode $=$ HIGH


Figure 7. DCDC1 Start-up Timing


Figure 9. DCDC1 Load Transient Response


Figure 11. DCDC2 Load Transient Response


Figure 8. LDO1 to LDO4 Start-up Timing


Figure 10. DCDC1 Load Transient Response


Figure 12. DCDC2 Load Transient Response


Figure 13. DCDC1 Line Transient Response


Figure 15. LDO1 Load Transient Response


Figure 17. LDO1 Line Transient Response


Figure 14. DCDC2 Line Transient Response


Figure 16. LDO4 Load Transient Response


Figure 18. Power Supply Rejection Ratio vs Frequency

## 8 Detailed Description

### 8.1 Overview

The TPS6505x devices have 2 DC-DC buck converters and 4 LDOs. Each DC-DC and LDO have their own enable pins, allowing external sequence control of the PMU rails. The TPS6505x devices, (except the TPS65050 device), have a RESET feature that is generated from a THRESHOLD comparator. This RESET signal can be used to reset or warn of power shutdown to the embedded mircocontroller or processor. The TPS65050 device has a push-button feature for reset and sequence control. This feature can be used to shut down and start the converter with a single push on a button by connecting the PB_OUT output to the enable input of the converters. The TPS6505x devices make power system integration easy for a variety of embedded processors or FPGAs.

### 8.2 Functional Block Diagrams



Figure 19. TPS65050 Block Diagram

## Functional Block Diagrams (continued)



Figure 20. TPS65051 Block Diagram

## Functional Block Diagrams (continued)



Figure 21. TPS65052 Block Diagram

## Functional Block Diagrams (continued)



Figure 22. TPS65054 Block Diagram

Functional Block Diagrams (continued)


Figure 23. TPS65056 Block Diagram

### 8.3 Feature Description

### 8.3.1 Operation of DCDC Converters

The TPS6505x devices include each two synchronous step-down converters. The converters operate with 2.25MHz (typical) fixed frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents, the converters automatically enter Power Save Mode and operate with PFM (Pulse Frequency Modulation).
During PWM operation the converters use a unique fast response voltage mode controller scheme with input voltage feed-forward to achieve good line and load regulation allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the P-channel MOSFET switch is turned on, and the inductor current ramps up until the current comparator trips, and the control logic turns off the switch. The current limit comparator turns off the switch if the current limit of the P-channel switch is exceeded. After the adaptive dead time, which prevents shoot through current, the N-channel MOSFET rectifier is turned on, and the inductor current ramps down. The next cycle is initiated by the clock signal turning off the N -channel rectifier, and turning on the on the P-channel switch.
The two DC-DC converters operate synchronized to each other, with converter 1 as the master. A $180^{\circ}$ phase shift between converter 1 and converter 2 decreases the input RMS current. Therefore, smaller input capacitors can be used.

### 8.3.1.1 DCDC1 Converter

The converter 1 output voltage is set by an external resistor divider connected to FB_DCDC1 pin for the TPS65050 device, the TPS65051 device, and the TPS65054 device. For the TPS65052 device, the output voltage is fixed to 3.3 V and this pin needs to be directly connected to the output. See Application and Implementation for more details. The maximum output current on DCDC1 is 600 mA for the TPS65050 and TPS65054 devices. For the TPS65051 device, the TPS65052 device, and the TPS65056 device, the maximum output current is 1 A .

### 8.3.1.2 DCDC2 Converter

The VDCDC2 pin must be directly connected to the DCDC2 converter output voltage. The DCDC2 converter output voltage is selected through the DEFDCDC2 pin.
For the TPS65050 and TPS65051 devices, the output voltage is set with an external resistor divider. Connect the DEFDCDC2 pin to the external resistor divider.
For the TPS65052, TPS65054, and TPS65056 devices, the The DEFDCDC2 pin can either be connected to GND, or to $\mathrm{V}_{\mathrm{CC}}$. The converter 2 output voltage defaults to:

| DEVICE | DEFDCDC2 $=$ LOW | DEFDCDC2 $=\mathbf{H I G H}$ |
| :---: | :---: | :---: |
| TPS65052 , TPS65056 | 1 V | 1.3 V |
| TPS65054 | 1.3 V | 1.05 V |

### 8.3.2 Power-Save Mode

The Power-Save Mode is enabled with the Mode pin set to 0 . If the load current decreases, the converters enters Power-Save Mode operation automatically. During Power-Save Mode, the converters operate with reduced switching frequency in PFM mode, and with a minimum quiescent current to maintain high-efficiency. The converter positions the output voltage $1 \%$ above the nominal output voltage. This voltage positioning feature minimizes voltage drops caused by a sudden load step.

To optimize the converter efficiency at light load, the average current is monitored. If in PWM mode, the inductor current remains below a certain threshold, then Power-Save Mode is entered. The typical threshold is calculated according to Equation 1.
$\mathrm{I}_{(\text {PFM_enter })}=\frac{\text { VINDCDC }}{32 \Omega}$
A. Average output current threshold to enter PFM mode.
$I_{(\text {PSMDCDC_leave })}=\frac{\text { VINDCDC }}{24 \Omega}$

During the Power-Save Mode, the output voltage is monitored with a comparator. As the output voltage falls below the skip comparator threshold (skip comp), the P-channel switch turns on, and the converter effectively delivers a constant current. If the load is below the delivered current, the output voltage rises until the skip comp threshold is crossed again, then all switching activity ceases, reducing the quiescent current to a minimum until the output voltage has dropped below the threshold. If the load current is greater than the delivered current, the output voltage falls until it crosses the skip comparator low (Skip Comp Low) threshold set to $1 \%$ below nominal $\mathrm{V}_{\mathrm{O}}$, then Power-Save Mode is exited, and the converter returns to PWM mode
These control methods reduce the quiescent current to $12 \mu \mathrm{~A}$ per converter, and the switching frequency to a minimum, achieving the highest converter efficiency. The PFM mode operates with low output voltage ripple. The ripple depends on the comparator delay, and the size of the output capacitor; increasing capacitor values decreases the output ripple voltage.
The Power-Save Mode can be disabled by driving the MODE pin high. In forced PWM mode, both converters operate with fixed frequency PWM mode regardless of the load.

### 8.3.3 Dynamic Voltage Positioning

This feature reduces the voltage undershoots and overshoots at load steps from light to heavy load and vice versa. It is activated in Power-Save Mode operation when the converter runs in PFM Mode. It provides more headroom for both, the voltage drop at a load step and the voltage increase at a load throw-off. This improves load transient behavior.

At light loads, in which the converter operate in PFM Mode, the output voltage is regulated typically $1 \%$ greater than the nominal value. In the event of a load transient from light load to heavy load, the output voltage drops until it reaches the skip comparator low threshold set to $-1 \%$ below the nominal value and enters PWM mode. During a release from heavy load to light load, the voltage overshoot is also minimized due to active regulation turning on the N -channel switch.


Figure 24. Dynamic Voltage Positioning

### 8.3.4 Soft Start

The two converters have an internal soft start circuit that limits the inrush current during start-up. During soft start, the output voltage ramp up is controlled as shown in Figure 25.


Figure 25. Soft Start

### 8.3.5 100\% Duty Cycle Low Dropout Operation

The converters offer a low input to output voltage difference while still maintaining operation with the use of the $100 \%$ duty cycle mode. In this mode, the P-channel switch is constantly turned on. This is useful in batterypowered applications to achieve longest operation time by taking full advantage of the whole battery voltage range (that is, the minimum input voltage to maintain regulation depends on the load current and output voltage) and can be calculated using Equation 3.
$V_{I}(\min )=V_{O}(\max )+I_{O}(\max ) \times\left(r_{D S(\text { on })}(\max )+R_{L}\right)$
where

- $\mathrm{I}_{0}$ max $=$ maximum output current plus inductor ripple current.
- $r_{D S(o n)} \max =$ maximum P-channel switch $r_{D S(o n)}$.
- $R_{L}=D C$ resistance of the inductor.
- $\mathrm{V}_{\mathrm{O}}(\max )=$ nominal output voltage plus maximum output voltage tolerance.


### 8.3.6 Undervoltage Lockout

The undervoltage lockout circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery and disables all internal circuitry. The undervoltage lockout threshold, which is sensed at the $\mathrm{V}_{\mathrm{CC}}$ pin, is typically $1.8 \mathrm{~V}, 2 \mathrm{~V}$ (maximum).

### 8.3.7 Mode Selection

The MODE pin allows mode selection between forced PWM Mode and Power-Safe Mode for both converters. Connecting this pin to GND enables the automatic PWM and power save mode operation. The converters operates in fixed frequency PWM mode at moderate to heavy loads and in the PFM mode during light loads, maintaining high-efficiency over a wide load current range.
Pulling the MODE pin high forces both converters to operate constantly in the PWM mode even at light load currents. The advantage is the converters operate with a fixed frequency that allows simple filtering of the switching frequency for noise sensitive applications. In this mode, the efficiency is lower compared to the PowerSave Mode during light loads. For additional flexibility, it is possible to switch from Power-Save Mode to forced PWM mode during operation. This allows efficient power management by adjusting the operation of the converter to the specific system requirements.

### 8.3.8 Enable

To start up each converter independently, the device has a separate enable pin for each DC-DC converter and for each LDO. If EN_DCDC1, EN_DCDC2, EN_LDO1, EN_LDO2, EN_LDO3, EN_LDO4 are set to high, the corresponding converter starts up with soft start as previously described.
Pulling the enable pin low forces the device into shutdown, with a shutdown quiescent current as defined in Electrical Characteristics. In this mode, the P and N -Channel MOSFETs are turned off, the and the entire internal control circuitry is switched off. If disabled, the outputs of the LDOs are pulled low by internal $350-\Omega$ resistors, actively discharging the output capacitor. For proper operation, the enable pins must be terminated and must not be left unconnected.

### 8.3.9 $\overline{R E S E T}$

The TPS65051, TPS65052, TPS65054, and TPS65056 devices contain circuitry that can generate a reset pulse for a processor with a $100-\mathrm{ms}$ delay time. The input voltage at a comparator is sensed at an input called threshold. When the voltage exceeds the threshold, the output goes high with a $100-\mathrm{ms}$ delay time. A hysteresis can be defined with an external resistor connected to the hysteresis input. This circuitry is functional as soon as the supply voltage at $\mathrm{V}_{C C}$ exceeds the undervoltage lockout threshold. Therefore, the TPS6505x devices have a shutdown current (all DC-DC converters and LDOs are off) of $9 \mu \mathrm{~A}$ to supply bandgap and comparator.


Figure 26. $\overline{\text { RESET Pulse Circuit }}$

### 8.3.10 Push-Button ON-OFF (PB-ON-OFF)

The TPS65050 device provides a PB-ON-OFF functionality instead of supervising a voltage with the threshold and hysteresis inputs. The output at PB_OUT is held low after voltage is applied at $\mathrm{V}_{\mathrm{cc}}$. Only after the input at PB-IN is pulled high once, the output driver at PB_OUT goes to its inactive state, driven high with its external pullup resistor. Further low-high pulses at PB-IN toggles the status of the PB_OUT output, and can be used to shut down and start the converter with a single push on a button by connecting the PB_OUT output to the enable input of the converters.


Figure 27. Push-Button Circuit

### 8.3.11 Short-Circuit Protection

All outputs are short-circuit protected with a maximum output current as defined in the Electrical Characteristics.

### 8.3.12 Thermal Shutdown

As soon as the junction temperature, $\mathrm{T}_{\mathrm{J}}$, exceeds $150^{\circ} \mathrm{C}$ (typically) for the DC-DC converters, the device goes into thermal shutdown. In this mode, the P and N -Channel MOSFETs are turned off. The device continues its operation when the junction temperature falls below the thermal shutdown hysteresis again. A thermal shutdown for one of the DC-DC converters disables both converters simultaneously.

The thermal shutdown temperature for the LDOs are set to typically $140^{\circ} \mathrm{C}$. Therefore, a LDO, which may be used to power an external voltage, never heats up the chip high enough to turn off the DC-DC converters. If one LDO exceeds the thermal shutdown temperature, all LDOs turns off simultaneously.

### 8.3.13 Low Dropout Voltage Regulators

The low dropout voltage regulators are designed to operate well with small ceramic input and output capacitors. They operate with input voltages down to 1.5 V . The LDOs offer a maximum dropout voltage of 280 mV at rated output current. Each LDO supports a current limit feature. The LDOs are enabled by the EN_LDO1, ENLDO2, EN_LDO3 and EN_LDO4 pin. In the TPS65050 and TPS65052 devices, the output voltage of the LDOs is set using 4 pins. The DEFLDO1 to DEFLDO4 pins can either be connected to GND or Vbat ( $\mathrm{V}_{\mathrm{Cc}}$ ) to define a set of output voltages for LDO1 to LDO4 according to table 1. Connecting the DEFLDOx pins to a voltage different from GND or $\mathrm{V}_{\mathrm{CC}}$ causes increased leakage current into $\mathrm{V}_{\mathrm{Cc}}$. In the TPS65051 and TPS65054 devices, the output voltage of the LDOs is set using external resistor dividers.

According to Table 2, The TPS65050 and TPS65052 devices default voltage options adjustable with DEFLDO4...DEFLDO1.

Table 2. Default Options

| DEFLDO1 | DEFLDO2 | DEFLDO3 | DEFLDO4 | VLDO1 | VLDO2 | VLDO3 | VLDO4 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | 400 mA LDO | 400 mA LDO | 200 mA LDO | 200 mA LDO |
|  |  |  |  | 1.8 V to 5.5 V <br> Input | 1.8 V to 5.5 V <br> Input | 1.5 V to 5.5 V <br> Input | 1.5 V to 5.5 V <br> Input |
| 0 | 0 | 0 | 0 | 3.3 V | 3.3 V | 1.85 V | 1.85 V |
| 0 | 0 | 0 | 1 | 3.3 V | 3.3 V | 1.5 V | 1.5 V |
| 0 | 0 | 1 | 0 | 3.3 V | 2.85 V | 2.85 V | 2.7 V |

Table 2. Default Options (continued)

| DEFLD01 | DEFLDO2 | DEFLDO3 | DEFLDO4 | VLDO1 | VLDO2 | VLDO3 | VLDO4 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 1 | 1 | 3.3 V | 2.85 V | 2.85 V | 2.5 V |
| 0 | 1 | 0 | 0 | 3.3 V | 2.85 V | 2.85 V | 1.85 V |
| 0 | 1 | 0 | 1 | 3.3 V | 2.85 V | 1.85 V | 1.85 V |
| 0 | 1 | 1 | 0 | 3.3 V | 2.85 V | 1.5 V | 1.5 V |
| 0 | 1 | 1 | 1 | 3.3 V | 2.85 V | 1.5 V | 1.3 V |
| 1 | 0 | 0 | 0 | 3.3 V | 2.85 V | 1.1 V | 1.3 V |
| 1 | 0 | 0 | 1 | 2.85 V | 2.85 V | 1.85 V | 1.85 V |
| 1 | 0 | 1 | 0 | 2.7 V | 3.3 V | 1.2 V | 1.2 V |
| 1 | 0 | 1 | 1 | 2.5 V | 3.3 V | 1.5 V | 1.5 V |
| 1 | 1 | 0 | 0 | 2.5 V | 3.3 V | 1.5 V | 1.3 V |
| 1 | 1 | 0 | 1 | 1.85 V | 1.85 V | 1.35 V | 1.35 V |
| 1 | 1 | 1 | 0 | 1.8 V | 2.5 V | 3.3 V | 2.85 V |
| 1 | 1 | 1 | 1 | 1.2 V | 1.8 V | 1.1 V | 1.3 V |

### 8.4 Device Functional Modes

The TPS6505x devices are either in the ON or the OFF mode. The OFF mode is entered when the voltage on $\mathrm{V}_{\mathrm{CC}}$ is below the UVLO threshold, 1.8 V (typically). Once the voltage at $\mathrm{V}_{\mathrm{CC}}$ has increased above UVLO, the device enters ON mode. In the ON mode, the DCDCs and LDOs are available for use.

## 9 Application and Implementation

## NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

This device integrates two step-down converters and four LDOs, which can be used to power the voltage rails needed by a processor or any other application. The PMIC can be controlled through the ENABLE and MODE pins or sequenced from the VIN using RC delay circuits. There is a logic output, RESET, provide the application processor or load a logic signal indicating power good or reset.

### 9.2 Typical Application



Figure 28. Typical Example Application With PB_ON/OFF Circuit

### 9.2.1 Design Requirements

The TPS6505x devices have only a few design requirements. Use the following parameters for the design examples:

## Typical Application (continued)

- $1-\mu \mathrm{F}$ bypass capacitor on VCC, located as close as possible to the VCC pin to ground.
- VCC and VINDCDC1/2 must be connected to the same voltage supply with minimal voltage difference.
- Input capacitors must be present on the VINDCDC1/2, VIN_LDO1, VINLDO2, and VIN_LDO3/4 supplies if used.
- Output inductor and capacitors must be used on the outputs of the DCDC converters if used.
- Output capacitors must be used on the outputs of the LDOs if used.


### 9.2.2 Detailed Design Procedure

### 9.2.2.1 Output Voltage Setting

### 9.2.2.1.1 Converter 1 (DCDC1)

The output voltage of converter 1 can be set by an external resistor network. The output voltage can be calculated using Equation 4.

$$
\begin{equation*}
\mathrm{V}_{\mathrm{O}}=\mathrm{V}_{\text {ref }} \times\left(1+\frac{\mathrm{R} 1}{\mathrm{R} 2}\right) \tag{4}
\end{equation*}
$$

with an internal reference voltage $\mathrm{V}_{\text {ref }}, 0.6 \mathrm{~V}$.
TI recommends setting the total resistance of R1 + R2 to less than $1 \mathrm{M} \Omega$. The resistor network connects to the input of the feedback amplifier, therefore, requiring a small feedforward capacitor in parallel to R1. A typical value of 47 pF is sufficient.
For the TPS65052 and TPS65056 devices, the DCDC1 output voltage is internally fixed to 3.3 V .

### 9.2.2.1.2 Converter 2 (DCDC2)

The output voltage of converter 2 can be selected as following:

- Adjustable output voltage defined with external resistor network on pin DEFDCDC2. This option is available for the TPS65050 and TPS65051 devices.
- Two default fixed output voltages are selectable by pin DEFDCDC2 (see Table 3). This option is available for the TPS65052, TPS65054, and TPS65056 devices.

Table 3. Default Fixed Output Voltages

| Converter 2 | DEFDCDC2 $=$ low | DEFDCDC2 $\boldsymbol{=}$ high |
| :---: | :---: | :---: |
| TPS65050 | - | - |
| TPS65051 | - | - |
| TPS65052 | 1 V | 1.3 V |
| TPS65054 | 1.3 V | 1.05 V |
| TPS65056 | 1 V | 1.3 V |

The adjustable output voltage can be calculated similarly to the DCDC1 converter. Setting the total resistance of $R 3+R 4$ to less than $1 \mathrm{M} \Omega$ is recommended. Route the DEFDCDC2 line separate from noise sources, such as the inductor or the L2 line. The VDCDC2 line needs to be directly connected to the output capacitor. As the VDCDC2 line is the feedback to the internal amplifier, no feedforward capacitor at R3 is needed.
Using an external resistor divider at DEFDCDC2:


Figure 29. External Resistor Divider

## $\mathrm{V}_{(\mathrm{DEFDCDC} 2)}=0.6 \mathrm{~V}$

$$
v_{O}=V_{(D E F D C D C 2)} \times \frac{R 3+R 4}{R 4} \quad R 3=R 4 \times\left(\frac{V_{O}}{V_{(D E F D C D C 2)}}\right)-R 4
$$

See Table 4 for typical resistor values:
Table 4. Typical Resistor Values

| OUTPUT VOLTAGE | R1 | R2 | NOMINAL VOLTAGE | Typical CFF |
| :---: | :---: | :---: | :---: | :---: |
| 3.3 V | $680 \mathrm{k} \Omega$ | $150 \mathrm{k} \Omega$ | 3.32 V | 47 pF |
| 3 V | $510 \mathrm{k} \Omega$ | $130 \mathrm{k} \Omega$ | 2.95 V | 47 pF |
| 2.85 V | $560 \mathrm{k} \Omega$ | $150 \mathrm{k} \Omega$ | 2.84 V | 47 pF |
| 2.5 V | $510 \mathrm{k} \Omega$ | $160 \mathrm{k} \Omega$ | 2.51 V | 47 pF |
| 1.8 V | $300 \mathrm{k} \Omega$ | $150 \mathrm{k} \Omega$ | 1.8 V | 47 pF |
| 1.6 V | $200 \mathrm{k} \Omega$ | $120 \mathrm{k} \Omega$ | 1.6 V | 47 pF |
| 1.5 V | $300 \mathrm{k} \Omega$ | $200 \mathrm{k} \Omega$ | 1.5 V | 47 pF |
| 1.2 V | $330 \mathrm{k} \Omega$ | $330 \mathrm{k} \Omega$ | 1.2 V | 47 pF |

### 9.2.2.2 Output Filter Design (Inductor and Output Capacitor)

### 9.2.2.2.1 Inductor Selection

The two converters operate with $2.2-\mu \mathrm{H}$ output inductor. Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. The selected inductor has to be rated for its DC resistance and saturation current. The DC resistance of the inductance directly influences the efficiency of the converter. Therefore, an inductor with lowest DC resistance should be selected for highest efficiency. The minimum inductor value is $1.5 \mu \mathrm{H}$, but an output capacitor of $22 \mu \mathrm{~F}$ minimum is needed in this case. For an output voltage above 2.8 V , TI recommends an inductor value of $3.3 \mu \mathrm{H}$ (minimum). Lower values result in an increased output voltage ripple in PFM mode.
Use Equation 6 to calculate the maximum inductor current under static load conditions. The saturation current of the inductor should be rated greater than the maximum inductor current as calculated with Equation 6. TI recommends this because during heavy load transient the inductor current rises above the calculated value.

$$
\Delta \mathrm{I}_{\mathrm{L}}=\mathrm{V}_{\mathrm{O}} \times \frac{1-\frac{\mathrm{V}_{\mathrm{O}}}{\mathrm{~V}_{\mathrm{I}}}}{\mathrm{~L} \times f} \quad \quad \mathrm{I}_{\mathrm{L}}(\max )=\mathrm{I}_{\mathrm{O}}(\max )+\frac{\Delta \mathrm{I}_{\mathrm{L}}}{2}
$$

where

- $\mathrm{f}=$ Switching Frequency (2.25-MHz typical)
- L = Inductor Value
- $\Delta \mathrm{I}_{\mathrm{L}}=$ Peak-to-peak inductor ripple current
- $\quad \mathrm{I}$ max = Maximum Inductor current

The highest inductor current occurs at maximum $\mathrm{V}_{\mathrm{I}}$. Open core inductors have a soft saturation characteristic, and they can normally handle greater inductor currents versus a comparable shielded inductor.

A more conservative approach is to select the inductor current rating just for the maximum switch current of the corresponding converter. Consideration must be given to the difference in the core material from inductor to inductor which has an impact on the efficiency especially at high switching frequencies. See Table 5 and the typical applications for possible inductors.

Table 5. Tested Inductors

| INDUCTOR TYPE | INDUCTOR VALUE | SUPPLIER |
| :---: | :---: | :---: |
| LPS3010 | $2.2 \mu \mathrm{H}$ | Coilcraft |
| LPS3015 | $3.3 \mu \mathrm{H}$ | Coilcraft |
| LPS4012 | $2.2 \mu \mathrm{H}$ | Coilcraft |
| VLF4012 | $2.2 \mu \mathrm{H}$ | TDK |

### 9.2.2.2.2 Output Capacitor Selection

The advanced Fast Response voltage mode control scheme of the two converters allows the use of small ceramic capacitors with a value of $22-\mu \mathrm{F}$ (typical) without having large output voltage undershoots and overshoots during heavy load transients. Ceramic capacitors having low ESR values result in lowest output voltage ripple, and are recommended.
If ceramic output capacitors are used, the capacitor RMS ripple current rating always meets the application requirements. For completeness, the RMS ripple current is calculated as:

$$
\begin{equation*}
\mathrm{I}_{\text {(RMSCout) }}=\mathrm{V}_{\mathrm{O}} \times \frac{1-\frac{\mathrm{V}_{\mathrm{O}}}{\mathrm{~V}_{\mathrm{I}}}}{\mathrm{~L} \times f} \times \frac{1}{2 \times \sqrt{3}} \tag{7}
\end{equation*}
$$

At nominal load current, the inductive converters operate in PWM mode, and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$
\Delta \mathrm{V}_{\mathrm{O}}=\mathrm{V}_{\mathrm{O}} \times \frac{1-\frac{\mathrm{V}_{\mathrm{O}}}{\mathrm{~V}_{\mathrm{I}}}}{\mathrm{~L} \times f} \times\left(\frac{1}{8 \times \mathrm{C}_{\mathrm{O}} \times f}+\mathrm{ESR}\right)
$$

where

- the highest output voltage ripple occurs at the highest input voltage $\mathrm{V}_{1}$

At light load currents, the converters operate in Power-Save Mode and the output voltage ripple is dependent on the output capacitor value. The output voltage ripple is set by the internal comparator delay and the external capacitor. The typical output voltage ripple is less than $1 \%$ of the nominal output voltage.

### 9.2.2.2.3 Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. The converters need a ceramic input capacitor of $10 \mu \mathrm{~F}$. The input capacitor can be increased without any limit for better input voltage filtering.

Table 6. Possible Capacitors

| CAPACITOR VALUE | SIZE | SUPPLIER | TYPE |
| :---: | :---: | :---: | :---: |
| $2.2 \mu \mathrm{~F}$ | 0805 | TDK C2012X5R0J226MT | Ceramic |
| $2.2 \mu \mathrm{~F}$ | 0805 | Taiyo Yuden JMK212BJ226MG | Ceramic |

Table 6. Possible Capacitors (continued)

| CAPACITOR VALUE | SIZE | SUPPLIER | TYPE |
| :---: | :---: | :---: | :---: |
| $10 \mu \mathrm{~F}$ | 0805 | Taiyo Yuden JMK212BJ106M | Ceramic |
| $10 \mu \mathrm{~F}$ | 0805 | TDK C2012X5R0J106M | Ceramic |
| $10 \mu \mathrm{~F}$ | 0603 | Taiyo Yuden JMK107BJ106MA | Ceramic |

### 9.2.2.3 Low Drop Out Voltage Regulators (LDOs)

The output voltage of all 4 LDOs in the TPS65051, TPS65054, and TPS65056 devices are set by an external resistor network. The output voltage is calculated using Equation 9.

$$
V_{\mathrm{O}}=\mathrm{V}_{\mathrm{ref}} \times\left(1+\frac{\mathrm{R} 5}{\mathrm{R} 6}\right)
$$

where

- an internal reference voltage, $\mathrm{V}_{\text {ref }}, 1 \mathrm{~V}$ (typical)

TI recommends setting the total resistance of R5 + R6 to less than $1 \mathrm{M} \Omega$. Typically, there is no feedforward capacitor needed at the voltage dividers for the LDOs.

$$
\begin{equation*}
V_{\mathrm{O}}=\mathrm{V}_{(\text {(FB_LDOs) }} \times \frac{R 5+R 6}{R 6} \quad R 5=R 6 \times\left(\frac{V_{O}}{V_{\left(F B \_L D O s\right)}}\right)-R 6 \tag{10}
\end{equation*}
$$

Typical resistor values:
Table 7. Typical Resistor Values

| OUTPUT VOLTAGE | R5 | $\mathbf{R 6}$ | NOMINAL VOLTAGE |
| :---: | :---: | :---: | :---: |
| 3.3 V | $300 \mathrm{k} \Omega$ | $130 \mathrm{k} \Omega$ | 3.31 V |
| 3 V | $300 \mathrm{k} \Omega$ | $150 \mathrm{k} \Omega$ | 3 V |
| 2.85 V | $240 \mathrm{k} \Omega$ | $130 \mathrm{k} \Omega$ | 2.85 V |
| 2.8 V | $360 \mathrm{k} \Omega$ | $200 \mathrm{k} \Omega$ | 2.8 V |
| 2.5 V | $300 \mathrm{k} \Omega$ | $200 \mathrm{k} \Omega$ | 2.5 V |
| 1.8 V | $240 \mathrm{k} \Omega$ | $300 \mathrm{k} \Omega$ | 1.8 V |
| 1.5 V | $150 \mathrm{k} \Omega$ | $300 \mathrm{k} \Omega$ | 1.5 V |
| 1.3 V | $36 \mathrm{k} \Omega$ | $120 \mathrm{k} \Omega$ | 1.3 V |
| 1.2 V | $100 \mathrm{k} \Omega$ | $510 \mathrm{k} \Omega$ | 1.19 V |
| 1.1 V | $33 \mathrm{k} \Omega$ | $330 \mathrm{k} \Omega$ | 1.1 V |

### 9.2.2.4 PB-ONOFF and Sequencing

The PB-ONOFF output can be used to enable one or several converters. After power up, the PB_OUT pin is low, and pulls down the enable pins connected to PB_OUT; EN_DCDC1, and EN_LDO1 in Figure 28. When PB_IN is pulled to $\mathrm{V}_{\mathrm{CC}}$ for longer than 32 ms , the PB_OUTT pin is turned off, hence the enable pins pulled high using a pullup resistor to $\mathrm{V}_{\mathrm{Cc}}$. This enables the DCDC1 converter and LDO1. The output voltage of DCDC1 (Vout1) is used as the enable signal for DCDC2 and LDO2 to LDO4. LDO1 with its output voltage of 3.3 V and LDO2 for an output voltage of 2.5 V are powered from the battery $\left(\mathrm{V}_{(\text {bat }}\right)$ directly. To save power, the input voltage for the lower voltage rails at LDO3 and LDO4 are derived from the output of the step-down converters, keeping the voltage drop at the LDOs low to increase efficiency. As LDO3 and LDO4 are powered from the output of DCDC1, the total output current on $\mathrm{V}_{\text {OUT }} 1$, LDO3 and LDO4 must not exceed the maximum rating of DCDC1.

Figure 30 shows the power-up timing for this example application.


Figure 30. Example Power-up Timing

### 9.2.2.5 RESET

The TPS65051, TPS65052, TPS65054, and TPS65056 devices contain a comparator that is used to supervise a voltage connected to an external voltage divider, and generate a reset signal if the voltage is lower than the threshold. The rising edge is delayed by 100 ms at the open-drain RESET output. The values for the external resistors R3 to R5 are calculated as follows:
$\mathrm{V}_{\mathrm{L}}=$ lower voltage threshold
$V_{L}=$ lower voltage threshold
$\mathrm{V}_{\text {REF }}=$ reference voltage ( 1 V )
Example:

- $\mathrm{V}_{\mathrm{L}}=3.3 \mathrm{~V}$
- $\mathrm{V}_{\mathrm{H}}=3.4 \mathrm{~V}$

Set R5 $=100 \mathrm{k} \Omega$
$\rightarrow \mathrm{R} 3+\mathrm{R} 4=240 \mathrm{k} \Omega$
$\rightarrow \mathrm{R} 4=3.03 \mathrm{k} \Omega$
$\rightarrow R 3=237 \mathrm{k} \Omega$
$R 3+R 4=R 5 \times\left(\frac{V_{H}}{V_{\text {ref }}}-1\right)$

$$
\begin{equation*}
R 4=R 5 \times \frac{V_{H}-V_{L}}{V_{L}} \tag{14}
\end{equation*}
$$



Figure 31. RESET Circuit

### 9.2.3 Application Curves



Figure 32. Efficiency vs Output Current


Figure 33. Efficiency vs Output Current

## 10 Power Supply Recommendations

Any supply from 2.5 V to 6 V will work as long as the power supply can supply enough current at the VIN voltage that the application demands.

## 11 Layout

### 11.1 Layout Guidelines

- The input capacitors for the DC-DC converters should be placed as close as possible to the VINDCDC1/2 pin and the PGND1 and PGND2 pins.
- The inductor of the output filter should be placed as close as possible to the device to provide the shortest switch node possible, reducing the noise emitted into the system and increasing the efficiency.
- Sense the feedback voltage from the output at the output capacitors to ensure the best DC accuracy. Feedback should be routed away from noisy sources such as the inductor. If possible route on the opposing side as the switch node and inductor and place a GND plane between the feedback and the noisy sources or keepout underneath them entirely.
- Place the output capacitors as close as possible to the inductor to reduce the feedback loop as much as possible. This will ensure best regulation at the feedback point.
- Place the device as close as possible to the most demanding or sensitive load. The output capacitors should be placed close to the input of the load. This will ensure the best AC performance possible.
- The input and output capacitors for the LDOs should be placed close to the device for best regulation performance.
- TI recommends using the common ground plane for the layout of this device. The AGND can be separated from the PGND but, a large low parasitic PGND is required to connect the PGNDx pins to the CIN and external PGND connections. If the AGND and PGND planes are separated, have one connection point to reference the grounds together. Place this connection point close to the IC.


### 11.2 Layout Example



Figure 34. Layout Example from EVM for TPS6505x

## 12 Device and Documentation Support

### 12.1 Device Support

### 12.1.1 Third-Party Products Disclaimer

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### 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE \& BUY | TECHNICAL <br> DOCUMENTS |  <br> SOFTWARE |  <br> COMMUNITY |
| :---: | :---: | :---: | :---: | :---: | :---: |
| TPS65050 | Click here | Click here | Click here | Click here | Click here |
| TPS65051 | Click here | Click here | Click here | Click here | Click here |
| TPS65052 | Click here | Click here | Click here | Click here | Click here |
| TPS65054 | Click here | Click here | Click here | Click here | Click here |
| TPS65056 | Click here | Click here | Click here | Click here | Click here |

### 12.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2ETM Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.
Design Support TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 Trademarks

TMS320, PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

### 12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.6 Glossary

SLYZ022 - TI Glossary.
This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status <br> (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <br> (2) | Lead/Ball Finish <br> (6) | MSL Peak Temp <br> (3) | Op Temp ( ${ }^{\circ} \mathrm{C}$ ) | Device Marking <br> (4/5) | Samples |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| TPS65050RSMR | ACTIVE | VQFN | RSM | 32 | 3000 | Green (RoHS \& no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |  | $\begin{aligned} & \text { TPS } \\ & 65050 \end{aligned}$ | Samples |
| TPS65050RSMT | ACTIVE | VQFN | RSM | 32 | 250 | Green (RoHS \& no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |  | $\begin{aligned} & \hline \text { TPS } \\ & 65050 \end{aligned}$ | Samples |
| TPS65050RSMTG4 | ACTIVE | VQFN | RSM | 32 | 250 | Green (RoHS \& no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |  | $\begin{aligned} & \text { TPS } \\ & 65050 \end{aligned}$ | Samples |
| TPS65051RSMR | ACTIVE | VQFN | RSM | 32 | 3000 | Green (RoHS \& no $\mathrm{Sb} / \mathrm{Br}$ ) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | $\begin{aligned} & \text { TPS } \\ & 65051 \end{aligned}$ | Samples |
| TPS65051RSMRG4 | ACTIVE | VQFN | RSM | 32 | 3000 | Green (RoHS \& no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TPS 65051 | Samples |
| TPS65051RSMT | ACTIVE | VQFN | RSM | 32 | 250 | Green (RoHS \& no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | $\begin{aligned} & \text { TPS } \\ & 65051 \\ & \hline \end{aligned}$ | Samples |
| TPS65051RSMTG4 | ACTIVE | VQFN | RSM | 32 | 250 | Green (RoHS \& no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TPS 65051 | Samples |
| TPS65052RSMT | ACTIVE | VQFN | RSM | 32 | 250 | Green (RoHS \& no $\mathrm{Sb} / \mathrm{Br}$ ) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | $\begin{aligned} & \text { TPS } \\ & 65052 \end{aligned}$ | Samples |
| TPS65054RSMR | ACTIVE | VQFN | RSM | 32 | 3000 | Green (RoHS \& no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | $\begin{aligned} & \text { TPS } \\ & 65054 \end{aligned}$ | Samples |
| TPS65054RSMT | ACTIVE | VQFN | RSM | 32 | 250 | Green (RoHS \& no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | $\begin{aligned} & \text { TPS } \\ & 65054 \end{aligned}$ | Samples |
| TPS65054RSMTG4 | ACTIVE | VQFN | RSM | 32 | 250 | Green (RoHS \& no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | $\begin{aligned} & \text { TPS } \\ & 65054 \end{aligned}$ | Samples |
| TPS65056RSMR | ACTIVE | VQFN | RSM | 32 | 3000 | Green (RoHS \& no $\mathrm{Sb} / \mathrm{Br}$ ) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TPS 65056 | Samples |
| TPS65056RSMT | ACTIVE | VQFN | RSM | 32 | 250 | Green (RoHS \& no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | $\begin{aligned} & \text { TPS } \\ & 65056 \end{aligned}$ | Samples |

${ }^{(1)}$ The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.
${ }^{(2)}$ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS \& no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined
Pb -Free (RoHS): Tl's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed $0.1 \%$ by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS \& no Sb/Br): Tl defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine ( Br ) and Antimony ( Sb ) based flame retardants ( Br or Sb do not exceed $0.1 \%$ by weight in homogeneous material)
${ }^{(3)}$ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
${ }^{(4)}$ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
${ }^{(5)}$ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a " $\sim$ " will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
${ }^{(6)}$ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

| Device | Package <br> Type | Package <br> Drawing | Pins | SPQ | Reel <br> Diameter <br> $(\mathbf{m m})$ | Reel <br> Width <br> $\mathbf{W 1}(\mathbf{m m})$ | A0 <br> $(\mathbf{m m})$ | B0 <br> $(\mathbf{m m})$ | K0 <br> $(\mathbf{m m})$ | P1 <br> $(\mathbf{m m})$ | $\mathbf{W}$ <br> $(\mathbf{m m})$ | Pin1 <br> uadrant |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| TPS65050RSMR | VQFN | RSM | 32 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| TPS65050RSMT | VQFN | RSM | 32 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| TPS65051RSMR | VQFN | RSM | 32 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| TPS65051RSMR | VQFN | RSM | 32 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| TPS65051RSMT | VQFN | RSM | 32 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| TPS65051RSMT | VQFN | RSM | 32 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| TPS65052RSMT | VQFN | RSM | 32 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| TPS65054RSMR | VQFN | RSM | 32 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| TPS65054RSMT | VQFN | RSM | 32 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| TPS65056RSMR | VQFN | RSM | 32 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| TPS65056RSMT | VQFN | RSM | 32 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| TPS65050RSMR | VQFN | RSM | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| TPS65050RSMT | VQFN | $R S M$ | 32 | 250 | 210.0 | 185.0 | 35.0 |
| TPS65051RSMR | VQFN | $R S M$ | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| TPS65051RSMR | VQFN | $R S M$ | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| TPS65051RSMT | VQFN | $R S M$ | 32 | 250 | 210.0 | 185.0 | 35.0 |
| TPS65051RSMT | VQFN | $R S M$ | 32 | 250 | 210.0 | 185.0 | 35.0 |
| TPS65052RSMT | VQFN | $R S M$ | 32 | 250 | 210.0 | 185.0 | 35.0 |
| TPS65054RSMR | VQFN | $R S M$ | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| TPS65054RSMT | VQFN | $R S M$ | 32 | 250 | 210.0 | 185.0 | 35.0 |
| TPS65056RSMR | VQFN | $R S M$ | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| TPS65056RSMT | VQFN | $R S M$ | 32 | 250 | 210.0 | 185.0 | 35.0 |



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) Package configuration.
(1) The package thermal pad must be soldered to the board for thermal and mechanical performance.

See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
RSM (S-PVQFN-N32) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION
This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.


Bottom View<br>Exposed Thermal Pad Dimensions

NOTE: All linear dimensions are in millimeters

RSM (S-PVQFN-N32)

## PLASTIC QUAD FLATPACK NO-LEAD



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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[^0]:    (1) Output voltage specification does not include tolerance of external voltage programming resistors.

