

TPS255x Precision Adjustable Current-Limited Power-Distribution Switches

1 Features

- Meets USB Current-Limiting Requirements
- Adjustable Current Limit, 500 mA to 5 A (Typical)
- $\pm 6.5\%$ Current-Limit Accuracy at 4.5 A
- Fast Overcurrent Response: 3.5- μs (Typical)
- 22-m Ω High-Side MOSFET
- Operating Voltage: 2.5 V to 6.5 V
- 2- μA Maximum Standby Supply Current
- Built-in Soft Start
- 15-kV and 8-kV System-Level ESD Capable
- UL Listed: File No. E169910 and CB IEC60950-1-am2 ed2.0

2 Applications

- USB Ports and Hubs
- Digital TVs
- Set-Top Boxes
- VOIP Phones

3 Description

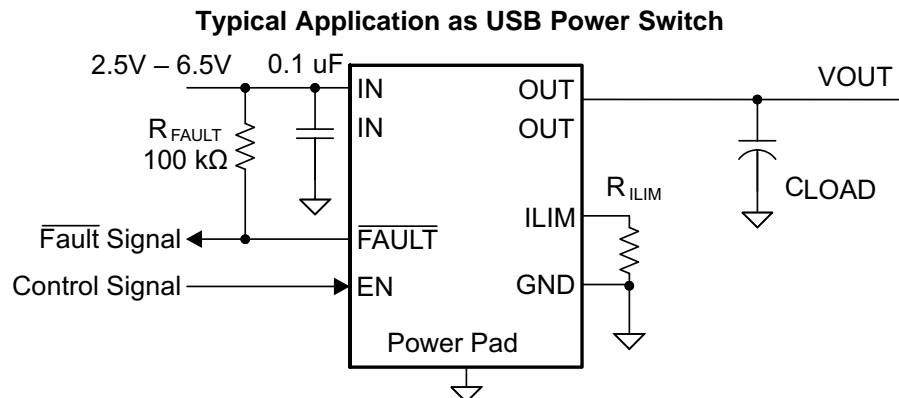
The TPS255x power-distribution switch is intended for applications where precision current limiting is required or heavy capacitive loads and short circuits are encountered. These devices offer a programmable current-limit threshold between 500 mA and 5 A (typical) through an external resistor. The power-switch rise and fall times are controlled to minimize current surges during turnon and turnoff.

TPS255x devices limit the output current to a safe level by switching into a constant-current mode when the output load exceeds the current-limit threshold. The FAULT logic output asserts low during overcurrent and overtemperature conditions.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|------------------|----------|-------------------|
| TPS2556, TPS2557 | VSON (8) | 3.00 mm x 3.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2012) to Revision B

Page

| | |
|--|----------|
| • Added <i>Device Information</i> table, <i>Device Comparison Table</i> , <i>Pin Configuration and Functions</i> section, <i>Specifications</i> section, <i>ESD Ratings</i> table, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section | 1 |
| • Deleted <i>Ordering Information</i> table; see Package Option Addendum at the end of the data sheet | 1 |
| • Added <i>Thermal Information</i> table | 5 |
| • Changed $R_{\theta JC(top)}$ value in <i>Thermal Information</i> table From: 10.7°C/W To: 54.5°C/W | 5 |
| • Changed Figure 11 title From: Current Limit Threshold Vs R_{ILM} To: Switch Current vs Drain-Source Voltage Across Switch | 7 |
| • Changed Figure 12 title From: Current Limit Threshold Vs R_{ILM} To: Switch Current vs Drain-Source Voltage Across Switch | 7 |

Changes from Original (November 2009) to Revision A

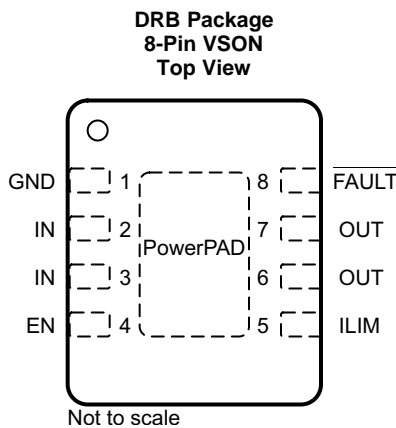
Page

| | |
|--|----------|
| • Changed V_{EN} to $V_{\overline{EN}}$ in <i>Recommended Operating Conditions</i> table | 4 |
| • Changed $V_{\overline{EN}}$ to V_{EN} in <i>Recommended Operating Conditions</i> table | 4 |

5 Device Comparison Table

| 33 mΩ, SINGLE | 80 mΩ, SINGLE | 80 mΩ, DUAL | 80 mΩ, DUAL | 80 mΩ, TRIPLE | 80 mΩ, QUAD | 80 mΩ, QUAD |
|--------------------|-----------------|-----------------|----------------|-----------------|-----------------|----------------|
| | | | | | | |
| TPS201xA 0.2 A–2 A | TPS2014 600 mA | TPS2042B 500 mA | TPS2080 500 mA | TPS2043B 500 mA | TPS2044B 500 mA | TPS2085 500 mA |
| TPS202x 0.2 A–2 A | TPS2015 1 A | TPS2052B 500 mA | TPS2081 500 mA | TPS2053B 500 mA | TPS2044B 500 mA | TPS2086 500 mA |
| TPS203x 0.2 A–2 A | TPS2041B 500 mA | TPS2052B 500 mA | TPS2081 500 mA | TPS2043B 500 mA | TPS2044B 500 mA | TPS2086 500 mA |
| | TPS2051B 500 mA | TPS2046B 250 mA | TPS2082 500 mA | TPS2053B 500 mA | TPS2044B 500 mA | TPS2085 500 mA |
| | TPS2045A 250 mA | TPS2056 250 mA | TPS2090 250 mA | TPS2047B 250 mA | TPS2054B 500 mA | TPS2086 500 mA |
| | TPS2049 100 mA | TPS2062 1 A | TPS2091 250 mA | TPS2057A 250 mA | TPS2048A 250 mA | TPS2087 500 mA |
| | TPS2055A 250 mA | TPS2066 1 A | TPS2092 250 mA | TPS2063 1 A | TPS2058 250 mA | TPS2095 250 mA |
| | TPS2061 1 A | TPS2060 1.5 A | | TPS2067 1 A | | TPS2096 250 mA |
| | TPS2065 1 A | TPS2064 1.5 A | | | | TPS2097 250 mA |
| | TPS2068 1.5 A | | | | | |
| | TPS2069 1.5 A | | | | | |

6 Pin Configuration and Functions



TPS2556: $\overline{\text{EN}}$ pin is active low.
 TPS2557: EN pin is active high.

Pin Functions

| NAME | PIN | | I/O | DESCRIPTION |
|---------------------------|----------|----------|-----|---|
| | TPS2556 | TPS2557 | | |
| $\overline{\text{EN}}$ | 4 | — | I | Enable input: Logic low turns on power switch. Applicable to the TPS2556. |
| EN | — | 4 | I | Enable input: Logic high turns on power switch. Applicable to the TPS2557. |
| $\overline{\text{FAULT}}$ | 8 | 8 | O | Active-low open-drain output: Asserted during overcurrent or overtemperature conditions. |
| GND | 1 | 1 | — | Ground connection: Connect externally to PowerPAD. |
| ILIM | 5 | 5 | O | External resistor used to set current-limit threshold. TI recommends $20 \text{ k}\Omega \leq R_{\text{ILIM}} \leq 187 \text{ k}\Omega$. |
| IN | 2, 3 | 2, 3 | I | Input voltage: Connect a 0.1- μF or greater ceramic capacitor from IN to GND as close to the IC as possible. |
| OUT | 6, 7 | 6, 7 | O | Power-switch output. |
| PowerPAD™ | PowerPAD | PowerPAD | — | Internally connected to GND. Used to heat-sink the part to the circuit board traces. Connect PowerPAD to GND pin externally. |

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

| | | MIN | MAX | UNIT |
|---|--|---|-------|------|
| Voltage | IN, OUT, EN or $\overline{\text{EN}}$, ILIM, and $\overline{\text{FAULT}}$ pins | -0.3 | 7 | V |
| Voltage from IN to OUT | | -7 | 7 | V |
| Continuous output current | | Internally limited | | |
| Continuous $\overline{\text{FAULT}}$ sink current | | 25 | | mA |
| ILIM source current | | Internally limited | | |
| Continuous total power dissipation | | See Thermal Information | | |
| Maximum junction temperature | | -40 | OTSD2 | °C |
| Storage temperature, T_{stg} | | -65 | 150 | °C |

- Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- Voltages are referenced to GND unless otherwise noted.

7.2 ESD Ratings

| | | VALUE | UNIT |
|--|--|--------|------|
| $V_{\text{(ESD)}}$ Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±500 | |
| | IEC 61000-4-2 contact discharge ⁽³⁾ | ±8000 | |
| | IEC 61000-4-2 air discharge ⁽³⁾ | ±15000 | |

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
- Surges per EN61000-4-2, 1999 applied between USB and output ground of the TPS2556EVM (HPA423) evaluation module (see [Using the TPS2556EVM-423 and TPS2557EVM-423](#)). These were the test levels, not the failure threshold.

7.3 Recommended Operating Conditions

| | | MIN | MAX | UNIT |
|----------------------------|---|---------|------|------------|
| V_{IN} | Input voltage, IN | 2.5 | 6.5 | V |
| $V_{\overline{\text{EN}}}$ | Enable voltage | TPS2556 | 0 | 6.5 |
| V_{EN} | | TPS2557 | 0 | |
| V_{IH} | High-level input voltage on Enable pin | 1.1 | | V |
| V_{IL} | Low-level input voltage on Enable pin | | 0.66 | |
| I_{OUT} | Continuous output current (OUT pin) | 0 | 5 | A |
| | Continuous $\overline{\text{FAULT}}$ sink current | 0 | 10 | mA |
| R_{ILIM} | Recommended resistor limit | 20 | 187 | k Ω |
| T_{J} | Operating virtual junction temperature | -40 | 125 | °C |

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | TPS255x | |
|-------------------------------|--|------------|------|
| | | DRB (VSON) | |
| | | 8 PINS | |
| | | | UNIT |
| R _{θJA} | Junction-to-ambient thermal resistance | 41.5 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 54.5 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 16.4 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 0.7 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 16.6 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | 3.6 | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Electrical Characteristics

over recommended operating conditions, V_{EN} = 0 V or V_{EN} = V_{IN} (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------|--|---|----------------------------|------|------|------|
| POWER SWITCH | | | | | | |
| r _{DS(ON)} | Static drain-source on-state resistance | T _J = 25°C | | 22 | 25 | mΩ |
| | | −40°C ≤ T _J ≤ 125°C | | | 35 | |
| | Enable pin turn on and off threshold | | 0.66 | | 1.1 | V |
| | Enable input hysteresis ⁽²⁾ | | | 55 | | mV |
| I _{EN} | Input current | V _{EN} = 0 V or 6.5 V, V _{EN} = 0 V or 6.5 V | −0.5 | | 0.5 | μA |
| I _{OS} | Current-limit threshold (Maximum DC output current I _{OUT} delivered to load) and short-circuit current, OUT connected to GND | R _{LIM} = 24.9 kΩ | 4130 | 4450 | 4695 | mA |
| | | R _{LIM} = 61.9 kΩ | 1590 | 1785 | 1960 | |
| | | R _{LIM} = 100 kΩ | 935 | 1100 | 1260 | |
| I _{IN_OFF} | Supply current, low-level output | V _{IN} = 6.5 V, No load on OUT, V _{EN} = 6.5 V or V _{EN} = 0 V | | 0.1 | 2 | μA |
| I _{IN_ON} | Supply current, high-level output | V _{IN} = 6.5 V, No load on OUT | R _{LIM} = 24.9 kΩ | 95 | 120 | μA |
| | | | R _{LIM} = 100 kΩ | 85 | 110 | μA |
| I _{REV} | Reverse leakage current | V _{OUT} = 6.5 V, V _{IN} = 0 V, T _J = 25 °C | | 0.01 | 1 | μA |
| UVLO | Low-level input voltage (IN pin) | V _{IN} rising | | 2.35 | 2.45 | V |
| | UVLO hysteresis (IN pin) ⁽²⁾ | | | 35 | | mV |
| FAULT FLAG | | | | | | |
| V _{OL} | Output low voltage ($\overline{\text{FAULT}}$ pin) | I _{FAULT} = 1 mA | | | 180 | mV |
| | Off-state leakage | V _{FAULT} = 6.5 V | | | 1 | μA |
| | $\overline{\text{FAULT}}$ deglitch | $\overline{\text{FAULT}}$ assertion or deassertion due to overcurrent condition | 6 | 9 | 13 | ms |
| THERMAL SHUTDOWN | | | | | | |
| OTSD2 | Thermal shutdown threshold | | 155 | | | °C |
| OTSD | Thermal shutdown threshold in current-limit | | 135 | | | °C |
| | Hysteresis ⁽²⁾ | | | 20 | | °C |

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be considered separately.

(2) These parameters are provided for reference only, and do not constitute part of TI's published specifications for purposes of TI's product warranty.

7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|------------------|---|---|-------------------------|-----|-----|-----|------|
| t _R | Rise time, output | C _L = 1 μF, R _L = 100 Ω, (see Figure 15) | V _{IN} = 6.5 V | 2 | 3 | 4 | ms |
| | | | V _{IN} = 2.5 V | 1 | 2 | 3 | |
| t _F | Fall time, output | C _L = 1 μF, R _L = 100 Ω, (see Figure 15) | V _{IN} = 6.5 V | 0.6 | 0.8 | 1 | ms |
| | | | V _{IN} = 2.5 V | 0.4 | 0.6 | 0.8 | |
| t _{ON} | Turnon time | C _L = 1 μF, R _L = 100 Ω, (see Figure 15) | | | | 9 | ms |
| t _{OFF} | Turnoff time | C _L = 1 μF, R _L = 100 Ω, (see Figure 15) | | | | 6 | ms |
| t _{IOS} | Response time to short circuit ⁽¹⁾ | V _{IN} = 5 V (see Figure 16) | | | 3.5 | | μs |

(1) These parameters are provided for reference only, and do not constitute part of TI's published specifications for purposes of TI's product warranty.

7.7 Typical Characteristics

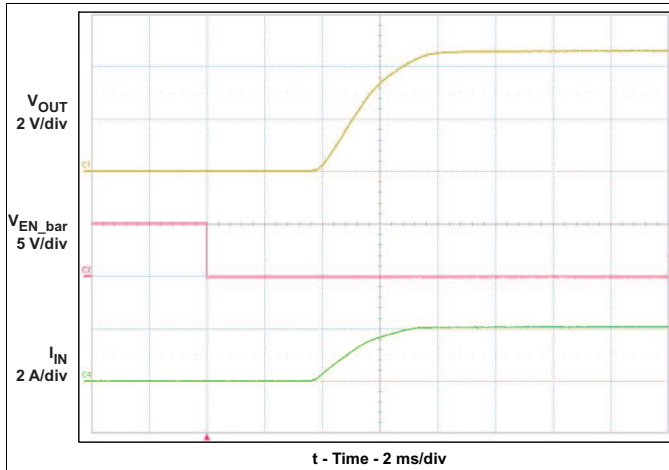


Figure 1. Turnon Delay and Rise Time

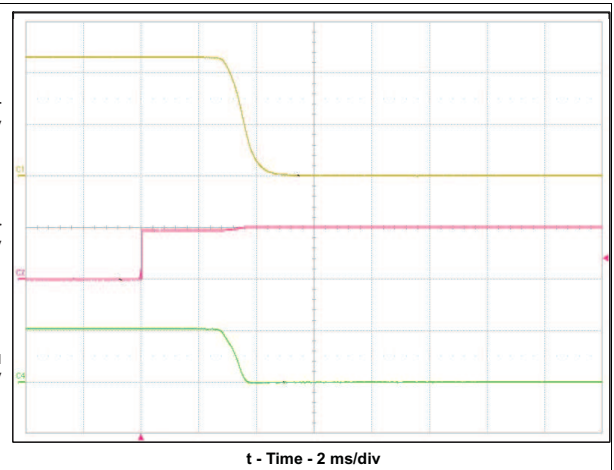


Figure 2. Turnoff Delay and Fall Time

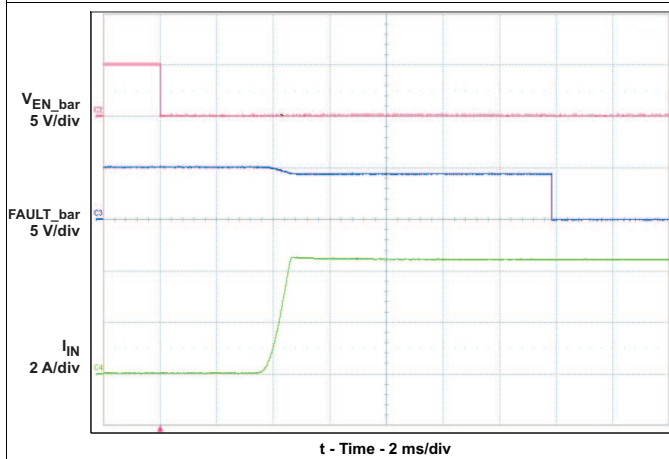


Figure 3. Device Enabled into Short-Circuit

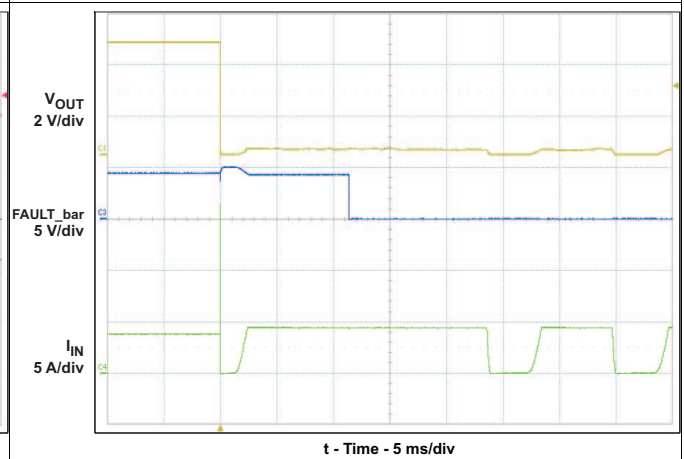


Figure 4. Full-Load to Short-Circuit Transient Response

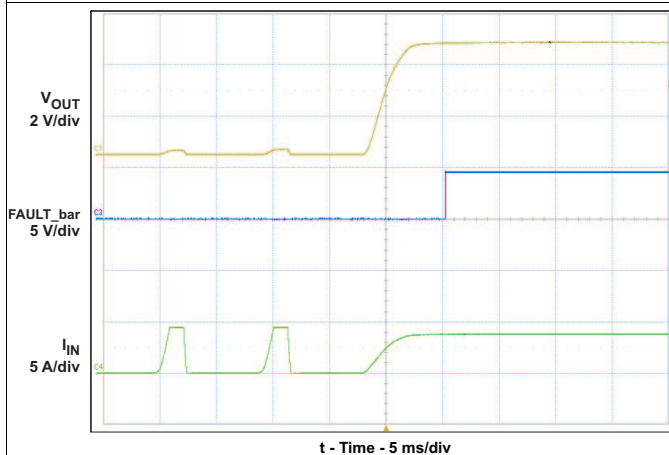


Figure 5. Short-Circuit to Full-Load Recovery Response

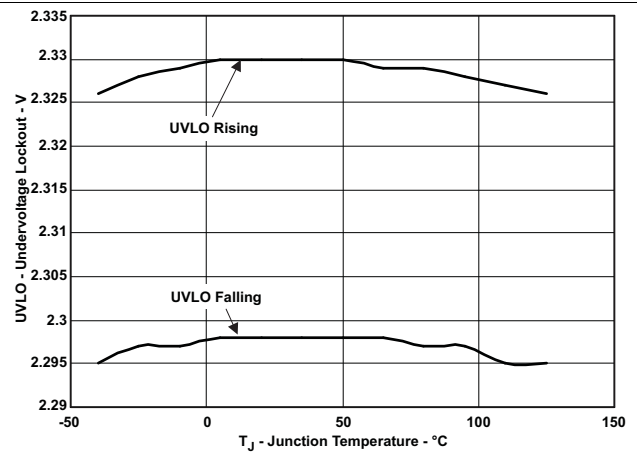


Figure 6. Undervoltage Lockout

Typical Characteristics (continued)

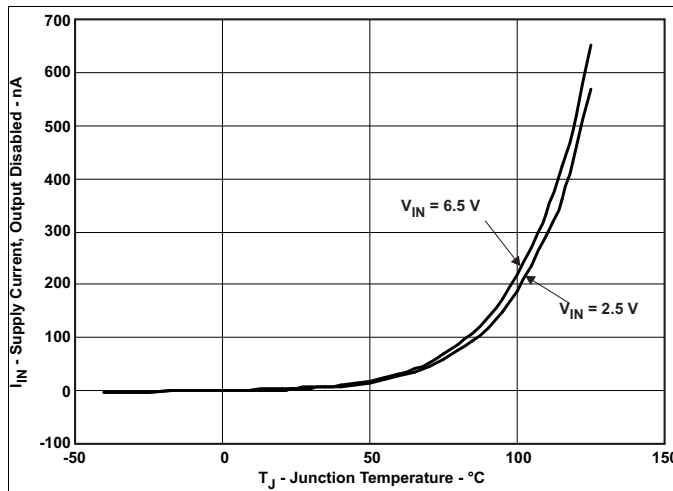


Figure 7. Supply Current, Output Disabled

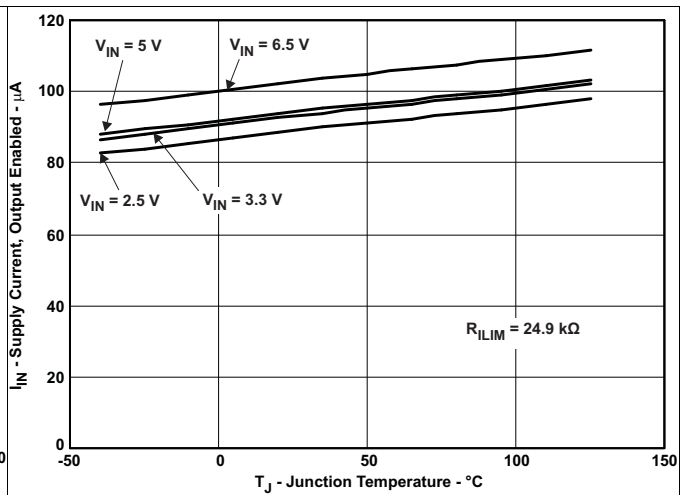


Figure 8. Supply Current, Output Enabled

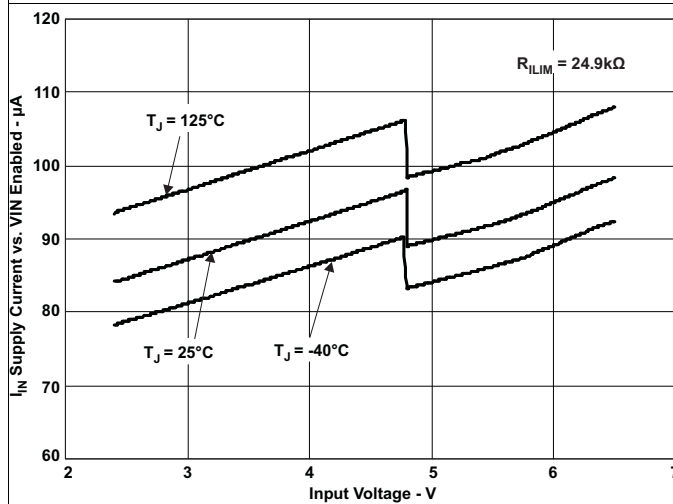


Figure 9. Supply Current, Output Enabled

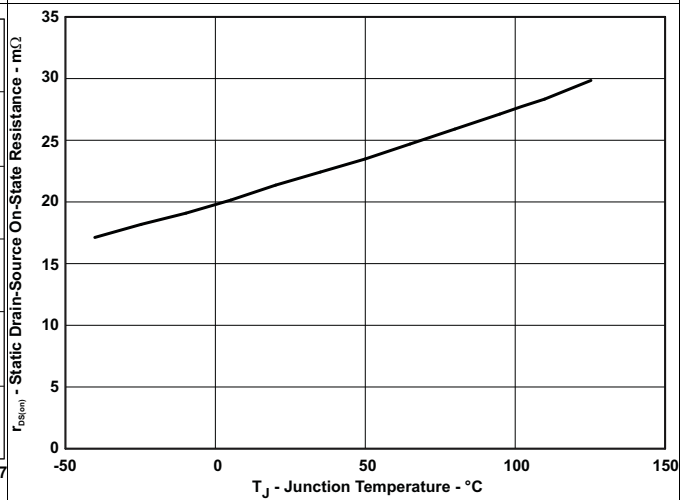


Figure 10. MOSFET $r_{DS(ON)}$ vs Junction Temperature

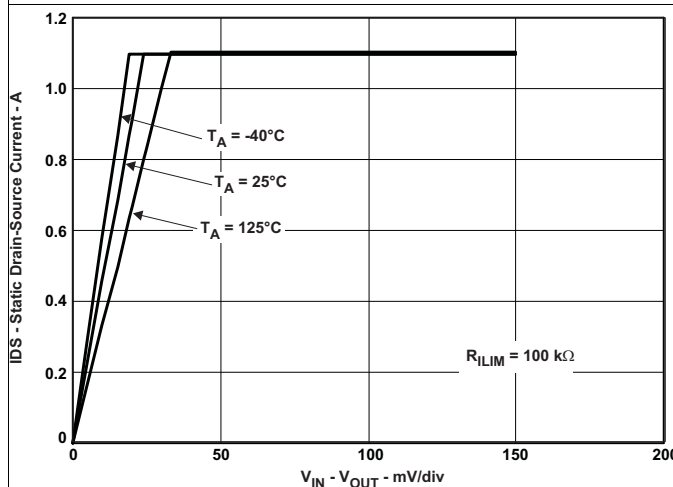


Figure 11. Switch Current vs Drain-Source Voltage Across Switch

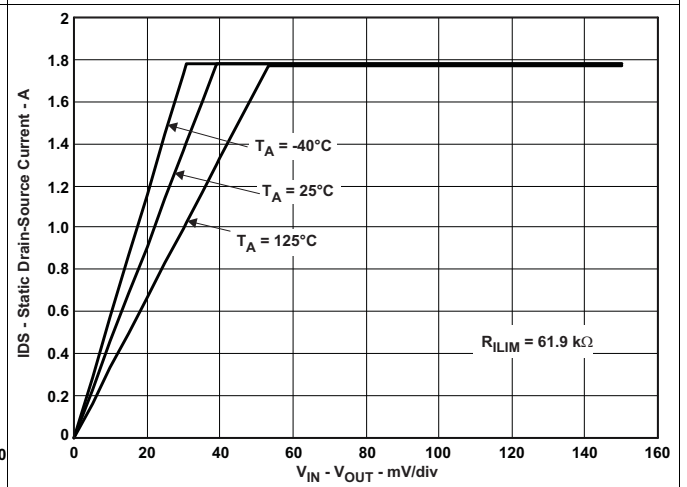


Figure 12. Switch Current vs Drain-Source Voltage Across Switch

Typical Characteristics (continued)

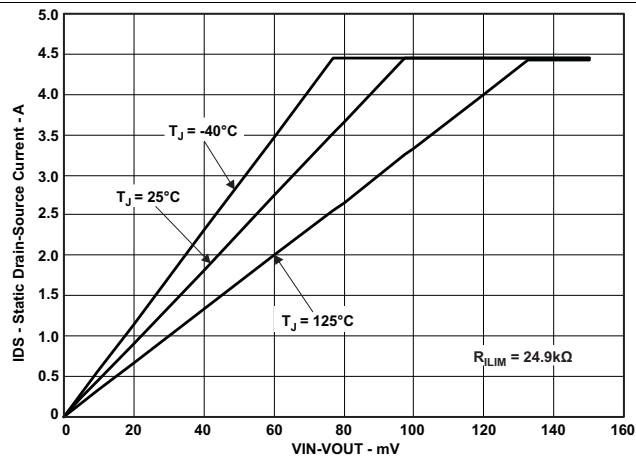


Figure 13. Switch Current vs Drain-Source Voltage Across Switch

8 Parameter Measurement Information

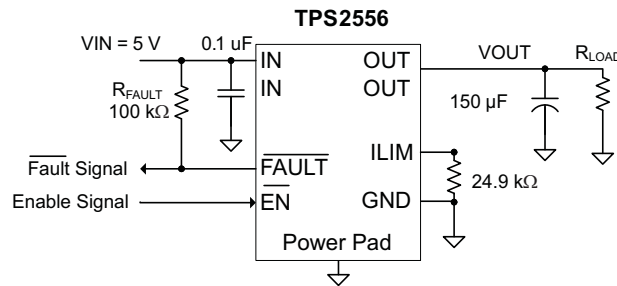


Figure 14. Typical Characteristics Reference Schematic

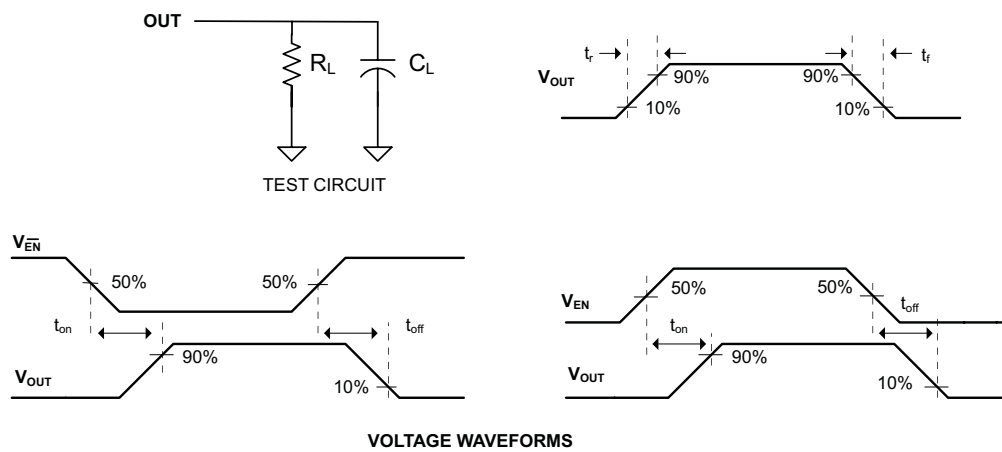


Figure 15. Test Circuit and Voltage Waveforms

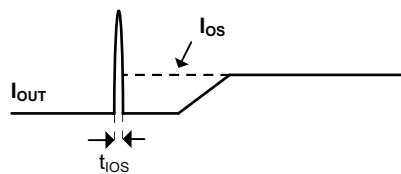


Figure 16. Response Time to Short Circuit Waveform

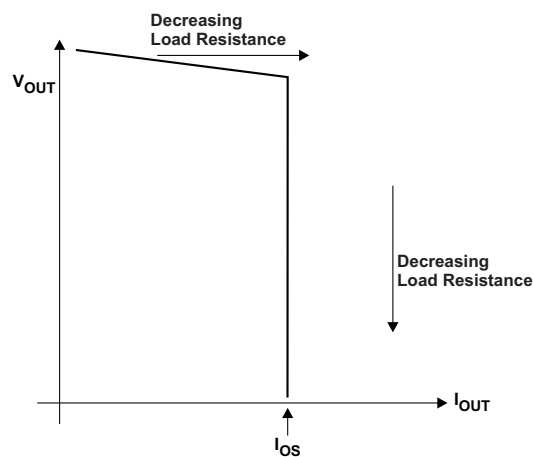


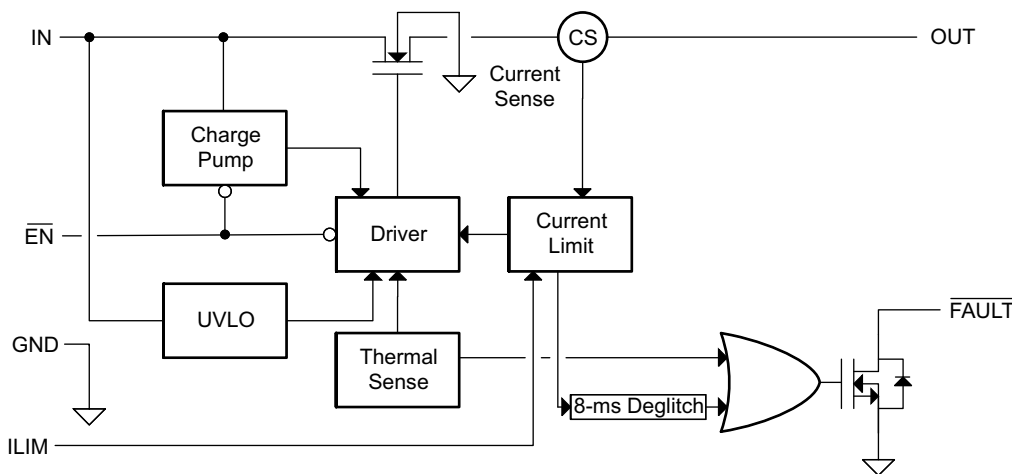
Figure 17. Output Voltage vs Current-Limit Threshold

9 Detailed Description

9.1 Overview

The TPS2556 and TPS2557 are current-limited, power-distribution switches using N-channel MOSFETs for applications where short circuits or heavy capacitive loads are encountered. These devices allow the user to program the current-limit threshold from 500 mA to 5 A (typical) through an external resistor. These devices incorporate an internal charge pump and the gate drive circuitry necessary to drive the N-channel MOSFET. The charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.5 V and requires little supply current. The driver controls the gate voltage of the power switch. The driver incorporates circuitry that controls the rise and fall times of the output voltage to limit large current and voltage surges and provides built-in soft-start functionality. The TPS255x family limits the output current to the programmed current-limit threshold (I_{OS}) during an overcurrent or short-circuit event by reducing the charge pump voltage driving the N-channel MOSFET and operating it in the linear range of operation. The result of limiting the output current to I_{OS} reduces the output voltage at OUT because N-channel MOSFET is no longer fully enhanced.

9.2 Functional Block Diagram



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9.3 Feature Description

9.3.1 Overcurrent Conditions

The TPS255x responds to overcurrent conditions by limiting their output current to I_{OS} . When an overcurrent condition is detected, the device maintains a constant output current and the output voltage reduces accordingly. Two possible overload conditions can occur.

The first condition is when a short circuit or partial short circuit is present when the device is powered up or enabled. The output voltage is held near zero potential with respect to ground and the TPS255x ramps the output current to I_{OS} . The TPS255x limits the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle.

The second condition is when a short circuit, partial short circuit, or transient overload occurs while the device is enabled and powered on. The device responds to the overcurrent condition within time t_{IOS} (see Figure 16). The current-sense amplifier is overdriven during this time and momentarily disables the internal N-channel MOSFET. The current-sense amplifier recovers and ramps the output current to I_{OS} . Similar to the previous case, the TPS255x limits the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle.

The TPS255s thermal cycles if an overload condition is present long enough to activate thermal limiting in any of the above cases. The device turns off when the junction temperature exceeds 135°C (minimum) while in current limit. The device remains off until the junction temperature cools 20°C (typical) and then restarts. The TPS255x cycles on and off until the overload is removed (see Figure 5).

Feature Description (continued)

9.3.2 $\overline{\text{FAULT}}$ Response

The $\overline{\text{FAULT}}$ open-drain output is asserted (active low) during an overcurrent or overtemperature condition. The TPS255s asserts the $\overline{\text{FAULT}}$ signal until the fault condition is removed and the device resumes normal operation. The TPS255s is designed to eliminate false $\overline{\text{FAULT}}$ reporting by using an internal delay *deglitch* circuit for overcurrent (9-ms typical) conditions without the need for external circuitry. This ensures that $\overline{\text{FAULT}}$ is not accidentally asserted due to normal operation such as starting into a heavy capacitive load. The deglitch circuitry delays entering and leaving current-limit induced fault conditions. The $\overline{\text{FAULT}}$ signal is not deglitched when the MOSFET is disabled due to an overtemperature condition but is deglitched after the device has cooled and begins to turn on. This unidirectional deglitch prevents $\overline{\text{FAULT}}$ oscillation during an overtemperature event.

9.3.3 Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turnon threshold. Built-in hysteresis prevents unwanted on and off cycling due to input voltage droop during turnon.

9.3.4 Enable ($\overline{\text{EN}}$ OR EN)

The logic enable controls the power switch and device supply current. The supply current is reduced to less than 2- μA when a logic high is present on $\overline{\text{EN}}$ or when a logic low is present on EN. A logic low input on $\overline{\text{EN}}$ or a logic high input on EN enables the driver, control circuits, and power switch. The enable input is compatible with both TTL and CMOS logic levels.

9.3.5 Thermal Sense

The TPS255x self-protects by using two independent thermal sensing circuits that monitor the operating temperature of the power switch and disable operation if the temperature exceeds recommended operating conditions. The TPS255x operates in constant-current mode during an overcurrent conditions, which increases the voltage drop across power switch. The power dissipation in the package is proportional to the voltage drop across the power switch, which increases the junction temperature during an overcurrent condition. The first thermal sensor (OTSD) turns off the power switch when the die temperature exceeds 135°C (minimum) and the part is in current limit. Hysteresis is built into the thermal sensor, and the switch turns on after the device has cooled approximately 20°C.

The TPS255x also has a second ambient thermal sensor (OTSD2). The ambient thermal sensor turns off the power switch when the die temperature exceeds 155°C (minimum) regardless of whether the power switch is in current limit and turns on the power switch after the device has cooled approximately 20°C. The TPS255x continues to cycle off and on until the fault is removed.

9.4 Device Functional Modes

There are no other functional modes.

10 Application and Implementation

NOTE

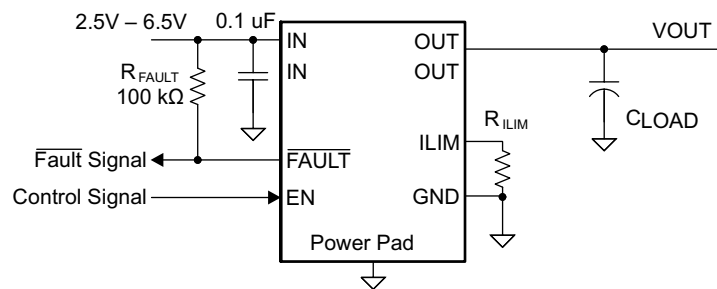
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS2556 and TPS2557 are precision power-distribution switches for applications where heavy capacitive loads and short circuits are expected to be encountered. The following design procedures can be used to choose the input and output capacitors as well as to calculate the current limit programming resistor value for a typical design. Additional application examples are provided including an auto-retry circuit and a two-level current limit circuit.

10.2 Typical Applications

10.2.1 Current-Limiting Power-Distribution Switch



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Figure 18. Typical Current-Limiting Application

10.2.1.1 Design Requirements

For this example, use the parameters listed in [Table 1](#) as the input parameters.

Table 1. Design Parameters

| PARAMETER | VALUE |
|-------------------------------|---------|
| Input voltage | 5 V |
| Output voltage | 5 V |
| Above a minimum current limit | 3000 mA |
| Below a maximum current limit | 5000 mA |

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Input and Output Capacitance

Input and output capacitance improves the performance of the device; the actual capacitance must be optimized for the particular application. TI recommends a 0.1- μ F or greater ceramic bypass capacitor between IN and GND as close to the device as possible for local noise decoupling for all applications. This precaution reduces ringing on the input due to power-supply transients. Additional input capacitance may be needed on the input to reduce voltage overshoot from exceeding the absolute-maximum voltage of the device during heavy transient conditions. This is especially important during bench testing when long, inductive cables are used to connect the evaluation board to the bench power supply.

Output capacitance is not required, but TI recommends placing a high-value electrolytic capacitor on the output pin when large transient currents are expected on the output.

10.2.1.2.2 Programming the Current-Limit Threshold

The overcurrent threshold is user programmable through an external resistor. The TPS255x uses an internal regulation loop to provide a regulated voltage on the ILIM pin. The current-limit threshold is proportional to the current sourced out of ILIM. The recommended 1% resistor for R_{ILIM} is $20\text{ k}\Omega \leq R_{ILIM} \leq 187\text{ k}\Omega$ to ensure stability of the internal regulation loop. Many applications require that the minimum current limit is above a certain current level or that the maximum current limit is below a certain current level, so it is important to consider the tolerance of the overcurrent threshold when selecting a value for R_{ILIM} . Equation 1 approximates the resulting overcurrent threshold for a given external resistor value (R_{ILIM}). See [Electrical Characteristics](#) for specific current limit settings. The traces routing the R_{ILIM} resistor to the TPS255x must be as short as possible to reduce parasitic effects on the current-limit accuracy.

$$\begin{aligned}
 I_{OSmax}(\text{mA}) &= \frac{99038\text{V}}{R_{ILIM}^{0.947}\text{k}\Omega} \\
 I_{OSnom}(\text{mA}) &= \frac{111704\text{V}}{R_{ILIM}^{1.0028}\text{k}\Omega} \\
 I_{OSmin}(\text{mA}) &= \frac{127981\text{V}}{R_{ILIM}^{1.0708}\text{k}\Omega}
 \end{aligned}
 \tag{1}$$

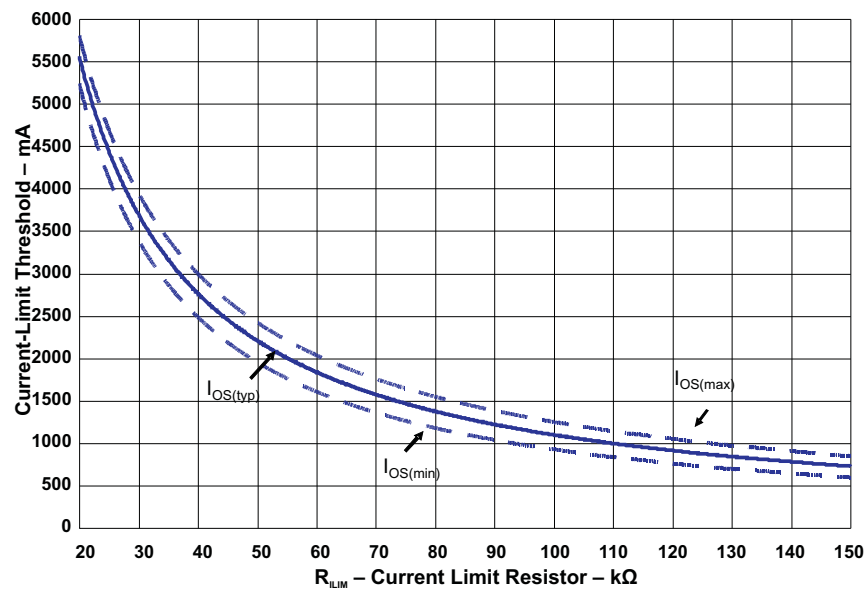


Figure 19. Current-Limit Threshold vs R_{ILIM}

10.2.1.2.2.1 Designing Above a Minimum Current Limit

Some applications require that current limiting cannot occur below a certain threshold. For this example, assume that 3 A must be delivered to the load so that the minimum desired current-limit threshold is 3000 mA. Use the I_{OS} equations and [Figure 19](#) to select R_{ILIM} .

$$\begin{aligned}
 I_{OSmin}(\text{mA}) &= 3000\text{mA} \\
 I_{OSmin}(\text{mA}) &= \frac{127981\text{V}}{R_{ILIM}^{1.0708}\text{k}\Omega} \\
 R_{ILIM}(\text{k}\Omega) &= \left(\frac{127981\text{V}}{I_{OSmin}\text{mA}} \right)^{\frac{1}{1.0708}} \\
 R_{ILIM}(\text{k}\Omega) &= 33.3\text{k}\Omega
 \end{aligned} \tag{2}$$

Select the closest 1% resistor less than the calculated value: $R_{ILIM} = 33.2 \text{ k}\Omega$. This sets the minimum current-limit threshold at 3000 mA. Use the I_{OS} equations, [Figure 19](#), and the previously calculated value for R_{ILIM} to calculate the maximum resulting current-limit threshold.

$$\begin{aligned}
 R_{ILIM}(\text{k}\Omega) &= 33.2\text{k}\Omega \\
 I_{OSmax}(\text{mA}) &= \frac{99038\text{V}}{R_{ILIM}^{0.947}\text{k}\Omega} \\
 I_{OSmax}(\text{mA}) &= \frac{99038\text{V}}{33.2^{0.947}\text{k}\Omega} \\
 I_{OSmax}(\text{mA}) &= 3592\text{mA}
 \end{aligned} \tag{3}$$

The resulting maximum current-limit threshold is 3592 mA with a 33.2-k Ω resistor.

10.2.1.2.2.2 Designing Below a Maximum Current Limit

Some applications require that current limiting must occur below a certain threshold. For this example, assume that the desired upper current-limit threshold must be below 5000 mA to protect an upstream power supply. Use the I_{OS} equations and [Figure 19](#) to select R_{ILIM} .

$$\begin{aligned}
 I_{OSmax}(\text{mA}) &= 5000\text{mA} \\
 I_{OSmax}(\text{mA}) &= \frac{99038\text{V}}{R_{ILIM}^{0.947}\text{k}\Omega} \\
 R_{ILIM}(\text{k}\Omega) &= \left(\frac{99038\text{V}}{I_{OSmax}\text{mA}} \right)^{\frac{1}{0.947}} \\
 R_{ILIM}(\text{k}\Omega) &= 23.4\text{k}\Omega
 \end{aligned} \tag{4}$$

Select the closest 1% resistor greater than the calculated value: $R_{ILIM} = 23.7 \text{ k}\Omega$. This sets the maximum current-limit threshold at 5000 mA. Use the I_{OS} equations, [Figure 19](#), and the previously calculated value for R_{ILIM} to calculate the minimum resulting current-limit threshold.

$$\begin{aligned}
 R_{ILIM}(\text{k}\Omega) &= 23.7\text{k}\Omega \\
 I_{OSmin}(\text{mA}) &= \frac{127981\text{V}}{R_{ILIM}^{1.0708}\text{k}\Omega} \\
 I_{OSmin}(\text{mA}) &= \frac{127981\text{V}}{23.7^{1.0708}\text{k}\Omega} \\
 I_{OSmin}(\text{mA}) &= 4316\text{mA}
 \end{aligned} \tag{5}$$

The resulting minimum current-limit threshold is 4316 mA with a 23.7-k Ω resistor.

10.2.1.2.2.3 Accounting for Resistor Tolerance

The analysis of resistor selection focused only on the TPS255x performance and assumed an exact resistor value. However, resistors sold in quantity are not exact and are bounded by an upper and lower tolerance centered around a nominal resistance. The additional R_{ILIM} resistance tolerance directly affects the current-limit threshold accuracy at a system level. Table 2 shows a process that accounts for worst-case resistor tolerance assuming 1% resistor values. Using the selection process outlined, determine the upper and lower resistance bounds of the selected resistor. Then calculate the upper and lower resistor bounds to determine the threshold limits. It is important to use tighter tolerance resistors (0.5% or 0.1%) when precision current limiting is desired.

Table 2. Common R_{ILIM} Resistor Selections

| DESIRED NOMINAL CURRENT LIMIT (mA) | IDEAL RESISTOR (k Ω) | CLOSEST 1% RESISTOR (k Ω) | RESISTOR BOUNDS (k Ω) | | I_{OS} ACTUAL LIMITS (mA) | | |
|------------------------------------|------------------------------|-----------------------------------|-------------------------------|---------|-----------------------------|------|------|
| | | | 1% LOW | 1% HIGH | MIN | NOM | MAX |
| 750 | 146.9 | 147 | 145.5 | 148.5 | 605 | 749 | 886 |
| 1000 | 110.2 | 110 | 108.9 | 111.1 | 825 | 1002 | 1166 |
| 1250 | 88.2 | 88.7 | 87.8 | 89.6 | 1039 | 1244 | 1430 |
| 1500 | 73.6 | 73.2 | 72.5 | 73.9 | 1276 | 1508 | 1715 |
| 1750 | 63.1 | 63.4 | 62.8 | 64 | 1489 | 1742 | 1965 |
| 2000 | 55.2 | 54.9 | 54.4 | 55.4 | 1737 | 2012 | 2252 |
| 2250 | 49.1 | 48.7 | 48.2 | 49.2 | 1975 | 2269 | 2523 |
| 2500 | 44.2 | 44.2 | 43.8 | 44.6 | 2191 | 2501 | 2765 |
| 2750 | 40.2 | 40.2 | 39.8 | 40.6 | 2425 | 2750 | 3025 |
| 3000 | 36.9 | 36.5 | 36.1 | 36.9 | 2689 | 3030 | 3315 |
| 3250 | 34 | 34 | 33.7 | 34.3 | 2901 | 3253 | 3545 |
| 3500 | 31.6 | 31.6 | 31.3 | 31.9 | 3138 | 3501 | 3800 |
| 3750 | 29.5 | 29.4 | 29.1 | 29.7 | 3390 | 3764 | 4068 |
| 4000 | 27.7 | 27.4 | 27.1 | 27.7 | 3656 | 4039 | 4349 |
| 4250 | 26 | 26.1 | 25.8 | 26.4 | 3851 | 4241 | 4554 |
| 4500 | 24.6 | 24.9 | 24.7 | 25.1 | 4050 | 4446 | 4761 |
| 4750 | 23.3 | 23.2 | 23 | 23.4 | 4369 | 4773 | 5091 |
| 5000 | 22.1 | 22.1 | 21.9 | 22.3 | 4602 | 5011 | 5331 |
| 5250 | 21.1 | 21 | 20.8 | 21.2 | 4861 | 5274 | 5595 |
| 5500 | 20.1 | 20 | 19.8 | 20.2 | 5121 | 5539 | 5859 |

10.2.1.2.3 Auto-Retry Functionality

Some applications require that an overcurrent condition disables the part momentarily during a fault condition and re-enables after a pre-set time. This *auto-retry* functionality can be implemented with an external resistor and capacitor. During a fault condition, \overline{FAULT} pulls EN low. The part is disabled when EN is pulled below the turn-off threshold, and \overline{FAULT} goes high impedance allowing C_{RETRY} to begin charging. The part re-enables when the voltage on EN reaches the turn-on threshold. The auto-retry time is determined by the resistor and capacitor time constant. The part continues to cycle in this manner until the fault condition is removed. The time between retries is given in Equation 6.

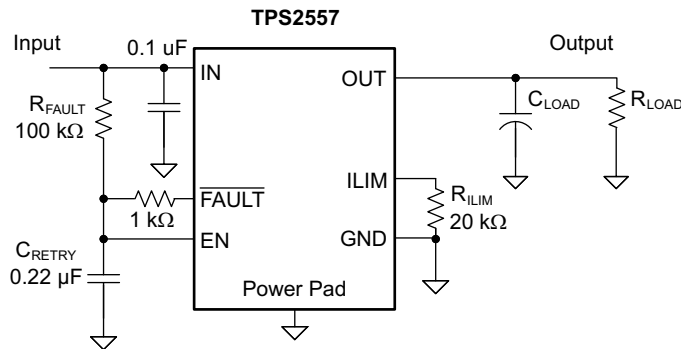
$$T_{BR} = -R_{FAULT} \times C_{RETRY} \times \text{LN} (1 - V_{EN} / (V_{IN} - V_{OL})) + T_{FAULT}$$

where

- V_{EN} is the EN pin typical threshold voltage
- V_{IN} is the input voltage
- V_{OL} is the \overline{FAULT} pin typical saturation voltage
- T_{FAULT} is the internal \overline{FAULT} typical deglitch time

The retry duty cycle is calculated with Equation 7, and the average current is $D \times I_{OS}$.

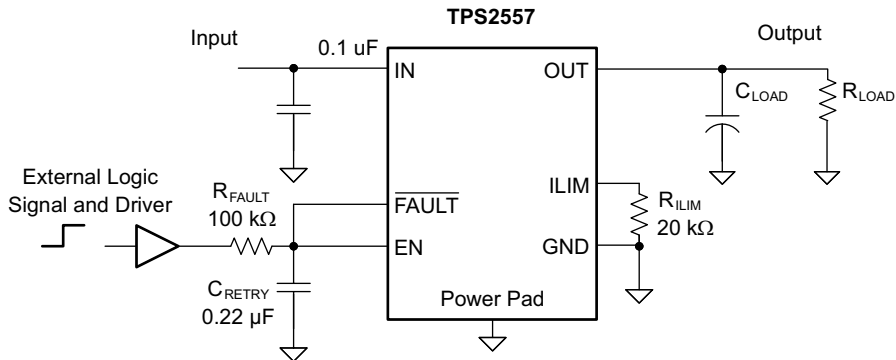
$$D = T_{FAULT} / (T_{FAULT} + T_{BR})$$



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Figure 20. Auto-Retry Functionality

Some applications require auto-retry functionality and the ability to enable and disable with an external logic signal. The figure below shows how an external logic signal can drive EN through R_{FAULT} and maintain auto-retry functionality. The resistor and capacitor time constant determines the auto-retry time-out period.



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Figure 21. Auto-Retry Functionality With External EN Signal

10.2.1.2.4 Two-Level Current-Limit Circuit

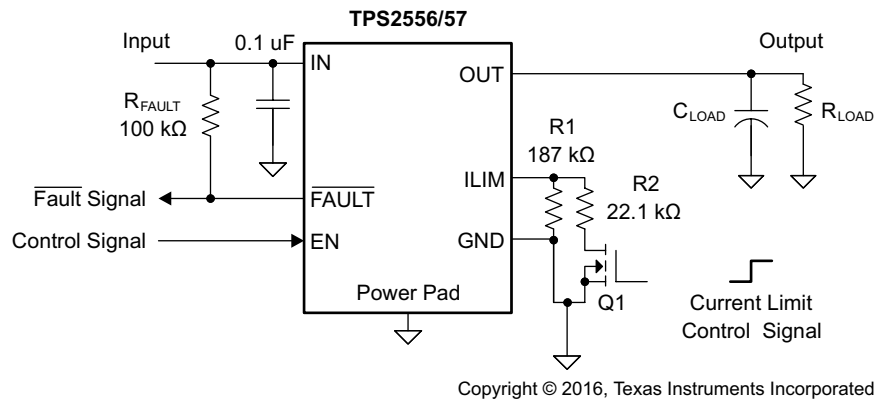


Figure 22. Two-Level Current-Limit Circuit

Some applications require different current-limit thresholds depending on external system conditions. Figure 22 shows an implementation for an externally-controlled, two-level current-limit circuit. The current-limit threshold is set by the total resistance from ILIM to GND (see [Programming the Current-Limit Threshold](#)). A logic-level input enables and disables MOSFET Q1 and changes the current-limit threshold by modifying the total resistance from ILIM to GND. Additional MOSFET and resistor combinations can be used in parallel to Q1 and R2 to increase the number of additional current-limit levels.

NOTE

ILIM must never be driven directly with an external signal.

10.2.1.3 Application Curve

In Figure 23, the load current setpoint is 5.05 A, as programmed by the 22.1-kΩ resistor. Load current is stepped mildly from approximately 4.9 A to 5.2 A. The internal FAULT timer runs and after 9 ms, FAULT goes low and current continues to be regulated at approximately 5 A. Due to the high power dissipation within the device, thermal cycling occurs.

In Figure 24, the load current setpoint is 597 mA, as programmed by the 187-kΩ resistor. Load current is stepped mildly from approximately 560 mA to 620 mA. The internal FAULT timer runs and after 9 ms, FAULT goes low and current continues to be regulated at approximately 580 mA.

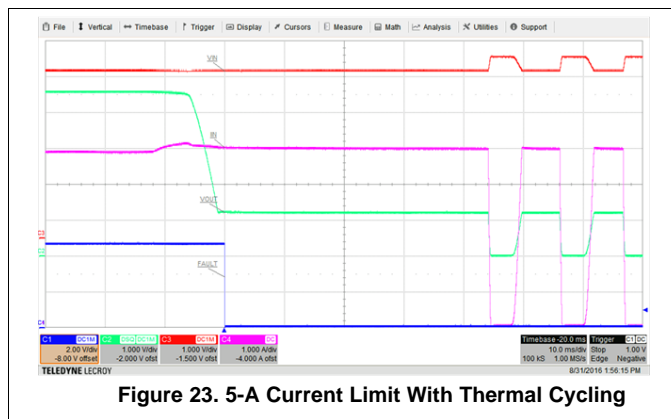


Figure 23. 5-A Current Limit With Thermal Cycling

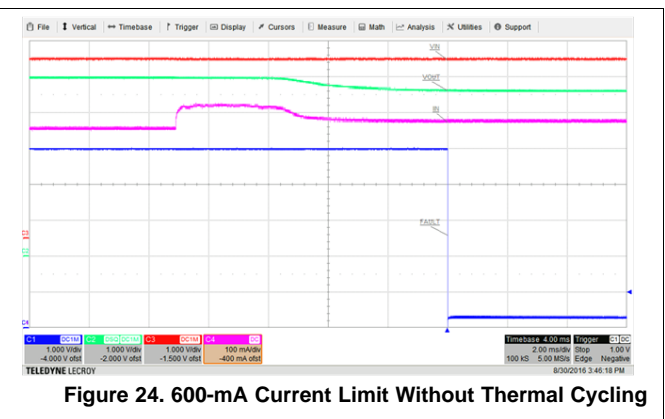


Figure 24. 600-mA Current Limit Without Thermal Cycling

11 Power Supply Recommendations

The TPS255x operates from 2.5 V to 6.5 V. TI recommends operating from either a 3.3-V ± 10% or 5-V ± 10% power supply. The load capacity of the power supply must be greater than the maximum current limit (I_{OS}) setting of the TPS255x.

12 Layout

12.1 Layout Guidelines

- TI recommends placing the 100-nF bypass capacitor near the IN and GND pins, and make the connections using a low-inductance trace.
- TI recommends placing a high-value electrolytic capacitor and a 100-nF bypass capacitor on the output pin when large transient currents are expected on the output.
- The traces routing the R_{ILIM} resistor to the device must be as short as possible to reduce parasitic effects on the current limit accuracy.
- The PowerPAD must be directly connected to PCB ground plane using wide and short copper trace.

12.2 Layout Example

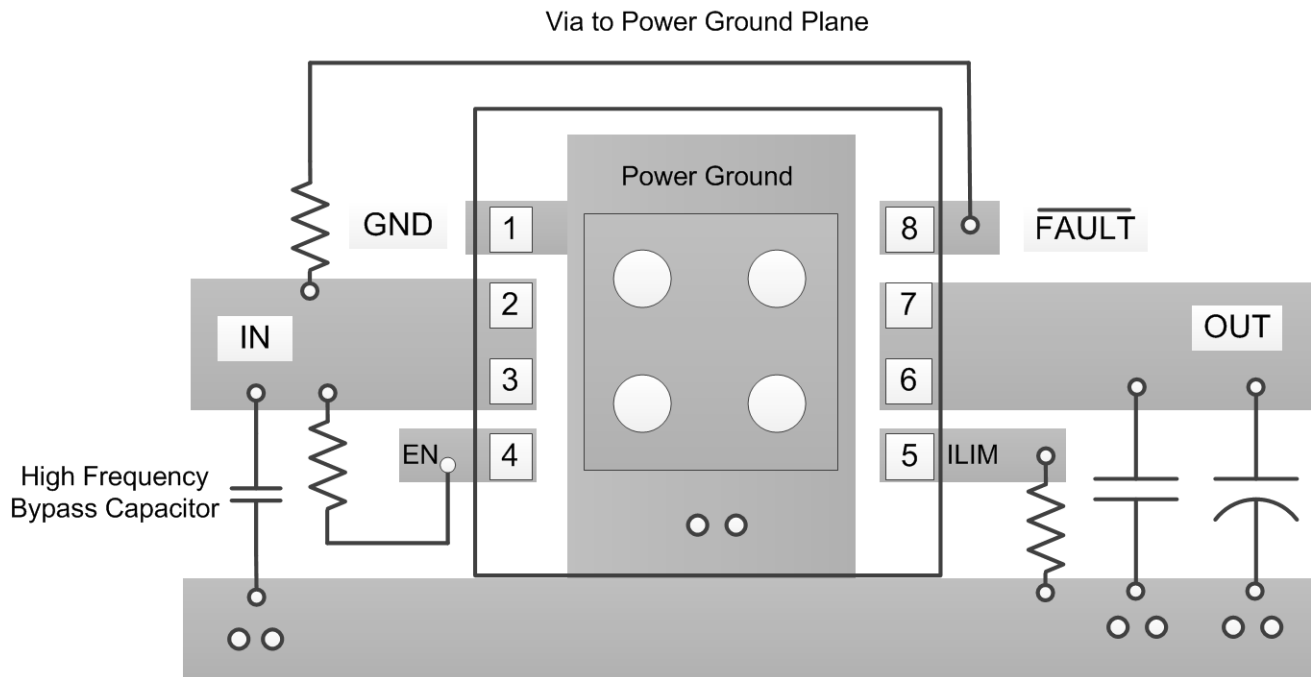


Figure 25. TPS255x Layout Example

12.3 Thermal Considerations

The low on-resistance of the N-channel MOSFET allows small surface-mount packages to pass large currents. It is good design practice to estimate power dissipation and junction temperature. This analysis gives an approximation for calculating junction temperature based on the power dissipation in the package. However, thermal analysis is strongly dependent on additional system level factors. Such factors include air flow, board layout, copper thickness and surface area, and proximity to other devices dissipating power. Good thermal design practice must include all system level factors in addition to individual component analysis.

Begin by determining the $r_{DS(ON)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(ON)}$ from the typical characteristics graph. Using this value, the power dissipation can be calculated by [Equation 8](#).

$$P_D = r_{DS(ON)} \times I_{OUT}^2$$

where

- P_D = Total power dissipation (W)
- $r_{DS(ON)}$ = Power switch on-resistance (Ω)
- I_{OUT} = Maximum current-limit threshold (A) (8)

Finally, calculate the junction temperature with [Equation 9](#).

$$T_J = P_D \times R_{\theta JA} + T_A$$

where

- T_A = Ambient temperature ($^{\circ}\text{C}$)
- $R_{\theta JA}$ = Thermal resistance ($^{\circ}\text{C}/\text{W}$)
- P_D = Total power dissipation (W) (9)

Compare the calculated junction temperature with the initial estimate. If they are not within a few degrees, repeat the calculation using the *refined* $r_{DS(ON)}$ from the previous calculation as the new estimate. Two or three iterations are generally sufficient to achieve the desired result. The final junction temperature is highly dependent on thermal resistance, and thermal resistance is highly dependent on the individual package and board layout.

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| TPS2556 | Click here | Click here | Click here | Click here | Click here |
| TPS2557 | Click here | Click here | Click here | Click here | Click here |

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS2556DRBR | ACTIVE | SON | DRB | 8 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2556 | Samples |
| TPS2556DRBT | ACTIVE | SON | DRB | 8 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2556 | Samples |
| TPS2557DRBR | ACTIVE | SON | DRB | 8 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2557 | Samples |
| TPS2557DRBT | ACTIVE | SON | DRB | 8 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2557 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS2556, TPS2557 :

- Automotive : [TPS2556-Q1](#), [TPS2557-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS2556DRBR | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS2556DRBR | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS2556DRBT | SON | DRB | 8 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS2556DRBT | SON | DRB | 8 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS2557DRBR | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS2557DRBT | SON | DRB | 8 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

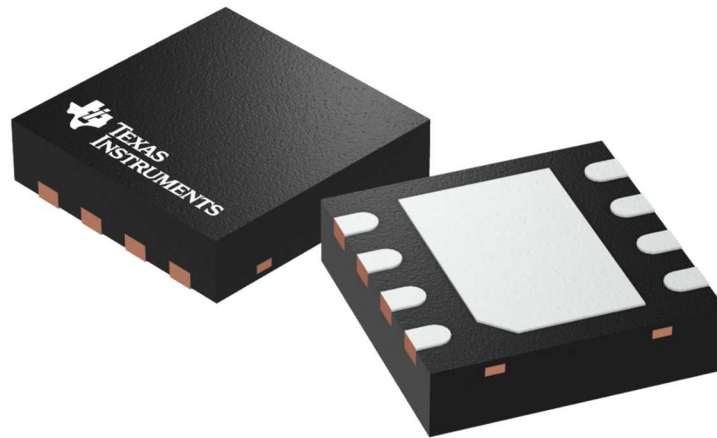
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS2556DRBR | SON | DRB | 8 | 3000 | 346.0 | 346.0 | 33.0 |
| TPS2556DRBR | SON | DRB | 8 | 3000 | 367.0 | 367.0 | 35.0 |
| TPS2556DRBT | SON | DRB | 8 | 250 | 210.0 | 185.0 | 35.0 |
| TPS2556DRBT | SON | DRB | 8 | 250 | 210.0 | 185.0 | 35.0 |
| TPS2557DRBR | SON | DRB | 8 | 3000 | 346.0 | 346.0 | 33.0 |
| TPS2557DRBT | SON | DRB | 8 | 250 | 210.0 | 185.0 | 35.0 |

DRB 8

GENERIC PACKAGE VIEW

VSON - 1 mm max height

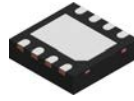
PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L

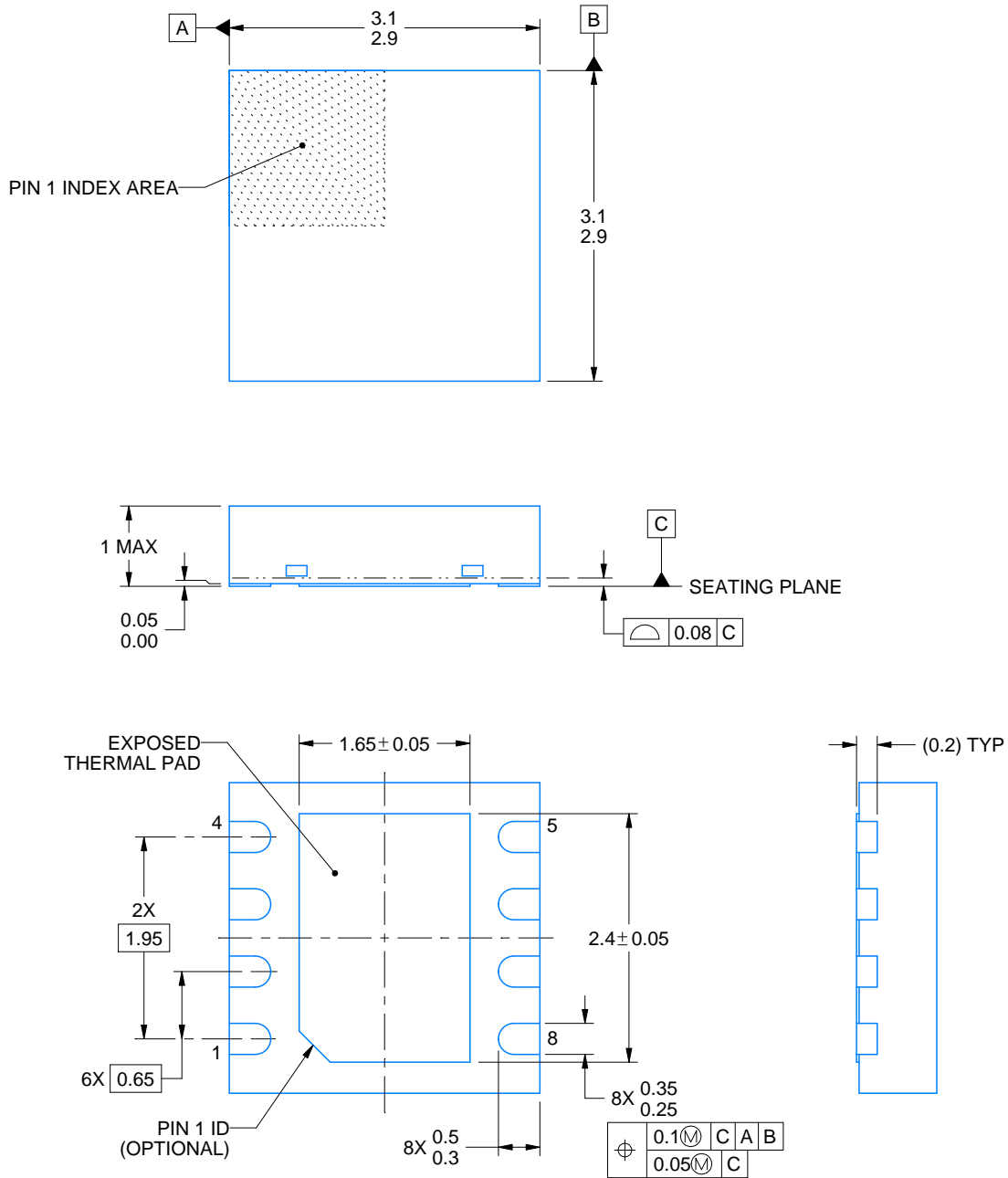
DRB0008B



PACKAGE OUTLINE

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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NOTES:

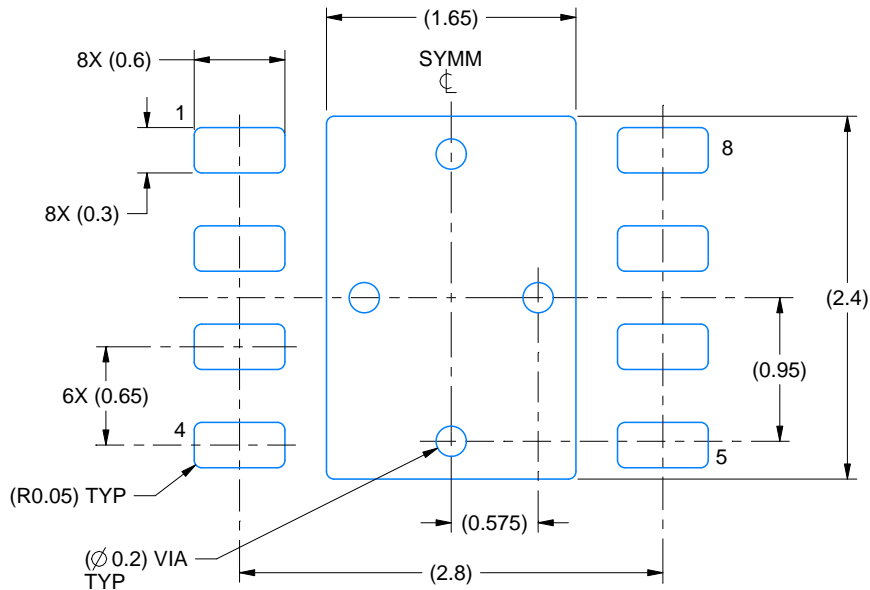
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

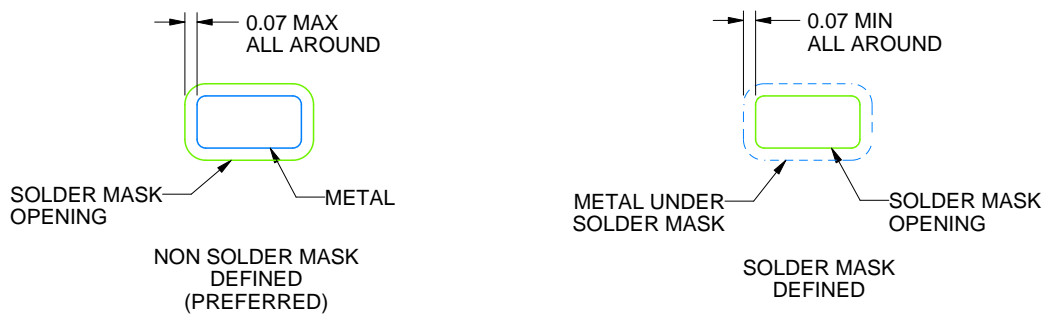
DRB0008B

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4218876/A 12/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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