TPS61251 Boost Converter for Battery Backup Charging With Adjustable Constant Current and Snooze Mode

1 Features

- Resistor Programmable Input Current Limit
  - ±10% Current Accuracy at 500 mA over Full Temperature Range
  - Programmable from 100 mA up to 1500 mA
- Snooze Mode Draws Only 2 µA (Typical) Quiescent Current
- Designed to Charge Large Capacitor Values in the Farad Range
- Up to 92% Efficiency
- Power Good Indicates Appropriate Output Voltage Level even in Shut Down
- VIN Range from 2.3 V to 6 V
- Adjustable Output Voltage up to 6.5 V
- 100% Duty-Cycle Mode When VIN > VOUT
- Load Disconnect and Reverse Current Protection
- Short-Circuit Protection
- Typical Operating Frequency 3.5 MHz
- Available in a 2 × 2-mm WSON-8 Package

2 Applications

- Current Limited Applications With High Peak Power Loads (SSD, PCMCIA Tx Bursts, Memory, GPRS/GSM Tx)
- Li-Ion Applications
- Battery Backup Applications
- Audio Applications
- RF-PA Buffer

3 Description

The TPS61251 device provides a power supply solution for products powered by either a three-cell, NiCd or NiMH battery, or a one-cell Li-Ion or Li-polymer battery. The wide input voltage range is ideal to power portable applications like mobile phones, solid state drives (SSD) and wireless modems. The converter is designed to charge large capacitors in the Farad range to support battery back up applications. During capacitor charging, the TPS61251 device is working as a constant current source until VOUT has reached its programmed value. The charge current can be programmed by an external resistor RILIM and provides a ±10% accuracy for the average input current limit.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS61251</td>
<td>WSON (8)</td>
<td>2.00 mm × 2.00 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.
Table of Contents

1 Features ..................................................................... 1
2 Applications ................................................................. 1
3 Description ................................................................... 1
4 Revision History ............................................................. 2
5 Description (Continued) .................................................. 3
6 Device Options .............................................................. 3
7 Pin Configuration and Functions ......................................... 3
8 Specifications ............................................................... 4
  8.1 Absolute Maximum Ratings ........................................ 4
  8.2 ESD Ratings ............................................................. 4
  8.3 Recommended Operating Conditions ............................ 4
  8.4 Thermal Information ................................................ 4
  8.5 Electrical Characteristics .......................................... 5
  8.6 Typical Characteristics ............................................ 5
9 Detailed Description ..................................................... 7
  9.1 Overview ............................................................... 7
  9.2 Functional Block Diagram ......................................... 8
  9.3 Feature Description ................................................ 8
  9.4 Device Functional Modes .......................................... 10
10 Application and Implementation ........................................ 11
  10.1 Application Information .......................................... 11
  10.2 Typical Application ............................................... 11
11 Power Supply Recommendations .................................... 16
12 Layout .................................................................... 16
  12.1 Layout Guidelines ................................................. 16
  12.2 Layout Example .................................................. 16
  12.3 Thermal Consideration .......................................... 17
13 Device and Documentation Support ................................. 18
  13.1 Device Support .................................................... 18
  13.2 Community Resource ........................................... 18
  13.3 Trademarks .......................................................... 18
  13.4 Electrostatic Discharge Caution ................................. 18
  13.5 Glossary ............................................................. 18
14 Mechanical, Packaging, and Orderable Information .......... 18

4 Revision History

Changes from Revision A (May 2015) to Revision B Page

• Deleted package suffix from device number in the Device Options table. ................................................................. 3

Changes from Original (September 2010) to Revision A Page

• Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ................................................................................................. 1
5 Description (Continued)
The TPS61251 device in combination with a reservoir capacitor allows the converter to provide high current pulses that would exceed the capability of the supplying circuit (PC slot, USB) and keeps the slot power safely within its capabilities. During light loads the device will automatically enter an enhanced power save mode (Snooze Mode), which allows the converter to maintain the required output voltage, while only drawing 2 μA from the battery. This will allow maximum efficiency at lowest quiescent currents.

TPS61251 device allows the use of small inductors and input capacitors to achieve a small solution size. During shutdown, the load is completely disconnected from the battery and will not discharge either the battery nor the charged bulk capacitor. The TPS61251 device is available in a 8-pin QFN package measuring 2 × 2 mm (DSG).

6 Device Options

<table>
<thead>
<tr>
<th>OUTPUT VOLTAGE(1)</th>
<th>PART NUMBER(2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Adjustable</td>
<td>TPS61251</td>
</tr>
</tbody>
</table>

(1) Contact TI for other fixed output voltage options
(2) For detailed ordering information please check the Mechanical, Packaging, and Orderable Information section at the end of this data sheet.

7 Pin Configuration and Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN</td>
<td>6</td>
<td>Enable input (1 enabled, 0 disabled)</td>
</tr>
<tr>
<td>FB</td>
<td>3</td>
<td>Voltage feedback pin</td>
</tr>
<tr>
<td>GND</td>
<td>1</td>
<td>Ground</td>
</tr>
<tr>
<td>ILIM</td>
<td>4</td>
<td>Adjustable average input current limit. Can be connected to ( V_{IN} ) for maximum current limit or to GND for minimum current limit.</td>
</tr>
<tr>
<td>PG</td>
<td>5</td>
<td>Output power good (1 good, 0 failure; open drain)</td>
</tr>
<tr>
<td>SW</td>
<td>7</td>
<td>Connection for Inductor</td>
</tr>
<tr>
<td>VIN</td>
<td>8</td>
<td>Supply voltage for power stage</td>
</tr>
<tr>
<td>VOUT</td>
<td>2</td>
<td>Boost converter output</td>
</tr>
</tbody>
</table>

Exposed Thermal Pad

Must be soldered to achieve appropriate power dissipation and for mechanical reasons. Must be connected to GND.
8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>Voltage(^{(2)})</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN, VOUT, SW, EN, PG, FB, ILIM</td>
<td>–0.3</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>Temperature</td>
<td>Operating junction, (T_J)</td>
<td>–40</td>
<td>150</td>
</tr>
<tr>
<td>Storage, (T_{stg})</td>
<td>–65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to network ground terminal.

8.2 ESD Ratings

<table>
<thead>
<tr>
<th>(V_{(ESD)})</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(^{(1)})</td>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td>Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(^{(2)})</td>
<td>±500</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage at VIN</td>
<td>2.3</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>Output voltage at VOUT</td>
<td>3</td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td>Programable input current limit set by (R_{ILIM})</td>
<td>100</td>
<td>1500</td>
<td>mA</td>
</tr>
<tr>
<td>Operating free air temperature, (T_A)</td>
<td>–40</td>
<td>85</td>
<td>°C</td>
</tr>
<tr>
<td>Operating junction temperature, (T_J)</td>
<td>–40</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

8.4 Thermal Information

<table>
<thead>
<tr>
<th>(\theta)</th>
<th>(\psi)</th>
<th>THERMAL METRIC(^{(1)})</th>
</tr>
</thead>
<tbody>
<tr>
<td>(\theta_{JA})</td>
<td>Junction-to-ambient thermal resistance</td>
<td>80.2</td>
</tr>
<tr>
<td>(\theta_{JCtop})</td>
<td>Junction-to-case (top) thermal resistance</td>
<td>93.5</td>
</tr>
<tr>
<td>(\theta_{JB})</td>
<td>Junction-to-board thermal resistance</td>
<td>54.2</td>
</tr>
<tr>
<td>(\psi_{JT})</td>
<td>Junction-to-top characterization parameter</td>
<td>0.9</td>
</tr>
<tr>
<td>(\psi_{JB})</td>
<td>Junction-to-board characterization parameter</td>
<td>59.3</td>
</tr>
<tr>
<td>(\theta_{JCbot})</td>
<td>Junction-to-case (bottom) thermal resistance</td>
<td>20</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.
8.5 Electrical Characteristics

Over recommended free air temperature range, typical values are at $T_A = 25^\circ$C. Unless otherwise noted, specifications apply for condition $V_{IN} = EN = 3.6$ V, $V_{OUT} = 5.5$ V.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{FB}$</td>
<td>Feedback voltage</td>
<td>1.182</td>
<td>1.2</td>
<td>1.218</td>
<td>V</td>
</tr>
<tr>
<td>Maximum line regulation</td>
<td>$2.3 \leq V_{IN} \leq 6$ V</td>
<td>0.5%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maximum load regulation</td>
<td></td>
<td>0.5%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$f$</td>
<td>Oscillator frequency</td>
<td>3500 kHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{DS(on)}$</td>
<td>High side switch ON resistance</td>
<td>200 mΩ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Low side switch ON resistance</td>
<td>130 mΩ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reverse leakage current into $V_{OUT}$</td>
<td>$EN = GND$</td>
<td>3.5 μA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{IN(DC)}$</td>
<td>Programmable input average switch current limit</td>
<td>ILIM pin set to $V_{IN}$</td>
<td>1500 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ILIM pin set to GND</td>
<td>100 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{ILIM} = 20$ kΩ (500 mA)</td>
<td>$-10%$</td>
<td>10%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_Q$</td>
<td>Quiescent current</td>
<td>PFM enabled, device is not switching</td>
<td>30 μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>SNOOZE mode, $I_{OUT} = 0$ mA, current into $V_{IN}$ pin</td>
<td>2 μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{SD}$</td>
<td>Shutdown current</td>
<td>$V_{IN}$ turned on when $EN$ is connected to GND and no voltage is present at $V_{OUT}$</td>
<td>0.85 μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3.5 μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OVP</td>
<td>Input over voltage protection threshold</td>
<td>Falling</td>
<td>6.4 V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Rising</td>
<td>6.5 V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**CONTROL STAGE**

<table>
<thead>
<tr>
<th>DESCRIPTION</th>
<th>FIGURE</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{UVLO}$</td>
<td>Under voltage lockout threshold</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>EN input low voltage</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>EN input high voltage</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Power Good threshold voltage</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>Power good delay</td>
<td></td>
</tr>
<tr>
<td>Overtemperature protection</td>
<td></td>
</tr>
<tr>
<td>Overtemperature hysteresis</td>
<td></td>
</tr>
</tbody>
</table>

(1) When the power good threshold is triggered the first time a comparator is turned on to observe the output voltage increasing the shutdown current.

8.6 Typical Characteristics

**Table 1. Table Of Graphs**

<table>
<thead>
<tr>
<th>DESCRIPTION</th>
<th>FIGURE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Efficiency</td>
<td>vs Output current ($V_{OUT} = 5.5$ V, $I_{LIM} = 1.5$ A, $R_1 = 2320$ kΩ and $R_2 = 649$ kΩ)</td>
</tr>
<tr>
<td></td>
<td>vs Output current in 100% Duty-Cycle Mode ($V_{OUT} = 5.5$V, $I_{LIM} = 1.5$ A, $R_1 = 2320$ kΩ and $R_2 = 649$ kΩ)</td>
</tr>
<tr>
<td></td>
<td>vs Input voltage ($V_{OUT} = 5.5$ V, $I_{LOAD} = {0.01; 0.1; 1.0; 10; 100; 500$ mA$}$, $R_1 = 2320$ kΩ and $R_2 = 649$ kΩ)</td>
</tr>
<tr>
<td>Maximum output current</td>
<td>vs Input voltage ($V_{OUT} = 5.5$ V, $I_{LIM} = {100; 200; 500; 1000; 1500$ mA$}$, $R_1 = 1000$ kΩ and $R_2 = 280$ kΩ)</td>
</tr>
<tr>
<td>Output voltage</td>
<td>vs Output current ($V_{OUT} = 5.5$ V, $I_{LIM} = 1.5$ A, $R_1 = 1000$ kΩ and $R_2 = 280$ kΩ)</td>
</tr>
</tbody>
</table>
9 Detailed Description

9.1 Overview

The TPS61251 Boost Converter operates as a quasi-constant frequency adaptive on-time controller. In a typical application the frequency will be 3.5 MHz and is defined by the input to output voltage ratio and does not vary from moderate to heavy load currents. At light load the converter will automatically enter Power Save Mode and operates in PFM (Pulse Frequency Modulation) mode. During PWM operation the converter uses a unique fast response quasi-constant on-time valley current mode controller scheme which offers excellent line and load regulation and the use of small ceramic input capacitors.

Based on the $V_{IN}/V_{OUT}$ ratio, a simple circuit predicts the required on-time. At the beginning of the switching cycle, the low-side N-MOS switch is turned on and the inductor current ramps up to a peak current that is defined by the on-time and the inductance. In the second phase, once the on-timer has expired, the rectifier is turned on and the inductor current decays to a preset valley current threshold. Finally, the switching cycle repeats by setting the on timer again and activating the low-side N-MOS switch.

The TPS61251 device directly and accurately controls the average input current through intelligent adjustment of the valley current limit, allowing an accuracy of ±10%. Together with an external bulk capacitor the TPS61251 device allows an application to be interfaced directly to its load, without overloading the input source due to appropriate set average input current limit.

High values of output capacitance are mainly achieved by putting capacitors in parallel. This reduces the overall series resistance (ESR) to very low values. This results in almost no voltage ripple at the output and therefore the regulation circuit has no voltage drop to react on. Nevertheless to ensure accurate output voltage regulation even with very low ESR the regulation loop can switch to a pure comparator regulation scheme. During this operation the output voltage is regulated between two thresholds. The upper threshold is defined by the programmed output voltage and the lower value is about 10 mV lower. If the upper threshold is reached the off-time is increased to reduce the current in the inductor. Therefore the output voltage will slightly drop until the lower threshold is tripped. Now the off-time will be reduced to increase the current in the inductor to charge up the output voltage to the steady-state value. The current swing during this operation mode is strongly depending on the current drawn by the load but will not exceed the programmed current limit. The output voltage during comparator operation stays within the specified accuracy with minimum voltage ripple.

This architecture with adaptive slope compensation provides excellent transient load response and requiring minimal output filtering. Internal softstart and loop compensation simplifies the design process while minimizing the number of external components.
9.2 Functional Block Diagram

9.3 Feature Description

9.3.1 Current Limit Operation

The current limit circuit employs a valley current sensing scheme. Current limit detection occurs during the off-time through sensing of the voltage drop across the synchronous rectifier. The output voltage is reduced as the power stage of the device operates in a constant current mode. The maximum continuous output current \( I_{\text{OUT(CL)}} \), before entering current limit (CL) operation, can be defined by Equation 1 as shown below:

\[
I_{\text{OUT(CL)}} = (1 - D) \cdot I_{\text{IN(DC)}}
\]

(1)

The duty cycle (D) can be estimated by following Equation 2

\[
D = 1 - \frac{V_{\text{IN}} \cdot \eta}{V_{\text{OUT}}}
\]

(2)
Feature Description (continued)

9.3.2 Soft-Start
The TPS61251 device has an internal charging circuit that controls the current during the output capacitor charging and prevents the converter from inrush current that exceeds the set current limit. For typical 100 µs the current is ramped to the set current limit. After reaching the current limit threshold the output capacitor is charged with a constant current until the programmed output voltage is reached. During the phase where $V_{IN} > V_{OUT}$, the rectifying switch is controlled by the current limit circuit and works as a linear regulator in constant current mode. If then $V_{IN} = V_{OUT}$, the converter starts switching and boosting up the voltage to its nominal output voltage by still charging the capacitor with a constant current set by resistor $R_{ILIM}$. During constant current charging power dissipation in the TPS61251 device is increased resulting in a thermal rise or heating of the device. If the output capacitor is very large charging time can be long and thermal rise high. To prevent overheating of the device during the charge phase the current will be limited to a lower value when device temperature is high. Please refer to Thermal Regulation.

9.3.3 Enable
The device is enabled by setting EN pin to a voltage above 1 V. At first, the internal reference is activated and the internal analog circuits are settled. Afterwards, the softstart is activated and the output voltage ramps up. The output voltage reaches its nominal value as fast as the current limit settings and the load condition allows it.

The EN input can be used to control power sequencing in a system with several DC-DC converters. The EN pin can be connected to the output of another converter, to drive the EN pin high and getting a sequencing of supply rails. With EN = GND, the device enters shutdown mode.

9.3.4 Undervoltage Lockout (UVLO)
The UVLO prevents the device from malfunctioning at low input voltages and the battery from excessive discharge. It disables the output stage of the converter once the falling $V_{IN}$ trips the undervoltage lockout threshold $V_{UVLO}$ which is typically 2 V. The device starts operation once the rising $V_{IN}$ trips $V_{UVLO}$ threshold plus its hysteresis of 100 mV at typical 2.1 V.

9.3.5 Power Good
The device has a built-in power good function to indicate whether the output voltage has reached the programmed value and therefore the capacitor is fully charged. The power good output (PG) is set high if the feedback voltage reaches 95% of its nominal value. The power good comparator operates even in shut down mode when EN is set to low and/or $V_{IN}$ is turned off. This guarantees power good functionality until the capacitor is discharged. The PG output goes low when $V_{OUT}$ drops below 2.3 V and indicates the discharge of the capacitor. If the output voltage decreases further and goes below 2 V the converter disables all internal circuitry. Therefore the PG open drain output becomes high resistive and follows the voltage the pullup resistor is connected to.

Because power good functionality is active as long as the output capacitors are charged the converter can be disconnected from its supply but is still supplying the following circuitry with energy. A connected buck converter or buck-boost converter can use this energy to support a follow-on circuit that needs additional energy for a secured shut down.

9.3.6 Input Over Voltage Protection
This converter has a input over voltage protection that protects the device from damage due to a voltage higher than the absolute maximum rating of the input allows. If 6.5 V (typical) at the input is exceeded, the converter completely shuts down to protect its inner circuitry as well as the circuit connected to $V_{OUT}$. If the input voltage drops below 6.4 V (typical), the device turns on again and enters normal start-up again.

9.3.7 Load Disconnect and Reverse Current Protection
The TPS61251 device has an intelligent load disconnect circuit that prevents current flow in any direction during shutdown. In case of a connected battery and $V_{IN} > V_{OUT}$ the converter will not discharge the battery during shutdown of the converter. In the opposite case when a bulk capacitor is connected to VOUT and charged to a higher voltage than $V_{IN}$ the converter prevents the capacitor from being discharged through the input load (battery).
Feature Description (continued)

9.3.8 Thermal Regulation

The TPS61251 device contains a thermal regulation loop that monitors the die temperature. If the die temperature rises to values above 110°C, the device automatically reduces the current to prevent the die temperature from further increasing. Once the die temperature drops about 10°C below the threshold, the device will automatically increase the current to the target value. This function also reduces the current during a short-circuit-condition.

9.3.9 Thermal Shutdown

As soon as the junction temperature, $T_J$, exceeds 140°C (typical) the device enters thermal shutdown. In this mode, the High Side and Low Side MOSFETs are turned off. When the junction temperature falls about 20°C below the thermal shutdown, the device continues the operation.

9.4 Device Functional Modes

9.4.1 Power-Save Mode

The TPS61251 device integrates a power save mode to improve efficiency at light load. In power save mode the converter only operates when the output voltage trips below a set threshold voltage. It ramps up the output voltage with several pulses and goes into power save mode once the output voltage exceeds the set threshold voltage. During the power save operation when the output voltage is above the set threshold the converter turns off some of the inner circuits to save energy.

The PFM mode is left and PWM mode entered in case the output current can not longer be supported in PFM mode.

9.4.2 Snooze Mode

During this enhanced power save mode, the converter still maintains the output voltage with a tolerance of ±2%. The operating current in snooze mode is, however, drastically reduced to a typical value of 2 μA. This will be achieved by turning off as much as possible of the inner regulation circuits. Load current in snooze mode is limited to 2 mA. If the load current increases above 2 mA, the controller recognizes a further drop of the output voltage and the device turns on again to charge the output capacitor to the programmed output voltage again.

9.4.3 100% Duty-Cycle Mode

If $V_{IN} > V_{OUT}$ the TPS61251 device offers the lowest possible input-to-output voltage difference while still maintaining current limit operation with the use of the 100% duty-cycle mode. In this mode, the PMOS switch is constantly turned on. During this operation the output voltage follows the input voltage and will not fall below the programmed value if the input voltage decreases below $V_{OUT}$. The output voltage drop during 100% mode depends on the load current and input voltage, and the resulting output voltage is calculated using Equation 3.

$$V_{OUT} = V_{IN} - (DCR + r_{DS(on)}) \cdot I_{OUT}$$

where
- DCR is the DC resistance of the inductor
- $r_{DS(on)}$ is the typical on-resistance of the PMOS switch

$$V_{OUT} = V_{IN} - (DCR + r_{DS(on)}) \cdot I_{OUT} \tag{3}$$
10 Application and Implementation

**NOTE**
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information
The TPS61251 device provides a power supply solution for products powered by either a three-cell, NiCd or NiMH battery, or a one-cell Li-Ion or Li-polymer battery. The wide input voltage range is ideal to power portable applications like mobile phones, solid state drives (SSD) and wireless modems. The converter is designed to charge large capacitors in the Farad range to support battery back up applications.

10.2 Typical Application
Figure 6 shows a typical application for 5.5 V output voltage with input current limit.

![Typical Application Schematic](image)

**Figure 6. Typical Application Schematic**

10.2.1 Design Requirements
Table 2 lists the design requirements.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage</td>
<td>$V_{IN}$</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>Minimum Input Voltage</td>
<td>$V_{IN(min)}$</td>
<td>2.9</td>
<td>V</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>$V_{OUT}$</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Input Current Limit set by $R_{ILIM}$</td>
<td>$I_{ILIM}$</td>
<td>500</td>
<td>mA</td>
</tr>
<tr>
<td>Feedback Voltage</td>
<td>$V_{FB}$</td>
<td>1.2</td>
<td>V</td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>$f$</td>
<td>3.5</td>
<td>MHz</td>
</tr>
<tr>
<td>Estimated Efficiency</td>
<td>$\eta$</td>
<td>90%</td>
<td></td>
</tr>
<tr>
<td>Inductor Value of Choice</td>
<td>$L_1$</td>
<td>1</td>
<td>(\mu F)</td>
</tr>
</tbody>
</table>

Table 2. Design Parameters
## 10.2.2 Detailed Design Procedure

### 10.2.2.1 Output Voltage Setting

The output voltage can be calculated using Equation 4.

\[
V_{\text{OUT}} = V_{\text{FB}} \cdot \left(1 + \frac{R_1}{R_2}\right)
\]

(4)

To minimize the current through the feedback divider network and therefore increase efficiency during snooze mode operation, \(R_2\) should be >240 kΩ. To keep the network robust against noise the resistor divider can also be in the lower 100-k values. In this case, \(R_1\) is 1000 kΩ and \(R_2\) is 280 kΩ.

An external feed forward capacitor \(C_1\) is required for optimum load transient response. The value of \(C_1\) should be 1000 pF. The connection from FB pin to the resistor divider should be kept short and away from noise sources, such as the inductor or the SW line.

### 10.2.2.2 Average Input Current Limit

The average input current is set by selecting the correct external resistor value correlating to the required current limit. Equation 5 is a guideline for selecting the correct resistor value.

\[
R_{\text{ILIM}} = \frac{1.0V}{I_{\text{ILIM}}} \cdot 10,000
\]

(5)

For a current limit of 500 mA the resistor value will be 20 kΩ.

To allow maximum current limit (1500 mA) the ILIM pin can be directly connected to \(V_{\text{IN}}\). If ILIM is connected to GND the minimum current (100 mA) limit is set.

### 10.2.2.3 Maximum Output Current

The maximum output current is set by \(R_{\text{ILIM}}\) and the input to output voltage ratio and can be calculated using Equation 6.

\[
I_{\text{OUT(max)}} = I_{\text{ILIM}} \cdot \frac{V_{\text{IN}} \cdot \eta}{V_{\text{OUT}}}
\]

(6)

Following the example, \(I_{\text{OUT(max)}}\) will be 295 mA at 3.6 V input voltage and will decrease with lower input voltage values due to the energy conservation.

### 10.2.2.4 Inductor Selection

As for all switch mode power supplies two main passive components are required for storing the energy during operation. This is done by an inductor and an output capacitor. The inductor must be connected between \(V_{\text{IN}}\) and SW pin to make sure that the TPS61251 device operates. To select the right inductor current rating the programmed input current limit as well as the current ripple through the inductor is necessary. Estimation of the maximum peak inductor current can be done using Equation 7.

\[
I_{\text{L(max)}} = I_{\text{ILIM}} + \Delta I_L = I_{\text{ILIM}} + \frac{V_{\text{IN(min)}} \cdot D}{L \cdot f} \quad \text{with} \quad D = 1 - \frac{V_{\text{IN(min)}} \cdot \eta}{V_{\text{OUT}}}
\]

(7)

Regarding the example from above the current ripple (\(\Delta I_L\)) will be 290 mA and therefore an inductor with a rated current of about 800 mA should be used.

The TPS61251 device is designed to work with inductor values between 1 µH and 2.2 µH. TI recommends a 1.5 µH inductor for typical applications. In space constrained applications, it might be possible to consider smaller inductor values depending on the targeted inductor ripple current. Therefore, the inductor value can be reduced down to 1 µH without degrading the stability.

In regular boost converter designs the current through the inductor is defined by the switch current limit of the converters switches and therefore bigger inductors have to be chosen. The TPS61251 device allows the design engineer to reduce the current limit to the needs of the application regardless the maximum switch current limit of the converter. Programming a lower current value allows the use of smaller inductors without the danger to get into saturation.
10.2.2.5 Output Capacitor

The second energy storing device is the output capacitor. When selecting output capacitors for large pulsed loads, the magnitude and duration of the pulsing current, together with the ripple voltage specification, determine the choice of the output capacitor. Both the ESR of the capacitor and the charge stored in the capacitor each cycle contribute to the output voltage ripple. The ripple due to the charge is approximately what results from Equation 8.

\[ V_{\text{RIPPLE(mV)}} = \frac{I_{\text{PULSE}} - I_{\text{STANDBY}} \cdot t_{\text{on}}}{C_{\text{OUT}}} \]

where
- \( I_{\text{PULSE}} \) and \( t_{\text{on}} \) are the peak current and on time during transmission burst.
- \( I_{\text{STANDBY}} \) is the current in standby mode.

(8)

The above is a worst-case approximation assuming all the pulsing energy comes from the output capacitor.

The ripple due to the capacitor ESR is defined by Equation 9.

\[ \Delta V_{\text{ESR}} = \left( I_{\text{PULSE}} - I_{\text{STANDBY}} \right) \cdot \text{ESR} \]

(9)

High capacitance values and low ESR can lead to instability in some internally compensated boost converters. The internal loop compensation of the TPS61251 device is optimized to be stable with output capacitor values greater than 150 \( \mu \)F with very low ESR.

Because big bulk capacitors cannot be placed very close to the IC, it is required to put a small ceramic capacitor of about 4.7 \( \mu \)F as close as possible to the output terminals. This will reduce parasitic effects that can influence the functionality of the converter.

Table 3. List Of Bulk Capacitors

<table>
<thead>
<tr>
<th>VENDOR (alphabetical order)</th>
<th>CAPACITANCE</th>
<th>PART NUMBER</th>
</tr>
</thead>
<tbody>
<tr>
<td>Kemet</td>
<td>470 ( \mu )F, 6.3 V, 55 m( \Omega )</td>
<td>T520W477M006ATE055</td>
</tr>
<tr>
<td>Sanyo</td>
<td>470 ( \mu )F, 6.3 V, 35 m( \Omega )</td>
<td>6TPE470MAZU</td>
</tr>
</tbody>
</table>

10.2.2.6 Input Capacitor

Multilayer ceramic capacitors are an excellent choice for input decoupling of the step-up converter as they have extremely low ESR and are available in small form factors. Input capacitors should be located as close as possible to the device. While a 10-\( \mu \)F input capacitor is sufficient for most applications, larger values may be used to reduce input current ripple on the supply rail without limitations. Although low ESR tantalum capacitors may be used.

\[ \text{DC Bias effect:} \] High capacitance ceramic capacitors have a DC Bias effect, which has a strong influence on the final effective capacitance. Therefore, the right capacitor value has to be chosen very carefully. Package size and voltage rating in combination with material are responsible for differences between the rated capacitor value and the effective capacitance. A 10-V rated 0805 capacitor with 10 \( \mu \)F can have an effective capacitance of less 5 \( \mu \)F at an output voltage of 5 V.

10.2.2.7 Checking Loop Stability

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:
- Switching node, SW
- Inductor current, \( I_L \)
- Output ripple voltage, \( V_{\text{OUT(AC)}} \)

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.
As a next step in the evaluation of the regulation loop, the load transient response is tested. The time between the load transient takes place and the turn on of the PMOS switch, the output capacitor must supply all of the current required by the load. \( V_{\text{OUT}} \) immediately shifts by an amount equal to \( \Delta I_{\text{LOAD}} \times ESR \), where ESR is the effective series resistance of \( C_{\text{OUT}} \). \( \Delta I_{\text{LOAD}} \) begins to charge or discharge \( C_{\text{OUT}} \) generating a feedback error signal used by the regulator to return \( V_{\text{OUT}} \) to its steady-state value. The results are most easily interpreted when the device operates in PWM mode.

During this recovery time, \( V_{\text{OUT}} \) can be monitored for settling time, overshoot or ringing that helps judge the converter’s stability. Without any ringing, the loop has usually more than 45°C of phase margin. Because the damping factor of the circuitry is directly related to several resistive parameters (for example, MOSFET \( r_{\text{DS(on)}} \) that are temperature dependent, the loop stability analysis has to be done over the input voltage range, load current range, and temperature range.

### 10.2.3 Application Curves

<table>
<thead>
<tr>
<th>Table 4. Table Of Graphs</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DESCRIPTION</strong></td>
</tr>
<tr>
<td>Waveforms</td>
</tr>
<tr>
<td>Load transient response (Tantal Capacitor 2.3 mF with &gt;60 mΩ ESR, ( V_{\text{OUT}} = 5.5 ) V, ( V_{\text{IN}} = 3.6 ) V, ( I_{\text{LIM}} = 1000 ) mA, Load change from 50 mA to 550 mA)</td>
</tr>
<tr>
<td>Load transient response (6 × 330-µF Polymer Tantal &lt;5 mΩ ESR in total, ( V_{\text{OUT}} = 5.5 ) V, ( V_{\text{IN}} = 3.6 ) V, ( I_{\text{LIM}} = 1000 ) mA, Load change from 500 mA to 1500 mA)</td>
</tr>
<tr>
<td>Start-up after enable (( V_{\text{OUT}} = 5.5 ) V, ( V_{\text{IN}} = 3.6 ) V, ( I_{\text{LIM}} = 1000 ) mA)</td>
</tr>
<tr>
<td>Start-up after enable (( V_{\text{OUT}} = 5.5 ) V, ( V_{\text{IN}} = 3.6 ) V, ( I_{\text{LIM}} = 500 ) mA)</td>
</tr>
</tbody>
</table>

**Figure 7. Load Transient Response (Tantal Capacitor)**

**Figure 8. Load Transient Response (Low ESR Polymer Tantal)**
Table 5 lists the components used for the waveform measurements.

<table>
<thead>
<tr>
<th>REFERENCE</th>
<th>DESCRIPTION</th>
<th>MANUFACTURER</th>
</tr>
</thead>
<tbody>
<tr>
<td>U1</td>
<td>TPS61251</td>
<td>Texas Instruments</td>
</tr>
<tr>
<td>L1</td>
<td>1 μH, 2.1 A, 27 mΩ, 2.8 mm × 2.8 mm × 1.5 mm</td>
<td>DEM2815C, TOKO</td>
</tr>
<tr>
<td>C1</td>
<td>1 × 4.7 μF, 10 V, 0805, X7R ceramic</td>
<td>GRM21BR71A475KA73, Murata</td>
</tr>
<tr>
<td>C2</td>
<td>1 × 1000 pF, 50 V, 0603, COG ceramic</td>
<td>GRM1885C1H102JA01B, Murata</td>
</tr>
<tr>
<td>C3</td>
<td>1 × 4.7 μF, 10 V, 0805, X7R ceramic</td>
<td>GRM21BR71A475KA73, Murata</td>
</tr>
<tr>
<td>C4</td>
<td>20 × 100 μF, 6.3 V, 1206, X5R</td>
<td>GRM31CR60J107ME39B, Murata</td>
</tr>
<tr>
<td>R1</td>
<td>Depending on the output voltage of TPS61251, 1%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(all waveform measurements with 5.5 V output voltage uses 1000 kΩ)</td>
<td></td>
</tr>
<tr>
<td>R2</td>
<td>Depending on the output voltage of TPS61251, 1%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(all waveform measurements with 5 V output voltage uses 280 kΩ)</td>
<td></td>
</tr>
<tr>
<td>R3</td>
<td>Depending on the input current limit of TPS61251, 1%</td>
<td></td>
</tr>
<tr>
<td>R4</td>
<td>1 MΩ, 1%</td>
<td>any</td>
</tr>
</tbody>
</table>
11 Power Supply Recommendations

The power supply can be a three-cell alkaline, NiCd or NiMH battery, or a one-cell Li-Ion or Li-polymer battery. The input supply should be well regulated with the rating of the TPS61251 device. If the input supply is located more than a few inches from the device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.

12 Layout

12.1 Layout Guidelines

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

The feedback divider should be placed close to the IC to keep the feedback connection short. To lay out the ground, short traces and wide are recommended. This avoids ground shift problems, which can occur due to superimposition of power ground current and the feedback divider.

12.2 Layout Example

![Figure 11. Suggested Layout Without Bulk Capacitors (Top)](image-url)
12.3 Thermal Consideration

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependant issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
  - For example, increase of the GND plane on the top layer which is connected to the exposed thermal pad
  - Use thicker copper layer
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design. The maximum junction temperature ($T_J$) of the TPS61251 device is 150°C.
13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

TI’S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT
CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES
OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER
ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

13.2 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective
contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of
Use.

TI E2E™ Online Community  Ti's Engineer-to-Engineer (E2E) Community. Created to foster collaboration
among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help
solve problems with fellow engineers.

Design Support  Ti's Design Support  Quickly find helpful E2E forums along with design support tools and
contact information for technical support.

13.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam
during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — Ti Glossary.
This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most
current data available for the designated devices. This data is subject to change without notice and revision of
this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
### PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS61251DSGR</td>
<td>ACTIVE</td>
<td>WSON</td>
<td>DSG</td>
<td>8</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>QTH</td>
<td></td>
</tr>
<tr>
<td>TPS61251DSGT</td>
<td>ACTIVE</td>
<td>WSON</td>
<td>DSG</td>
<td>8</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>QTH</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.
- **Pb-Free (RoHS)**: TI's terms “Lead-Free” or “Pb-Free” mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
- **Pb-Free (RoHS Exempt)**: This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
- **Green (RoHS & no Sb/Br)**: TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
### TAPE AND REEL INFORMATION

#### REEL DIMENSIONS

![Reel Dimensions Diagram](image)

#### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

![Quadrant Assignments Diagram](image)

*All dimensions are nominal.*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS61251DSGR</td>
<td>WSON</td>
<td>DSG</td>
<td>8</td>
<td>3000</td>
<td>179.0</td>
<td>8.4</td>
<td>2.2</td>
<td>2.2</td>
<td>1.2</td>
<td>4.0</td>
<td>8.0</td>
<td>Q2</td>
</tr>
<tr>
<td>TPS61251DSGR</td>
<td>WSON</td>
<td>DSG</td>
<td>8</td>
<td>3000</td>
<td>178.0</td>
<td>8.4</td>
<td>2.25</td>
<td>2.25</td>
<td>1.0</td>
<td>4.0</td>
<td>8.0</td>
<td>Q2</td>
</tr>
<tr>
<td>TPS61251DSGT</td>
<td>WSON</td>
<td>DSG</td>
<td>8</td>
<td>250</td>
<td>179.0</td>
<td>8.4</td>
<td>2.2</td>
<td>2.2</td>
<td>1.2</td>
<td>4.0</td>
<td>8.0</td>
<td>Q2</td>
</tr>
<tr>
<td>TPS61251DSGT</td>
<td>WSON</td>
<td>DSG</td>
<td>8</td>
<td>250</td>
<td>178.0</td>
<td>8.4</td>
<td>2.25</td>
<td>2.25</td>
<td>1.0</td>
<td>4.0</td>
<td>8.0</td>
<td>Q2</td>
</tr>
</tbody>
</table>
**TAPE AND REEL BOX DIMENSIONS**

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS61251DSGR</td>
<td>WSON</td>
<td>DSG</td>
<td>8</td>
<td>3000</td>
<td>195.0</td>
<td>200.0</td>
<td>45.0</td>
</tr>
<tr>
<td>TPS61251DSGR</td>
<td>WSON</td>
<td>DSG</td>
<td>8</td>
<td>3000</td>
<td>205.0</td>
<td>200.0</td>
<td>33.0</td>
</tr>
<tr>
<td>TPS61251DSGT</td>
<td>WSON</td>
<td>DSG</td>
<td>8</td>
<td>250</td>
<td>195.0</td>
<td>200.0</td>
<td>45.0</td>
</tr>
<tr>
<td>TPS61251DSGT</td>
<td>WSON</td>
<td>DSG</td>
<td>8</td>
<td>250</td>
<td>205.0</td>
<td>200.0</td>
<td>33.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, “Designers”) understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers’ applications and compliance of their applications (and of all TI products used in or for Designers’ applications) with all applicable regulations, laws and other applicable requirements. Designers represent that, with respect to their applications, Designers have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designers agree that prior to using or distributing any applications that include TI products, Designers will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI’s provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, “TI Resources”) are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer’s company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI’s provision of TI Resources does not expand or otherwise alter TI’s applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY TECHNOLOGY, PATENT OR INTELLECTUAL PROPERTY RIGHTS OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED “AS IS” AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designers may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers’ own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer’s non-compliance with the terms and provisions of this Notice.