TPS61165-Q1 High-Brightness White LED Driver in SOT-23 Package

1 Features

- Qualified for Automotive Applications
- 40-V Maximum Breakdown Voltage of Internal MOSFET
- 38-V Open LED Protection
- 200-mV Reference Voltage With 2% Accuracy
- 1.2-A Switch FET With 1.2-MHz Switching Frequency
- Flexible 1-Wire Digital and PWM Brightness Control
- Built-in Soft Start
- Up to 90% Efficiency
- SOT-23 Package

2 Applications

- High-Brightness LED Lighting
- White LED Backlighting for Media Form Factor Display
- Automotive Cluster Backlighting

3 Description

With a 40-V rated integrated switch FET, the TPS61165-Q1 device is a boost converter that drives LEDs in series. The boost converter runs at a 1.2-MHz fixed switching frequency with 1.2-A switch current limit, and allows for the use of a high brightness LED in general lighting.

The default white LED current is set with the external sensor resistor Rset, and the feedback voltage is regulated to 200 mV, as shown in the *Typical Application* section. During the operation, the LED current can be controlled using the 1-wire digital interface (EasyScale™ protocol) through the CTRL pin. Alternatively, a pulse width modulation (PWM) signal can be applied to the CTRL pin through which the duty cycle determines the feedback reference voltage. In either digital or PWM mode, the TPS61165-Q1 device does not burst the LED current; therefore, the device does not generate audible noises on the output capacitor. For maximum protection, the TPS61165-Q1 device features integrated open LED protection that disables it to prevent the output from exceeding its absolute maximum voltage ratings during open LED conditions.

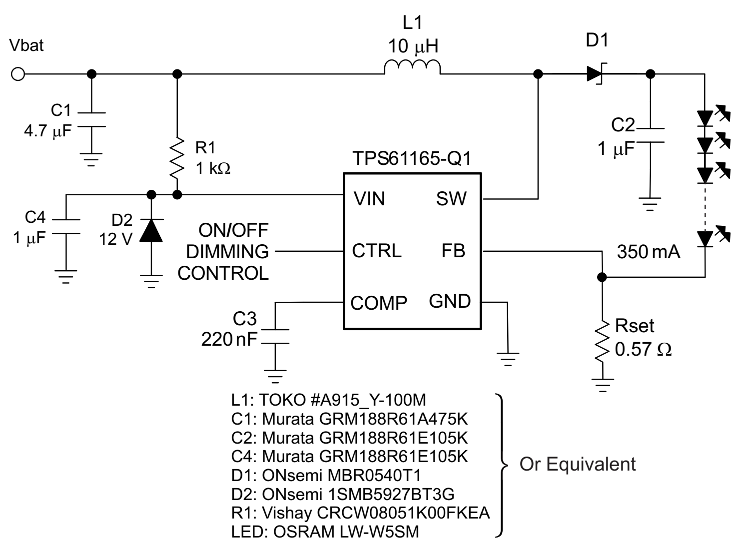
The TPS61165-Q1 device is available in a SOT-23 package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61165-Q1	SOT-23 (6)	1.60 mm × 2.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



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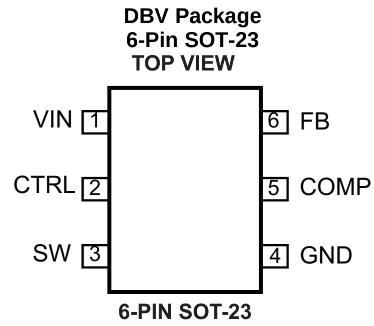
4 Revision History

Changes from Revision A (September 2013) to Revision B	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
COMP	5	O	Output of the transconductance error amplifier. Connect an external capacitor to this pin to compensate the converter.
CTRL	2	I	Control pin of the boost converter. It is a multi-functional pin which can be used for enable control, PWM, and digital dimming.
FB	6	I	Feedback pin for current. Connect the sense resistor from FB to GND.
GND	4	O	Ground
SW	3	I	This is the switching node of the IC. Connect the switched side of the inductor to SW. This pin is also used to sense the output voltage for open LED protection.
VIN	1	I	The input supply pin for the IC. Connect VIN to a supply voltage between 3 V and 18 V.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_I	Supply Voltages on VIN (2)	–0.3	20	V
	Voltages on CTRL (2)	–0.3	20	
	Voltage on FB and COMP (2)	–0.3	3	
	Voltage on SW (2)	–0.3	40	
P_D	Continuous Power Dissipation	See *Thermal Information*		
T_J	Operating Junction Temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)		±1000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 3, 6, and 4)	±1000	
			Other pins	±1000	
		Machine model		±100	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_I	Input voltage range, VIN	3		18	V
V_O	Output voltage range	VIN		38	V
L	Inductor[(1)]	10		22	µH
f_{dim}	PWM dimming frequency	5		100	kHz
C_{IN}	Input capacitor	1			µF
C_O	Output capacitor	1		10	µF
T_A	Operating ambient temperature	–40		105	°C
T_J	Operating junction temperature	–40		125	°C

(1) These values are recommended values that have been successfully tested in several applications. Other values may be acceptable in other applications but should be fully tested by the user.

6.4 Thermal Information

THERMAL METRIC[(1)]		TPS61165-Q1 DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	210.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

VIN = 3.6 V, CTRL = VIN, T_A = –40°C to 105°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_I	Input voltage range, VIN		3		18	V
I_Q	Operating quiescent current into VIN	Device PWM switching no load			2.3	mA
I_{SD}	Shutdown current	CRTL=GND, VIN = 4.2 V			2	µA
UVLO	Undervoltage lockout threshold	VIN falling		2.2	2.5	V
V_{hys}	Undervoltage lockout hysterisis			70		mV
ENABLE AND REFERENCE CONTROL						
$V_{(CTRLh)}$	CTRL logic high voltage	VIN = 3 V to 18 V	1.2			V
$V_{(CTRLl)}$	CTRL logic low voltage	VIN = 3 V to 18 V			0.4	V
$R_{(CTRL)}$	CTRL pulldown resistor		400	800	1600	kΩ
t_{off}	CTRL pulse width to shutdown	CTRL high to low	2.5			ms
t_{es_det}	EasyScale detection time[(1)]	CTRL pin low	260			µs
t_{es_delay}	EasyScale detection delay		100			µs
t_{es_win}	EasyScale detection window time	Measured from CTRL high	1			ms
VOLTAGE AND CURRENT CONTROL						
V_{REF}	Voltage feedback regulation voltage		196	200	204	mV
$V_{(REF\_PWM)}$	Voltage feedback regulation voltage under brightness control	V_{FB} = 50 mV	47	50	53	mV
		V_{FB} = 20 mV	17	20	23	mV
I_{FB}	Voltage feedback input bias current	V_{FB} = 200 mV			2	µA
f_S	Oscillator frequency		1	1.2	1.5	MHz
D_{max}	Maximum duty cycle	V_{FB} = 100 mV	90%	93%		

(1) To select EasyScale mode, the CTRL pin must be low for more than t_{es_det} during t_{es_win}.

Electrical Characteristics (continued)

VIN = 3.6 V, CTRL = VIN, T_A = –40°C to 105°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{min_on}	Minimum on pulse width			40		ns
I_{sink}	Comp pin sink current			100		μA
I_{source}	Comp pin source current			100		μA
G_{ea}	Error amplifier transconductance		240	320	400	umho
R_{ea}	Error amplifier output resistance			6		MΩ
f_{ea}	Error amplifier crossover frequency	5 pF connected to COMP		500		kHz
POWER SWITCH						
$R_{DS(ON)}$	N-channel MOSFET on-resistance	VIN = 3.6 V		0.3	0.6	Ω
		VIN = 3 V			0.7	
I_{LN_NFET}	N-channel leakage current	V_{SW} = 35 V, T_A = 25°C			1	μA
OC and OLP						
I_{LIM}	N-Channel MOSFET current limit	D = D_{max}	0.96	1.2	1.44	A
I_{LIM_Start}	Start-up current limit	D = D_{max}		0.7		A
t_{Half_LIM}	Time step for half current limit			5		ms
V_{ovp}	Open LED protection threshold	Measured on the SW pin	37	38	39	V
$V_{(FB\_OVP)}$	Open LED protection threshold on FB	Measured on the FB pin, percentage of Vref, Vref = 200 mV and 20 mV		50%		
t_{REF}	V_{REF} filter time constant			180		μs
t_{step}	V_{REF} ramp up time	Each step measured as number of cycles of the 1.2-MHz clock		213		μs
THERMAL SHUTDOWN						
$T_{shutdown}$	Thermal shutdown threshold			160		°C
$T_{hysteresis}$	Thermal shutdown threshold hysteresis			15		°C

6.6 Timing Requirements

			MIN	NOM	MAX	UNIT
EasyScale TIMING						
t_{start}	Start time of program stream		2			μs
t_{EOS}	End time of program stream		2		360	μs
t_{H_LB}	High time low bit	Logic 0	2		180	μs
t_{L_LB}	Low time low bit	Logic 0	2 × t_{H_LB}		360	μs
t_{H_HB}	High time high bit	Logic 1	2 × t_{L_HB}		360	μs
t_{L_HB}	Low time high bit	Logic 1	2		180	μs
V_{ACKNL}	Acknowledge output voltage low	Open drain, Rpullup =15 kΩ to VIN			0.4	V
$t_{valACKN}$	Acknowledge valid time	See [1]			2	μs
t_{ACKN}	Duration of acknowledge condition	See [1]			512	μs

(1) Acknowledge condition active 0, this condition will only be applied in case the RFA bit is set. Open-drain output, line must be pulled high by the host with resistor load.

6.7 Typical Characteristics

Table 1. Table of Graphs

		FIGURE
Efficiency	3 LEDs (VOUT = 12 V); VIN = 3, 5, 8.5 V; L = 10 μH	Figure 1
Efficiency	6 LEDs (VOUT = 24 V); VIN = 5, 8.5, 12V; L = 10 μH	Figure 2
Current limit	T_A = 25°C	Figure 3
Current limit		Figure 4
EasyScale step		Figure 5
PWM dimming linearity	VIN = 3.6 V; PWM Freq = 10 kHz and 32 kHz	Figure 6
Output ripple at PWM dimming	3 LEDs; VIN = 5 V; I_{LOAD} = 350 mA; PWM = 32 kHz	Figure 7
Switching waveform	3 LEDs; VIN = 5 V; I_{LOAD} = 3500 mA; L = 10 μH	Figure 8
Start-up	3 LEDs; VIN = 5 V; I_{LOAD} = 350 mA; L = 10 μH	Figure 9
Open LED protection	8 LEDs; VIN = 3.6 V; I_{LOAD} = 20 mA	Figure 10

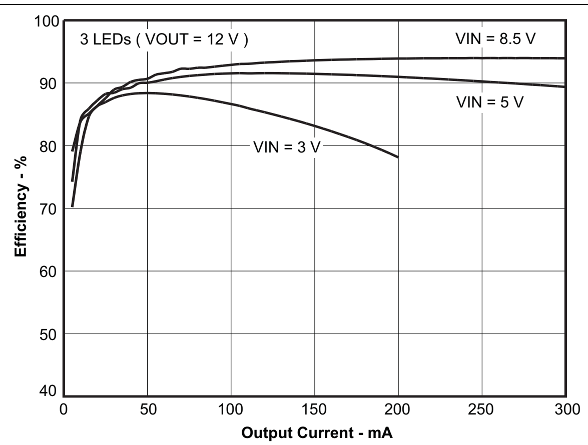


Figure 1. Efficiency vs Output Current

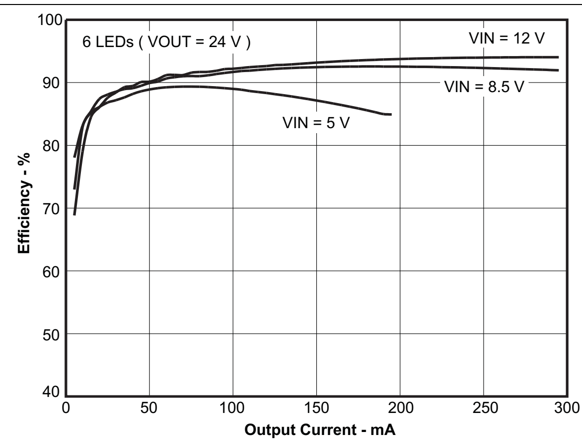


Figure 2. Efficiency vs Output Current

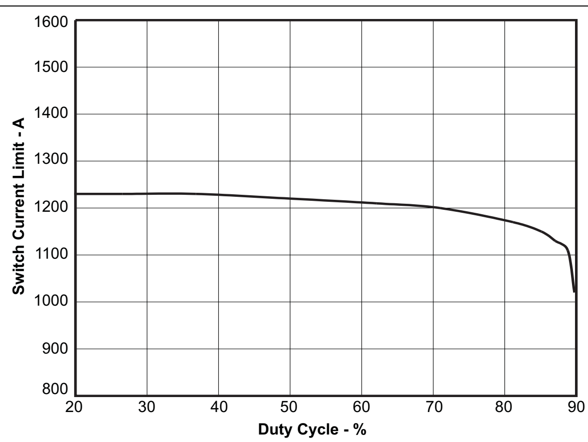


Figure 3. Switch Current Limit vs Duty Cycle

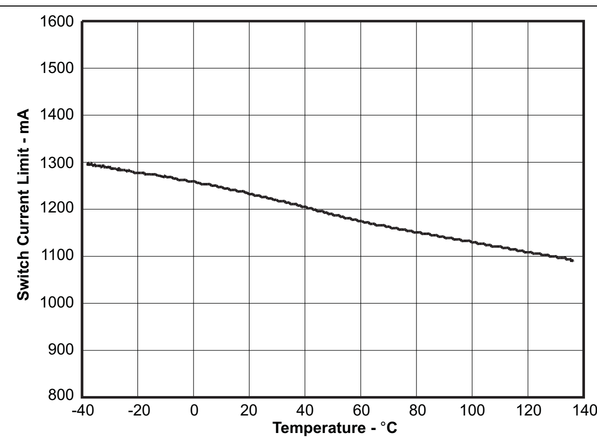


Figure 4. Switch Current Limit vs Temperature

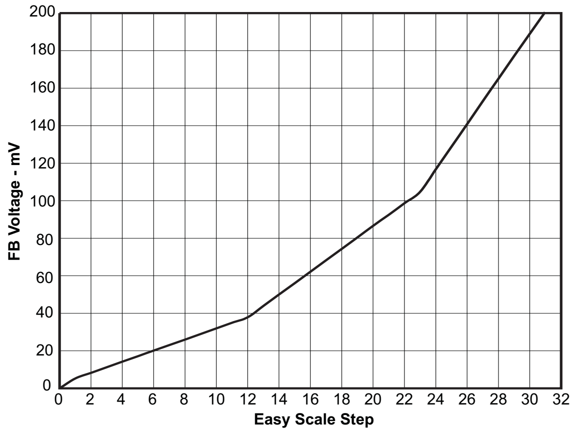


Figure 5. FB Voltage vs EasyScale Step

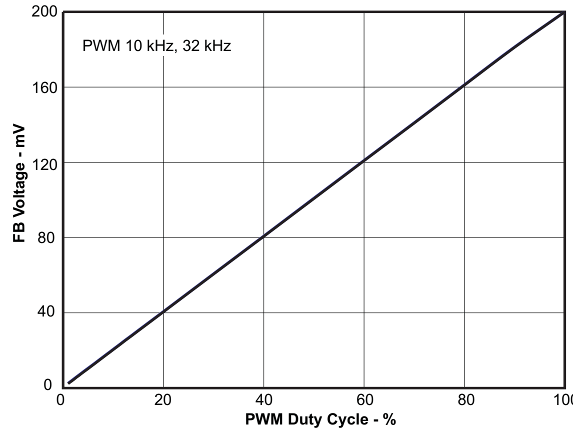


Figure 6. FB Voltage vs PWM Duty Cycle

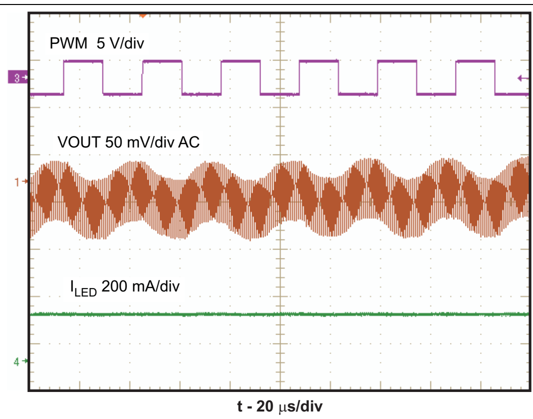


Figure 7. Output Ripple at PWM Dimming

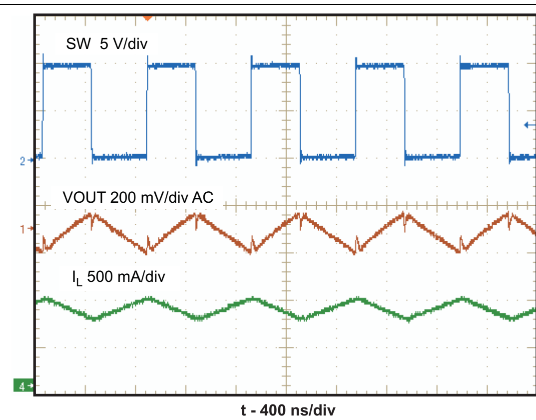


Figure 8. Switching Waveform

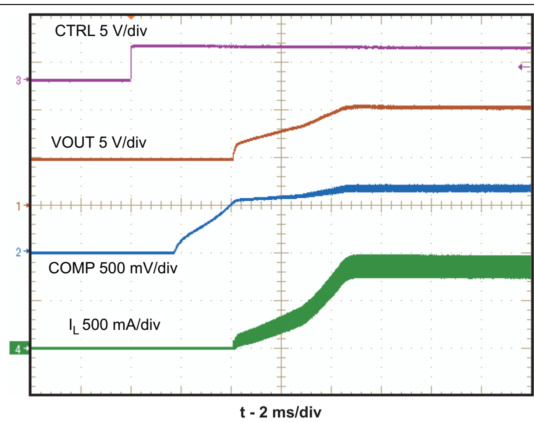


Figure 9. Start-Up

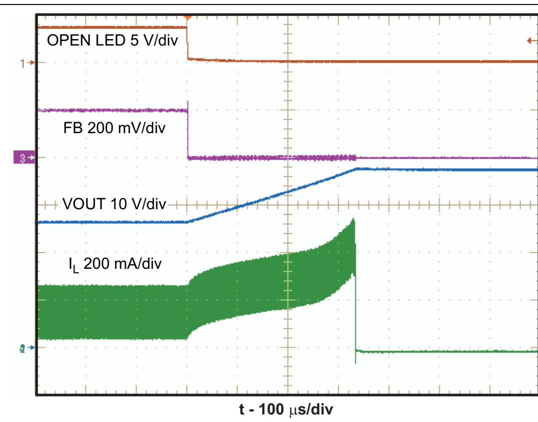


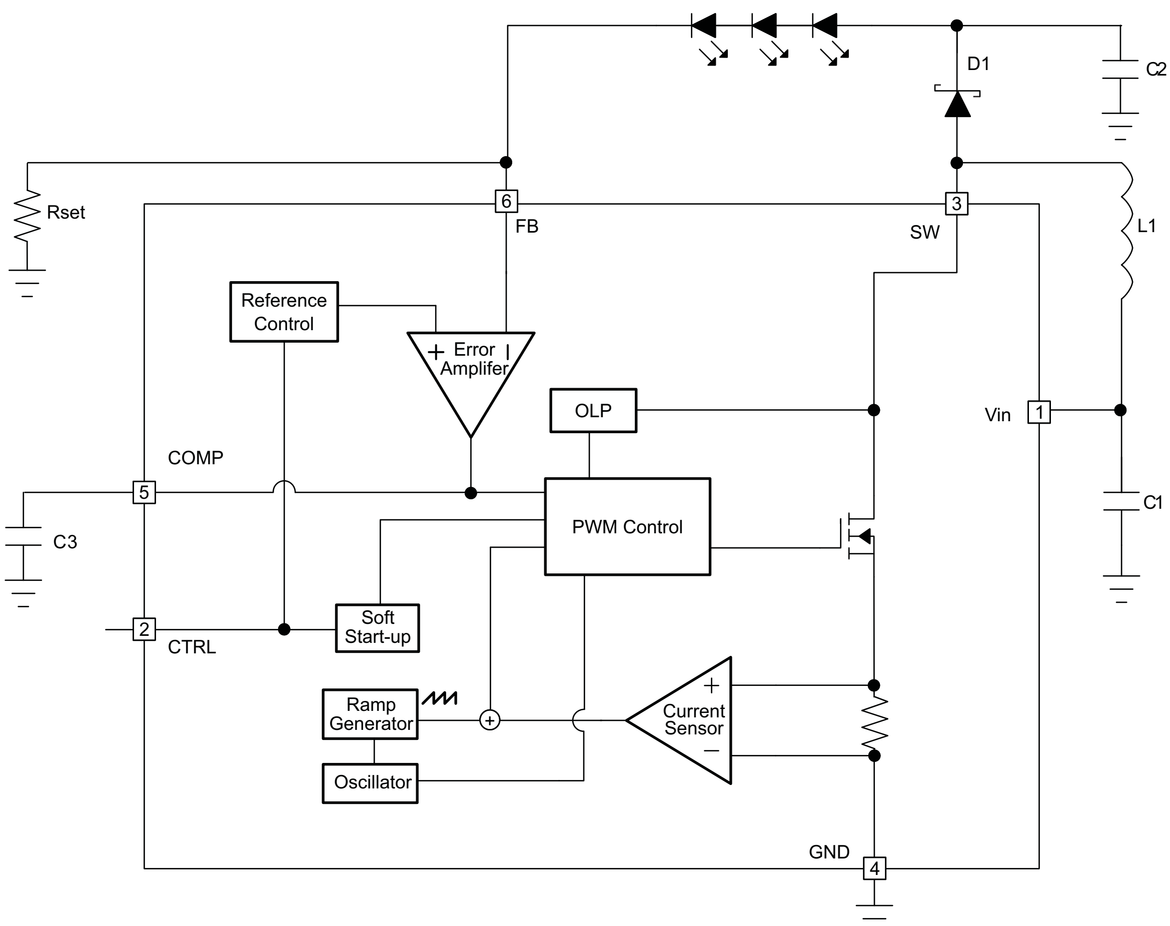
Figure 10. Open LED Protection

7 Detailed Description

7.1 Overview

The TPS61165-Q1 device is a high-efficiency, high-output voltage boost converter in small package size. The device is ideal for driving white LEDs in series. The serial LED connection provides even illumination by sourcing the same output current through all LEDs, eliminating the need for expensive factory calibration. The device integrates 40-V and 1.2-A switch FET and operates in pulse width modulation (PWM) with 1.2-MHz fixed switching frequency. For operation see *Functional Block Diagram*. The duty cycle of the converter is set by the error amplifier output and the current signal applied to the PWM control comparator. The control architecture is based on traditional current-mode control; therefore, slope compensation is added to the current signal to allow stable operation for duty cycles larger than 40%. The feedback loop regulates the FB pin to a low reference voltage (200 mV typical), reducing the power dissipation in the current sense resistor.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Soft Start-Up

Soft-start circuitry is integrated into the IC to avoid a high inrush current during start-up. After the device is enabled, the voltage at FB pin ramps up to the reference voltage in 32 steps; each step takes 213 µs. This ensures that the output voltage rises slowly to reduce the input current. Additionally, for the first 5 ms after the COMP voltage ramps, the current limit of the switch is set to half of the normal current limit specification. During this period, the input current is kept below 700 mA (typical). These two features ensure smooth start-up and minimize the inrush current. See the start-up waveform of a typical example (Figure 9).

Feature Description (continued)

7.3.2 Open LED Protection

Open LED protection circuitry prevents IC damage as the result of white LED disconnection. The TPS61165-Q1 device monitors the voltage at the SW pin and FB pin during each switching cycle. The circuitry turns off the switch FET and shuts down the IC when both of the following conditions persist for 8 switching clock cycles: (1) the SW voltage exceeds the V_{OVP} threshold and (2) the FB voltage is less than half of regulation voltage. As a result, the output voltage falls to the level of the input supply. The device remains in shutdown mode until it is enabled by toggling the CTRL pin. The product of the number of external series LEDs and each LED's maximum forward voltage plus the 200-mV reference voltage does not exceed the 38-V minimum OVP threshold or (N_{LEDS} X $V_{LED(MAX)}$ + 200 mV ≤ 38 V.

7.3.3 Undervoltage Lockout

An undervoltage lockout prevents operation of the device at input voltages below 2.2 V (typical). When the input voltage is below the undervoltage threshold, the device shuts down and the internal switch FET is turned off. If the input voltage rises by undervoltage lockout hysteresis, the IC restarts.

7.3.4 Thermal Shutdown

An internal thermal shutdown turns off the device when the typical junction temperature exceeds 160°C. The device is released from shutdown automatically when the junction temperature decreases by 15°C.

7.4 Device Functional Modes

7.4.1 Shutdown

The TPS61165-Q1 enters shutdown mode when the CTRL voltage is logic low for more than 2.5 ms. During shutdown, the input supply current for the device is less than 1 µA (maximum). Although the internal FET does not switch in shutdown, there is still a DC current path between the input and the LEDs through the inductor and Schottky diode. The minimum forward voltage of the LED array must exceed the maximum input voltage to ensure that the LEDs remain off in shutdown.

7.5 Programming

7.5.1 Current Program

The FB voltage is regulated by a low 0.2-V reference voltage. The LED current is programmed externally using a current-sense resistor in series with the LED string. The value of the R_{SET} is calculated using Equation 1.

$$I_{LED} = \frac{V_{FB}}{R_{SET}}$$

where

- I_{LED} = output current of LEDs
- V_{FB} = regulated voltage of FB
- R_{SET} = current sense resistor (1)

The output current tolerance depends on the FB accuracy and the current sensor resistor accuracy.

7.5.2 LED Brightness Dimming Mode Selection

The CTRL pin is used for the control input for both dimming modes, PWM dimming and the 1 wire dimming. The dimming mode for the TPS61165-Q1 device is selected each time the device is enabled. The default dimming mode is PWM dimming. To enter 1-wire mode, the following digital pattern on the CTRL pin must be recognized by the IC every time the IC starts from the shutdown mode.

1. Pull CTRL pin high to enable the TPS61165-Q1 device, and to start the 1-wire detection window.
2. After the EasyScale detection delay (t_{es_delay}, 100 µs) expires, drive CTRL low for more than the EasyScale detection time (t_{es_detect}, 260 µs).
3. The CTRL pin must be low for more than EasyScale detection time before the EasyScale detection window (t_{es_win}, 1 ms) expires. EasyScale detection window starts from the first CTRL pin low to high transition.

Programming (continued)

The IC immediately enters the 1-wire mode once the above three conditions are met. the EasyScale communication can start before the detection window expires. Once the dimming mode is programmed, it cannot be changed without another start-up. This means the IC needs to be shut down by pulling the CTRL low for 2.5 ms and restarts. See the *Dimming Mode Detection and Soft Start* (see Figure 11) for a graphical explanation.

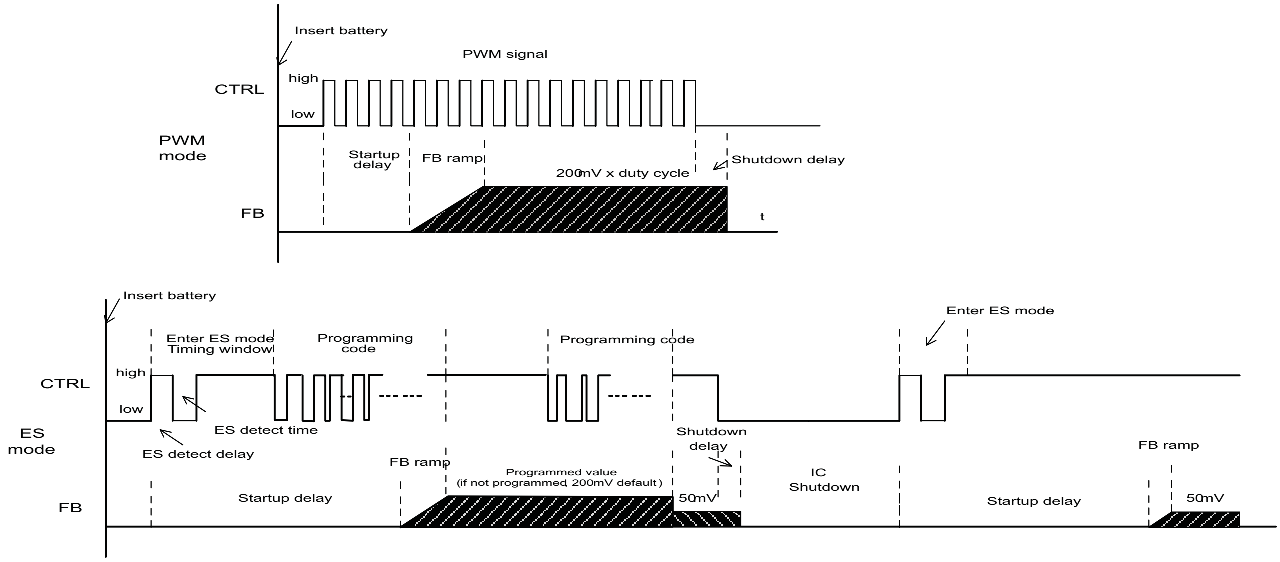


Figure 11. Dimming Mode Detection and Soft Start PWM Brightness Dimming

7.5.3 PWM Brightness Dimming

When the CTRL pin is constantly high, the FB voltage is regulated to 200 mV typically. However, the CTRL pin allows a PWM signal to reduce this regulation voltage; therefore, it achieves LED brightness dimming. The relationship between the duty cycle and FB voltage is given by Equation 2:

$$V_{FB} = \text{Duty} \times 200\ \text{mV}$$

where

- Duty = duty cycle of the PWM signal
- 200 mV = internal reference voltage (2)

As shown in Figure 12, the IC chops up the internal 200-mV reference voltage at the duty cycle of the PWM signal. The pulse signal is then filtered by an internal low pass filter. The output of the filter is connected to the error amplifier as the reference voltage for the FB pin regulation. Therefore, although a PWM signal is used for brightness dimming, only the WLED DC current is modulated, which is often referred as analog dimming. This eliminates the audible noise which often occurs when the LED current is pulsed in replica of the frequency and duty cycle of PWM control. Unlike other methods which filters the PWM signal for analog dimming, TPS61165-Q1 device's regulation voltage is independent of the PWM logic voltage level which often has large variations.

For optimum performance, use the PWM dimming frequency in the range of 5 kHz to 100 kHz. The requirement of minimum dimming frequency comes from the EasyScale detection delay and detection time specification in the dimming mode selection. Because the CTRL pin is logic only pin, adding an external RC filter applied to the pin does not work.

To use lower PWM dimming, add external RC network connected to the FB pin as shown in the additional typical application, .

Programming (continued)

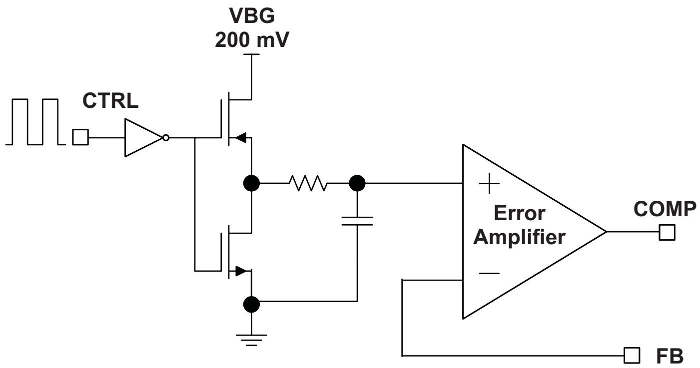


Figure 12. Block Diagram of Programmable FB Voltage Using PWM Signal

7.5.4 Digital 1 Wire Brightness Dimming

The CTRL pin features a simple digital interface to allow digital brightness control. The digital dimming can save the processor power and battery life as it does not require a PWM signal all the time, and the processor can enter idle mode if available.

The TPS61165-Q1 device adopts the EasyScale protocol for the digital dimming, which can program the FB voltage to any of the 32 steps with single command. The step increment increases with the voltage to produce pseudo logarithmic curve for the brightness step. See Table 2 for the FB pin voltage steps. The default step is full scale when the device is first enabled (V_{FB} = 200 mV). The programmed reference voltage is stored in an internal register and will not be changed by pulling CTRL low for 2.5 ms and then re-enabling the IC by taking CTRL high. A power reset clears the register value and reset it to default.

7.5.5 EasyScale: 1 Wire Digital Dimming

EasyScale is a simple but flexible 1-pin interface to configure the FB voltage. The interface is based on a master-slave structure, where the master is typically a microcontroller or application processor. Figure 13 and Table 3 give an overview of the protocol. The protocol consists of a device specific address byte and a data byte. The device specific address byte is fixed to 72 hex. The data byte consists of 5 bits for information, 2 address bits, and the RFA bit. The RFA bit set to high indicates the *Request for Acknowledge* condition. The Acknowledge condition is applied only if the protocol was received correctly. The advantage of EasyScale compared with other 1-pin interfaces is that its bit detection is in a large extent independent from the bit transmission rate. It can automatically detect bit rates between 1.7 kbps and up to 160 kbps.

Table 2. Selectable FB Voltage

	FB voltage (mV)	D4	D3	D2	D1	D0
0	0	0	0	0	0	0
1	5	0	0	0	0	1
2	8	0	0	0	1	0
3	11	0	0	0	1	1
4	14	0	0	1	0	0
5	17	0	0	1	0	1
6	20	0	0	1	1	0
7	23	0	0	1	1	1
8	26	0	1	0	0	0
9	29	0	1	0	0	1
10	32	0	1	0	1	0
11	35	0	1	0	1	1
12	38	0	1	1	0	0

Table 2. Selectable FB Voltage (continued)

	FB voltage (mV)	D4	D3	D2	D1	D0
13	44	0	1	1	0	1
14	50	0	1	1	1	0
15	56	0	1	1	1	1
16	62	1	0	0	0	0
17	68	1	0	0	0	1
18	74	1	0	0	1	0
19	80	1	0	0	1	1
20	86	1	0	1	0	0
21	92	1	0	1	0	1
22	98	1	0	1	1	0
23	104	1	0	1	1	1
24	116	1	1	0	0	0
25	128	1	1	0	0	1
26	140	1	1	0	1	0
27	152	1	1	0	1	1
28	164	1	1	1	0	0
29	176	1	1	1	0	1
30	188	1	1	1	1	0
31	200	1	1	1	1	1

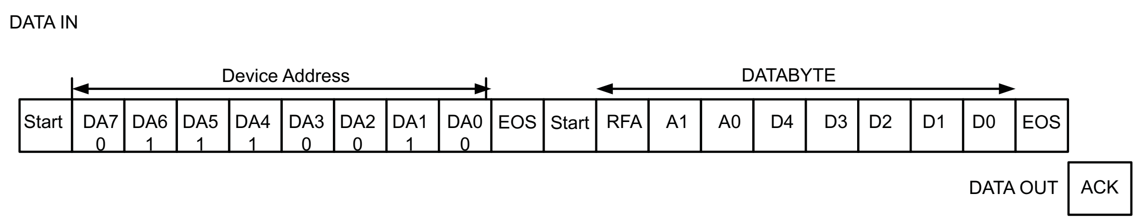


Figure 13. EasyScale Protocol Overview

Table 3. EasyScale Bit Description

BYTE	BIT NUMBER	NAME	TRANSMISSION DIRECTION	DESCRIPTION
Device Address Byte 72 hex	7	DA7	IN	0 MSB device address
	6	DA6		1
	5	DA5		1
	4	DA4		1
	3	DA3		0
	2	DA2		0
	1	DA1		1
	0	DA0		0 LSB device address

Table 3. EasyScale Bit Description (continued)

BYTE	BIT NUMBER	NAME	TRANSMISSION DIRECTION	DESCRIPTION
Data byte	7 (MSB)	RFA	IN	Request for acknowledge. If high, acknowledge is applied by device
	6	A1		0 Address bit 1
	5	A0		0 Address bit 0
	4	D4		Data bit 4
	3	D3		Data bit 3
	2	D2		Data bit 2
	1	D1		Data bit 1
	0 (LSB)	D0		Data bit 0
		ACK	OUT	Acknowledge condition active 0, this condition will only be applied in case RFA bit is set. Open-drain output, Line needs to be pulled high by the host with a pullup resistor. This feature can only be used if the master has an open-drain output stage. In case of a push-pull output stage Acknowledge condition may not be requested!

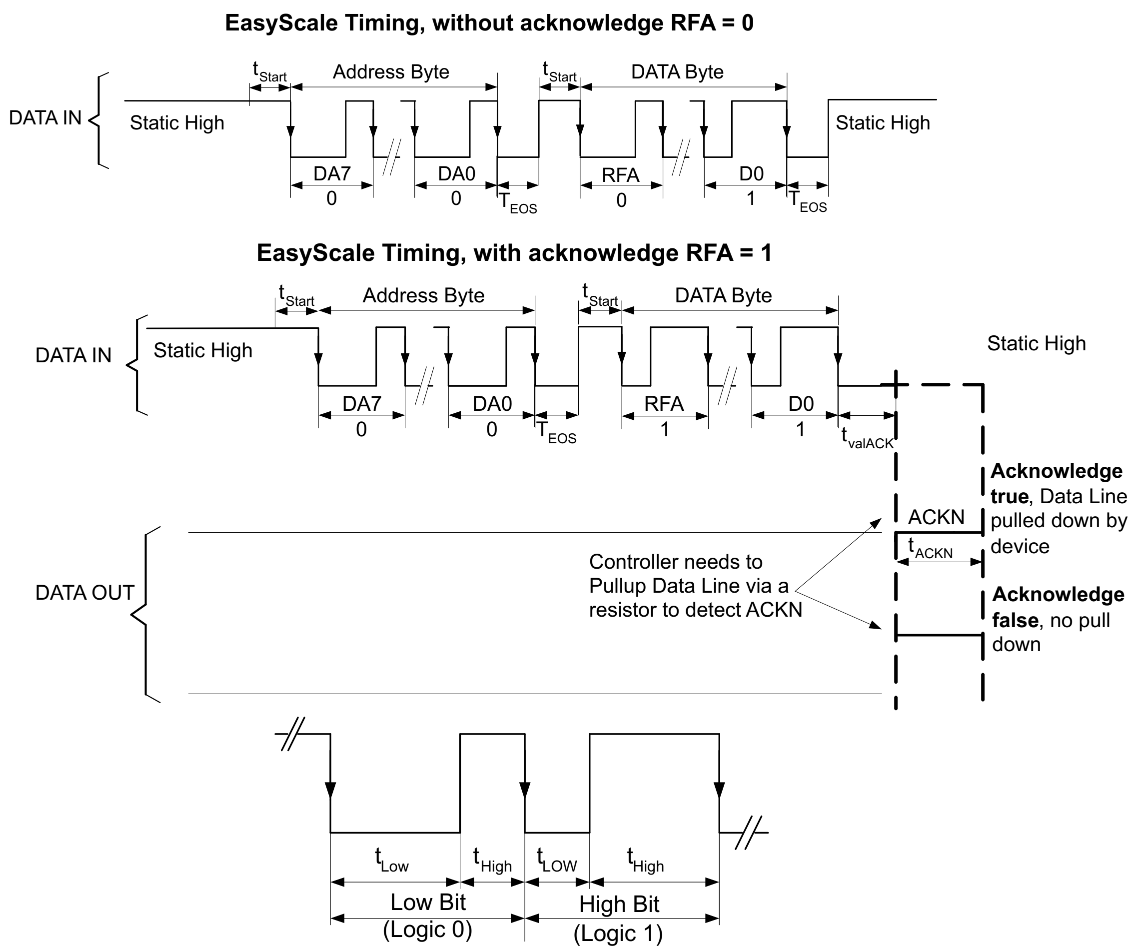


Figure 14. EasyScale— Bit Coding

All bits are transmitted MSB first and LSB last. Figure 14 shows the protocol without acknowledge request (Bit RFA = 0), Figure 14 with acknowledge (Bit RFA = 1) request. Before both bytes, device address byte and data byte, a start condition must be applied. For this, the CTRL pin must be pulled high for at least t_{start} (2 µs) before the bit transmission starts with the falling edge. If the CTRL pin is already at a high level, no start condition is needed before the device address byte. The transmission of each byte is closed with an End of Stream condition for at least t_{EOS} (2 µs).

The bit detection is based on a Logic Detection scheme, where the criterion is the relation between t_{LOW} and t_{HIGH}. It can be simplified to:

High Bit: $t_{HIGH} > t_{LOW}$, but with t_{HIGH} at least 2x t_{LOW}, see Figure 14.

Low Bit: $t_{HIGH} < t_{LOW}$, but with t_{LOW} at least 2x t_{HIGH}, see Figure 14.

The bit detection starts with a falling edge on the CTRL pin and ends with the next falling edge. Depending on the relation between t_{HIGH} and t_{LOW}, the logic 0 or 1 is detected.

The acknowledge condition is only applied if:

- Acknowledge is requested by a set RFA bit.
- The transmitted device address matches with the device address of the device.
- 16 bits is received correctly.

If the device turns on the internal ACKN-MOSFET and pulls the CTRL pin low for the time t_{ACKN}, which is 512 µs maximum then the Acknowledge condition is valid after an internal delay time t_{valACK}. This means that the internal ACKN-MOSFET is turned on after t_{valACK}, when the last falling edge of the protocol was detected. The master controller keeps the line low in this period. The master device can detect the acknowledge condition with its input by releasing the CTRL pin after t_{valACK} and read back a logic 0. The CTRL pin can be used again after the acknowledge condition ends.

The acknowledge condition may only be requested if the master device has an open-drain output. For a push-pull output stage, the use a series resistor in the CRTL line to limit the current to 500 µA is recommended to for such cases as:

- Accidentally requested acknowledge.
- Protect the internal ACKN-MOSFET.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS61165-Q1 device drives 6 high-brightness LEDs; the LED current is set at 350 mA. A 12-V Zener diode is used to clamp the input voltage, which makes the TPS61165-Q1 device suitable for car battery supply applications.

8.2 Typical Application

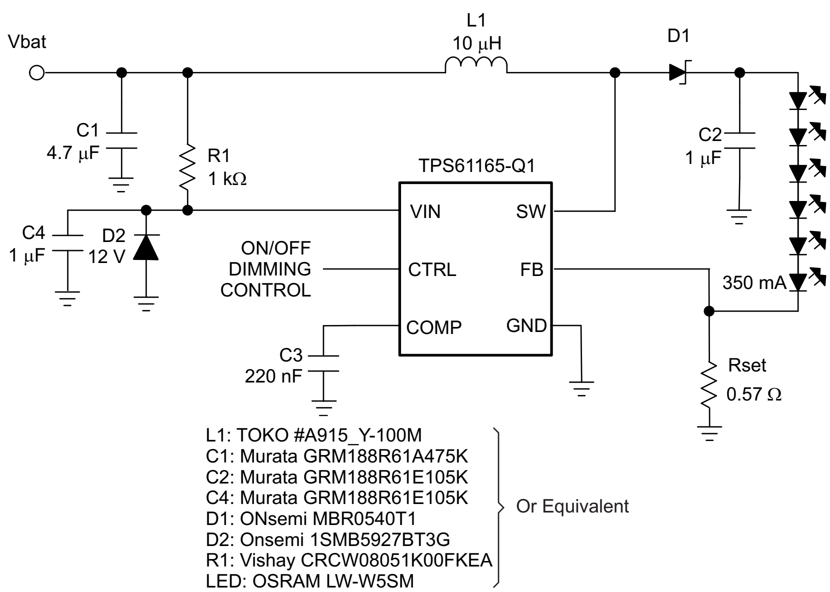


Figure 15. Drive Six High-Brightness LEDs

For assistance in selecting the proper values, the detailed external PWM dimming network for the specific application, see SLVA471 and/or SLVC366.

8.2.1 Design Requirements

Table 4 lists the input parameters for this design example.

Table 4. Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Brightness control	PWM Dimming
Input voltage	12 V
Output current	350 mA
LED loads	6 LEDs

8.2.2 Detailed Design Procedures

8.2.2.1 Maximum Output Current

The overcurrent limit in a boost converter limits the maximum input current and thus maximum input power for a given input voltage. Maximum output power is less than maximum input power due to power conversion losses. Therefore, the current limit setting, input voltage, output voltage and efficiency can all change maximum current output. The current limit clamps the peak inductor current; therefore, the ripple must be subtracted to derive maximum DC current. The ripple current is a function of switching frequency, inductor value and duty cycle. Use Equation 3 and Equation 4 consider of all the above factors for maximum output current calculation.

$$I_P = \frac{1}{\left[L \times F_s \times \left(\frac{1}{V_{out} + V_f - V_{in}} + \frac{1}{V_{in}}\right)\right]}$$

where

- I_p = inductor peak to peak ripple
- L = inductor value
- V_f = Schottky diode forward voltage
- Fs = switching frequency
- V_{out} = output voltage of the boost converter. It is equal to the sum of VFB and the voltage drop across LEDs. (3)

$$I_{out\_max} = \frac{V_{in} \times (I_{lim} - I_p / 2) \times \eta}{V_{out}}$$

where

- I_{out_max} = Maximum output current of the boost converter
- I_{lim} = over current limit
- η = efficiency (4)

For instance, when VIN is 3 V, 8 LEDs output equivalent to VOUT of 26 V, the inductor is 22 μH, the Schottky forward voltage is 0.2 V; and then the maximum output current is 110 mA in typical condition. When VIN is 5 V, 10 LEDs output equivalent to VOUT of 32 V, the inductor is 22 μH, the Schottky forward voltage is 0.2 V; and then the maximum output current is 150 mA in typical condition.

8.2.2.2 Inductor Selection

The selection of the inductor affects steady state operation as well as transient behavior and loop stability. These factors make it the most important component in power regulator design. There are three important inductor specifications, inductor value, DC resistance and saturation current. Considering inductor value alone is not enough.

The inductor value determines the inductor ripple current. Choose an inductor that can handle the necessary peak current without saturating, according to half of the peak-to-peak ripple current given by Equation 3, pause the inductor DC current given by:

$$I_{in\_DC} = \frac{V_{out} \times I_{out}}{V_{in} \times \eta} \quad (5)$$

Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the 0 A value depending on how the inductor vendor defines saturation current. Using an inductor with a smaller inductance value forces discontinuous PWM when the inductor current ramps down to zero before the end of each switching cycle. This reduces the boost converter’s maximum output current, causes large input voltage ripple and reduces efficiency. Large inductance value provides much more output current and higher conversion efficiency. For these reasons, a 10 μH to 22 μH inductor value range is recommended. A 22 μH inductor optimized the efficiency for most application while maintaining low inductor peak to peak ripple. Table 5 lists the recommended inductor for the TPS61165-Q1 device. When recommending inductor value, the factory has considered –40% and +20% tolerance from its nominal value.

TPS61165-Q1 device has built-in slope compensation to avoid subharmonic oscillation associated with current mode control. If the inductor value is lower than 10 µH, the slope compensation may not be adequate, and the loop can be unstable. Therefore, customers need to verify the inductor in their application if it is different from the recommended values.

Table 5. Recommended Inductors for TPS61165-Q1

PART NUMBER	L (µH)	DCR MAX (mΩ)	SATURATION CURRENT (A)	SIZE (L × W × H mm)	VENDOR
A915_Y-100M	10	90	1.3	5.2 × 5.2 × 3	TOKO
VLCF5020T-100M1R1-1	10	237	1.1	5 × 5 × 2	TDK
CDRH4D22/HP	10	144	1.2	5 × 5 × 2.4	Sumida
LQH43PN100MR0	10	247	0.84	4.5 × 3.2 × 2	Murata

8.2.2.3 Schottky Diode Selection

The high switching frequency of the TPS61165-Q1 device demands a high-speed rectification for optimum efficiency. Ensure that the diode's average and peak current rating exceeds the average output current and peak inductor current. In addition, the reverse breakdown voltage of the diode must exceed the open LED protection voltage. The ONSemi MBR0540 and the ZETEX ZHCS400 are recommended for the TPS61165-Q1 device.

8.2.2.4 Compensation Capacitor Selection

The compensation capacitor C3 (see *Functional Block Diagram*), connected from COMP pin to GND, is used to stabilize the feedback loop of the TPS61165-Q1 device. A 220-nF ceramic capacitor is suitable for most applications.

8.2.2.5 Input and Output Capacitor Selection

The output capacitor is mainly selected to meet the requirements for the output ripple and loop stability. This ripple voltage is related to the capacitance of the capacitor and its equivalent series resistance (ESR). Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated using Equation 6.

$$C_{out} = \frac{(V_{out} - V_{in})\, I_{out}}{V_{out} \times F_s \times V_{ripple}}$$

where

- V_{ripple} = peak-to-peak output ripple (6)

The additional output ripple component caused by ESR is calculated using Equation 7

$$V_{ripple\_ESR} = I_{out} \times R_{ESR} \tag{7}$$

Due to its low ESR, V_{ripple_ESR} can be neglected for ceramic capacitors, but must be considered if tantalum or electrolytic capacitors are used.

Care must be taken when evaluating a ceramic capacitors derating under DC bias, aging and AC signal. For example, larger form factor capacitors (in 1206 size) have a self resonant frequencies in the range of the switching frequency. So the effective capacitance is significantly lower. The DC bias can also significantly reduce capacitance. Ceramic capacitors can loss as much as 50% of its capacitance at its rated voltage. Therefore, leave the margin on the voltage rating to ensure adequate capacitance at the required output voltage.

The capacitor in the range of 1 µF to 4.7 µF is recommended for input side. The output requires a capacitor in the range of 1 µF to 10 µF. The output capacitor affects the loop stability of the boost regulator. If the output capacitor is below the range, the boost regulator can potentially become unstable.

The popular vendors for high value ceramic capacitors are:

TDK (http://www.component.tdk.com/components.php)

Murata (http://www.murata.com/cap/index.html)

8.2.3 Application Curves

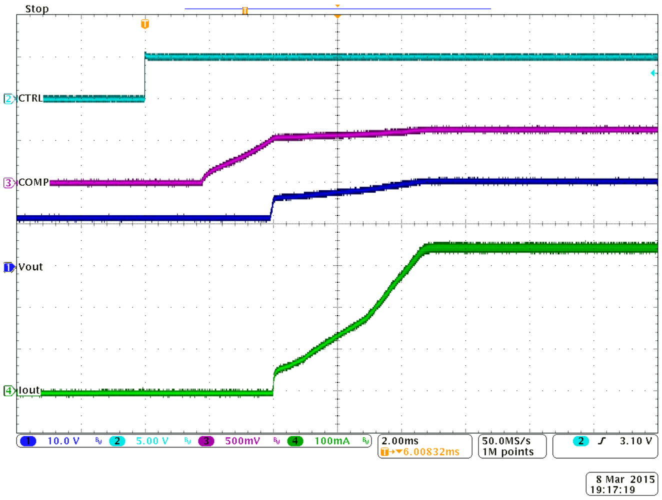


Figure 16. Start-Up Waveform

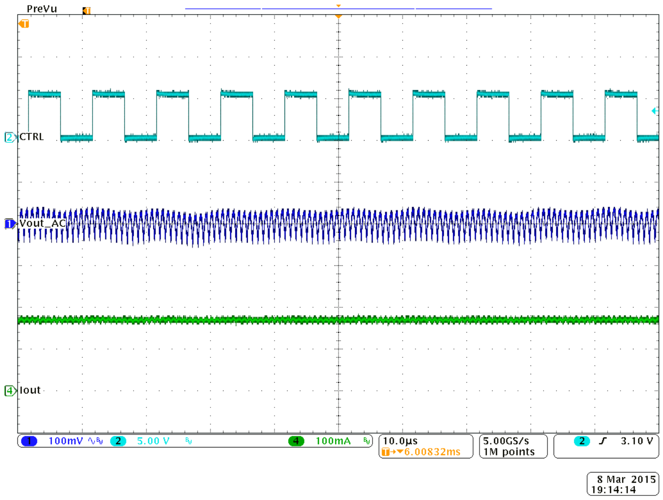


Figure 17. 100 kHz PWM Dimming Waveform Under 50% Duty Cycle

8.3 Do's and Don'ts

There is a known issue with the TPS61165-Q1 device when using the EasyScale interface to increase the feedback voltage. When VFB is increased from 0 mV to any value more than 0 mV, some ICs do not properly soft-start during this transition and the voltage on their SW pin overshoots. If the overshoot exceeds the absolute maximum voltage rating on the SW pin, the IC is damaged.

With VFB set below 10 mV through EasyScale, the parasitic offsets on the input pins of the internal transconductance amplifier determine the value of output of the amplifier. IC process variations are causing the offset to be larger and in the opposite polarity than expected. If the amplifier's output is already high before a transition from VFB = 0 mV to any other voltage, then the modulator turns on full, bypassing soft start, and causes the SW pin and output voltage to overshoot.

To avoid this issue do not use EasyScale to change the feedback voltage from 0 mV, effectively disabling the device, to any other voltage. One alternative is to start with VFB = 10 mV and go to a higher voltage. Another alternative is to disable the IC by taking the CTRL pin low for 2.5 ms and then re-enter EasyScale to force a soft start from VFB = 0 mV to the default 200 mV.

9 Power Supply Recommendations

The TPS61165-Q1 device requires a single supply input voltage. This voltage can range from 3 V to 18 V and be able to supply enough current for a given application.

10 Layout

10.1 Layout Guidelines

As for all switching power supplies, especially those high frequency and high current ones, layout is an important design step. If layout is not carefully done, the regulator could suffer from instability as well as noise problems. To reduce switching losses, the SW pin rise and fall times are made as short as possible. To prevent radiation of high frequency resonance problems, proper layout of the high frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin and always use a ground plane under the switching regulator to minimize inter-plane coupling. The loop including the PWM switch, Schottky diode, and output capacitor, contains high current rising and falling in nanosecond and should be kept as short as possible. The input capacitor needs not only to be close to the VIN pin, but also to the GND pin to reduce the IC supply ripple.

10.2 Layout Example

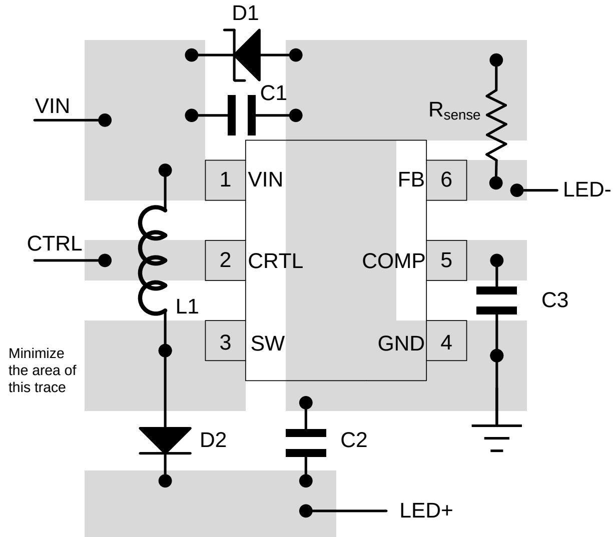


Figure 18. Recommended Layout Example

10.3 Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation of the TPS61165-Q1 device. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation 8:

$$P_{D(max)} = \frac{125°C - T_A}{R_{\theta JA}} \tag{8}$$

where

- T_A is the maximum ambient temperature for the application
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient given in *Thermal Information* Table (8)

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *How to Use Analog Dimming With the TPS6116x*, SLVA471
- *Design Tool for Analog Dimming using a PWM Signal*, SLVC366

11.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

EasyScale, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61165TDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	SBM	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS61165-Q1 :

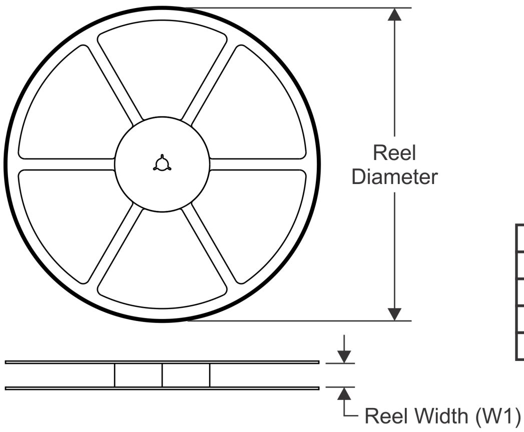
- Catalog: TPS61165

NOTE: Qualified Version Definitions:

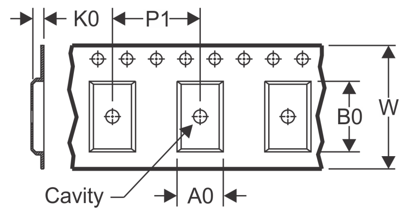
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

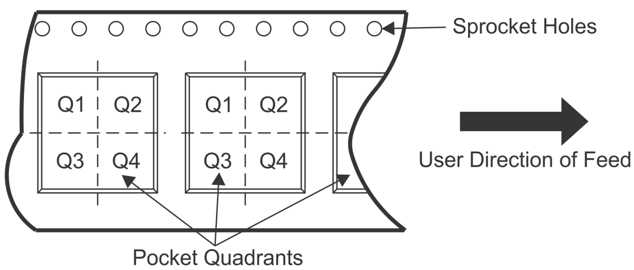


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

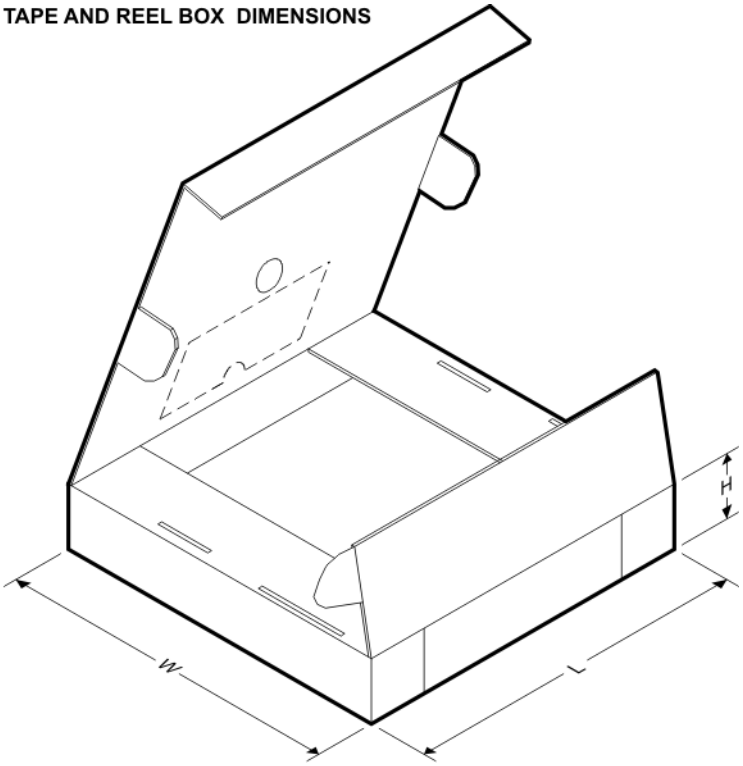
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

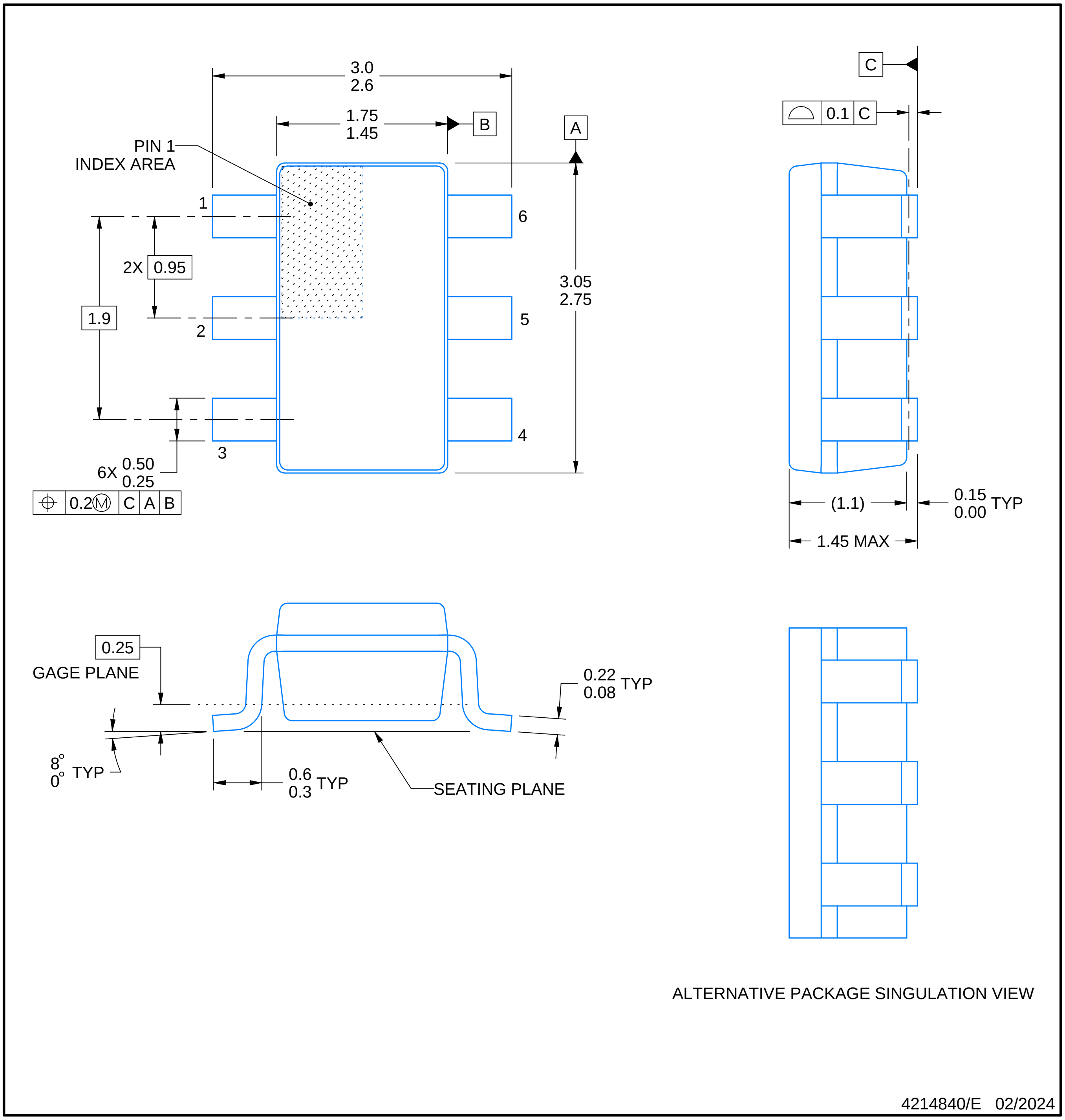
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61165TDBVRQ1	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



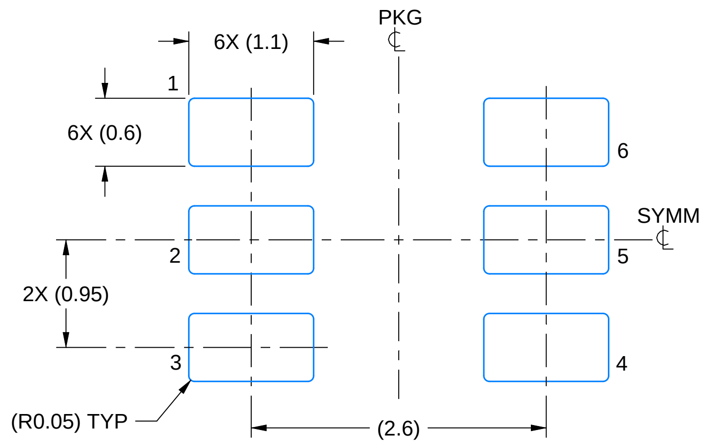
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61165TDBVRQ1	SOT-23	DBV	6	3000	200.0	183.0	25.0

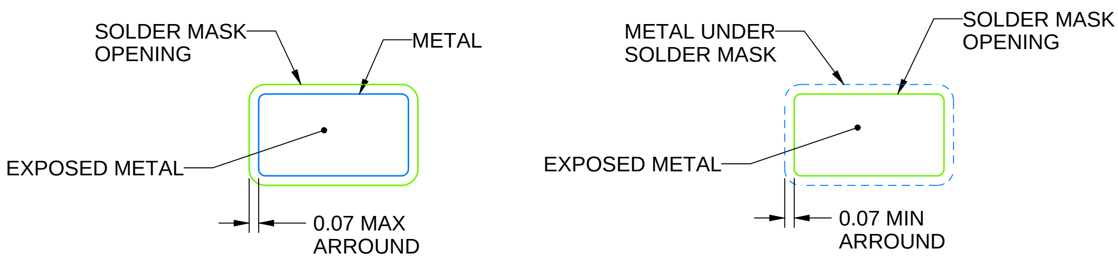


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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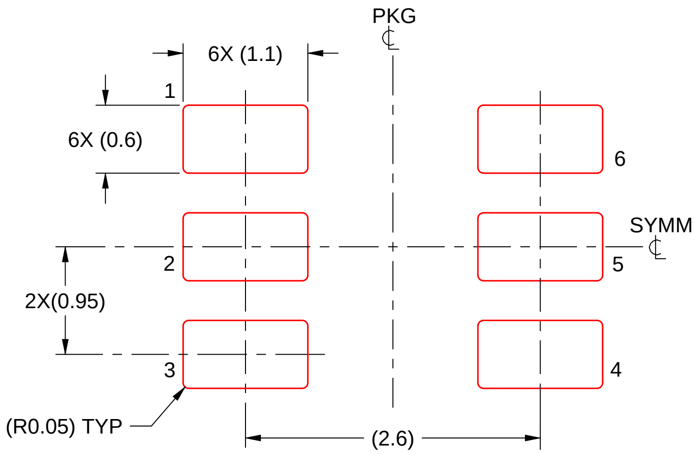
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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