1 Features

- Qualified for Automotive Applications
- 40-V Maximum Breakdown Voltage of Internal MOSFET
- 38-V Open LED Protection
- 200-mV Reference Voltage With 2% Accuracy
- 1.2-A Switch FET With 1.2-MHz Switching Frequency
- Flexible 1-Wire Digital and PWM Brightness Control
- Built-in Soft Start
- Up to 90% Efficiency
- SOT-23 Package

2 Applications

- High-Brightness LED Lighting
- White LED Backlighting for Media Form Factor Display
- Automotive Cluster Backlighting

3 Description

With a 40-V rated integrated switch FET, the TPS61165-Q1 device is a boost converter that drives LEDs in series. The boost converter runs at a 1.2-MHz fixed switching frequency with 1.2-A switch current limit, and allows for the use of a high brightness LED in general lighting.

The default white LED current is set with the external sensor resistor Rset, and the feedback voltage is regulated to 200 mV, as shown in the Typical Application section. During the operation, the LED current can be controlled using the 1-wire digital interface (EasyScale™ protocol) through the CTRL pin. Alternatively, a pulse width modulation (PWM) signal can be applied to the CTRL pin through which the duty cycle determines the feedback reference voltage. In either digital or PWM mode, the TPS61165-Q1 device does not burst the LED current; therefore, the device does not generate audible noises on the output capacitor. For maximum protection, the TPS61165-Q1 device features integrated open LED protection that disables it to prevent the output from exceeding its absolute maximum voltage ratings during open LED conditions.

The TPS61165-Q1 device is available in a SOT-23 package.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS61165-Q1</td>
<td>SOT-23</td>
<td>1.60 mm × 2.90 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic
Table of Contents

1 Features ................................................................. 1
2 Applications .......................................................... 1
3 Description ............................................................. 1
4 Revision History ...................................................... 2
5 Pin Configuration and Functions ............................... 3
6 Specifications ........................................................ 3
   6.1 Absolute Maximum Ratings .................................. 3
   6.2 ESD Ratings ...................................................... 3
   6.3 Recommended Operating Conditions ..................... 4
   6.4 Thermal Information ........................................... 4
   6.5 Electrical Characteristics ................................... 4
   6.6 Timing Requirements ......................................... 5
   6.7 Typical Characteristics ....................................... 6
7 Detailed Description ............................................... 8
   7.1 Overview ........................................................ 8
   7.2 Functional Block Diagram .................................. 8
   7.3 Feature Description .......................................... 8
   7.4 Device Functional Modes .................................... 9
8 Application and Implementation .............................. 15
   8.1 Application Information ..................................... 15
   8.2 Typical Application .......................................... 15
   8.3 Do's and Don'ts ............................................... 18
9 Power Supply Recommendations .............................. 18
10 Layout ................................................................. 18
   10.1 Layout Guidelines .......................................... 18
   10.2 Layout Example ............................................... 19
   10.3 Thermal Considerations ................................... 19
11 Device and Documentation Support ........................... 20
   11.1 Device Support .............................................. 20
   11.2 Documentation Support ................................... 20
   11.3 Community Resource ....................................... 20
   11.4 Trademarks ................................................... 20
   11.5 Electrostatic Discharge Caution .......................... 20
   11.6 Glossary ...................................................... 20
12 Mechanical, Packaging, and Orderable Information ....... 20

4 Revision History

Changes from Revision A (September 2013) to Revision B Page

- Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ................................................................. 1
5 Pin Configuration and Functions

![Pin Configuration Diagram]

### Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>NAME</th>
<th>NO.</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>COMP</td>
<td>5</td>
<td>O</td>
<td>Output of the transconductance error amplifier. Connect an external capacitor to this pin to compensate the converter.</td>
<td></td>
</tr>
<tr>
<td>CTRL</td>
<td>2</td>
<td>I</td>
<td>Control pin of the boost converter. It is a multi-functional pin which can be used for enable control, PWM, and digital dimming.</td>
<td></td>
</tr>
<tr>
<td>FB</td>
<td>6</td>
<td>I</td>
<td>Feedback pin for current. Connect the sense resistor from FB to GND.</td>
<td></td>
</tr>
<tr>
<td>GND</td>
<td>4</td>
<td>O</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>SW</td>
<td>3</td>
<td>I</td>
<td>This is the switching node of the IC. Connect the switched side of the inductor to SW. This pin is also used to sense the output voltage for open LED protection.</td>
<td></td>
</tr>
<tr>
<td>VIN</td>
<td>1</td>
<td>I</td>
<td>The input supply pin for the IC. Connect VIN to a supply voltage between 3 V and 18 V.</td>
<td></td>
</tr>
</tbody>
</table>

### 6 Specifications

#### 6.1 Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltages on VIN</td>
<td>2</td>
<td>–0.3 to 20 V</td>
</tr>
<tr>
<td>Voltages on CTRL</td>
<td>2</td>
<td>–0.3 to 20 V</td>
</tr>
<tr>
<td>Voltage on FB and COMP</td>
<td>2</td>
<td>–0.3 to 3 V</td>
</tr>
<tr>
<td>Voltage on SW</td>
<td>3</td>
<td>–0.3 to 40 V</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>–0.3</td>
<td>V</td>
</tr>
<tr>
<td>20</td>
<td></td>
</tr>
<tr>
<td>–0.3</td>
<td>V</td>
</tr>
<tr>
<td>20</td>
<td></td>
</tr>
<tr>
<td>–0.3</td>
<td>V</td>
</tr>
<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>–0.3</td>
<td>V</td>
</tr>
<tr>
<td>40</td>
<td></td>
</tr>
</tbody>
</table>

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>±1000</td>
<td>V</td>
</tr>
<tr>
<td>±1000</td>
<td>V</td>
</tr>
<tr>
<td>±1000</td>
<td>V</td>
</tr>
<tr>
<td>±100</td>
<td></td>
</tr>
</tbody>
</table>

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
6.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>V&lt;sub&gt;IN&lt;/sub&gt;</strong> Input voltage range, VIN</td>
<td>3</td>
<td>18</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td><strong>V&lt;sub&gt;OUT&lt;/sub&gt;</strong> Output voltage range</td>
<td>VIN</td>
<td>38</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td><strong>L</strong> Inductor&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>10</td>
<td>22</td>
<td></td>
<td>μH</td>
</tr>
<tr>
<td>**f&lt;sub&gt;dim&lt;/sub&gt;&lt;/sup&gt; PWM dimming frequency</td>
<td>5</td>
<td>100</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td><strong>C&lt;sub&gt;IN&lt;/sub&gt;</strong> Input capacitor</td>
<td>1</td>
<td></td>
<td></td>
<td>μF</td>
</tr>
<tr>
<td><strong>C&lt;sub&gt;OUT&lt;/sub&gt;</strong> Output capacitor</td>
<td>1</td>
<td>10</td>
<td></td>
<td>μF</td>
</tr>
<tr>
<td><strong>T&lt;sub&gt;A&lt;/sub&gt;</strong> Operating ambient temperature</td>
<td>–40</td>
<td>105</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td><strong>T&lt;sub&gt;J&lt;/sub&gt;</strong> Operating junction temperature</td>
<td>–40</td>
<td>125</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

(1) These values are recommended values that have been successfully tested in several applications. Other values may be acceptable in other applications but should be fully tested by the user.

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC&lt;sup&gt;(1)&lt;/sup&gt;</th>
<th>TPS61165-Q1</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>R&lt;sub&gt;θJA&lt;/sub&gt;</strong> Junction-to-ambient thermal resistance</td>
<td>210.1</td>
<td>°C/W</td>
</tr>
<tr>
<td><strong>R&lt;sub&gt;θJC(top)&lt;/sub&gt;</strong> Junction-to-case (top) thermal resistance</td>
<td>46.8</td>
<td>°C/W</td>
</tr>
<tr>
<td><strong>R&lt;sub&gt;θJB&lt;/sub&gt;</strong> Junction-to-board thermal resistance</td>
<td>56.7</td>
<td>°C/W</td>
</tr>
<tr>
<td>**ψ&lt;sub&gt;JT&lt;/sub&gt;&lt;/sup&gt; Junction-to-top characterization parameter</td>
<td>0.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>**ψ&lt;sub&gt;JB&lt;/sub&gt;&lt;/sup&gt; Junction-to-board characterization parameter</td>
<td>50.2</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

VIN = 3.6 V, CTRL = VIN, T<sub>A</sub> = –40°C to 105°C, typical values are at T<sub>A</sub> = 25°C (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SUPPLY CURRENT</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>V&lt;sub&gt;IN&lt;/sub&gt;</strong> Input voltage range, VIN</td>
<td></td>
<td>3</td>
<td>18</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>**I&lt;sub&gt;Q&lt;/sub&gt;&lt;/sup&gt; Operating quiescent current into VIN</td>
<td>Device PWM switching no load</td>
<td>2.3</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>**I&lt;sub&gt;SD&lt;/sub&gt;&lt;/sup&gt; Shutdown current</td>
<td>CRTL=GND, VIN = 4.2 V</td>
<td>2</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>UVLO</strong> Undervoltage lockout threshold</td>
<td>VIN falling</td>
<td>2.2</td>
<td>2.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td><strong>V&lt;sub&gt;UVLO&lt;/sub&gt;</strong> Undervoltage lockout hysterisis</td>
<td></td>
<td>70</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>ENABLE AND REFERENCE CONTROL</th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>V&lt;sub&gt;(CTRL&lt;h_AT)&lt;/sub&gt;</strong> CTRL logic high voltage</td>
<td>VIN = 3 V to 18 V</td>
<td>1.2</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>V&lt;sub&gt;(CTRL)L&lt;/sub&gt;</strong> CTRL logic low voltage</td>
<td>VIN = 3 V to 18 V</td>
<td>0.4</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>R&lt;sub&gt;(CTRL)&lt;/sub&gt;</strong> CTRL pulldown resistor</td>
<td></td>
<td>400</td>
<td>800</td>
<td>1600</td>
<td>kΩ</td>
</tr>
<tr>
<td>**t&lt;sub&gt;off&lt;/sub&gt;&lt;/sup&gt; CTRL pulse width to shutdown</td>
<td>CTRL high to low</td>
<td>2.5</td>
<td>ms</td>
<td></td>
<td></td>
</tr>
<tr>
<td>**t&lt;sub&gt;off_det&lt;/sub&gt;&lt;/sup&gt; EasyScale detection time&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>CTRL pin low</td>
<td>260</td>
<td>μs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>**t&lt;sub&gt;off_delay&lt;/sub&gt;&lt;/sup&gt; EasyScale detection delay</td>
<td></td>
<td>100</td>
<td>μs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>**t&lt;sub&gt;off_win&lt;/sub&gt;&lt;/sup&gt; EasyScale detection window time</td>
<td>Measured from CTRL high</td>
<td>1</td>
<td>ms</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>VOLTAGE AND CURRENT CONTROL</th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>**V&lt;sub&gt;REF&lt;/sub&gt;&lt;/sup&gt; Voltage feedback regulation voltage</td>
<td></td>
<td>196</td>
<td>200</td>
<td>204</td>
<td>mV</td>
</tr>
<tr>
<td><strong>V&lt;sub&gt;(REF,PWM)&lt;/sub&gt;</strong> Voltage feedback regulation voltage under brightness control</td>
<td>V&lt;sub&gt;FB&lt;/sub&gt; = 50 mV</td>
<td>47</td>
<td>50</td>
<td>53</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;FB&lt;/sub&gt; = 20 mV</td>
<td>17</td>
<td>20</td>
<td>23</td>
<td>mV</td>
</tr>
<tr>
<td>**I&lt;sub&gt;FB&lt;/sub&gt;&lt;/sup&gt; Voltage feedback input bias current</td>
<td>V&lt;sub&gt;FB&lt;/sub&gt; = 200 mV</td>
<td>2</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>**I&lt;sub&gt;FB&lt;/sub&gt;&lt;/sup&gt; Oscillator frequency</td>
<td></td>
<td>1</td>
<td>1.2</td>
<td>1.5</td>
<td>MHz</td>
</tr>
<tr>
<td><strong>D&lt;sub&gt;MAX&lt;/sub&gt;</strong> Maximum duty cycle</td>
<td>V&lt;sub&gt;FB&lt;/sub&gt; = 100 mV</td>
<td>90%</td>
<td>93%</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) For select EasyScale mode, the CTRL pin must be low for more than t<sub>off_det</sub> during t<sub>off_win</sub>.
Electrical Characteristics (continued)

VIN = 3.6 V, CTRL = VIN, T_A = –40°C to 105°C, typical values are at T_A = 25°C (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_{min_on}</td>
<td>Minimum on pulse width</td>
<td></td>
<td>40</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>I_{sink}</td>
<td>Comp pin sink current</td>
<td>100</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>I_{source}</td>
<td>Comp pin source current</td>
<td>100</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>G_{ea}</td>
<td>Error amplifier transconductance</td>
<td>240</td>
<td></td>
<td></td>
<td>umho</td>
</tr>
<tr>
<td>R_{ea}</td>
<td>Error amplifier output resistance</td>
<td>6</td>
<td></td>
<td></td>
<td>MΩ</td>
</tr>
<tr>
<td>f_{ea}</td>
<td>Error amplifier crossover frequency</td>
<td>5 pF connected to COMP</td>
<td>500</td>
<td></td>
<td>kHz</td>
</tr>
</tbody>
</table>

POWER SWITCH

| R_{DS(ON)}                             | N-channel MOSFET on-resistance | VIN = 3.6 V | 0.3 | 0.6 | Ω   |
| I_{LN, NFET}                           | N-channel leakage current | V_{SW} = 35 V, T_A = 25°C | 1   |     | μA  |

OC and OLP

| I_{LM}                                 | N-Channel MOSFET current limit | D = D_{max} | 0.96 | 1.2 | 1.44 | A |
| I_{LM, Start}                          | Start-up current limit | D = D_{max} | 0.7 |     |     | A |
| t_{Half_LIM}                           | Time step for half current limit | 5 |     |     | ms |
| V_{ovp}                                | Open LED protection threshold | Measured on the SW pin | 37 | 38  | 39  | V |
| V_{(FB_OVP)}                           | Open LED protection threshold on FB | Measured on the FB pin, percentage of Vref, Vref = 200 mV and 20 mV | 50% |
| t_{REF}                                | V_{REF} filter time constant | 180 |     |     | μs  |
| t_{step}                               | V_{REF} ramp up time | Each step measured as number of cycles of the 1.2-MHz clock | 213 |     | μs  |

THERMAL SHUTDOWN

| T_{shutdown}                           | Thermal shutdown threshold | 160 |     |     | °C  |
| T_{hysteresis}                         | Thermal shutdown threshold hysteresis | 15 |     |     | °C  |

6.6 Timing Requirements

<table>
<thead>
<tr>
<th>EasyScale TIMING</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_{start}</td>
<td>Start time of program stream</td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_{EOS}</td>
<td>End time of program stream</td>
<td>2</td>
<td>360</td>
<td></td>
</tr>
<tr>
<td>t_{H_LB}</td>
<td>High time low bit</td>
<td>Logic 0</td>
<td>2</td>
<td>180</td>
</tr>
<tr>
<td>t_{L_LB}</td>
<td>Low time low bit</td>
<td>Logic 0</td>
<td>2 × t_{L_LB}</td>
<td>360</td>
</tr>
<tr>
<td>t_{H_HB}</td>
<td>High time high bit</td>
<td>Logic 1</td>
<td>2 × t_{L_HB}</td>
<td>360</td>
</tr>
<tr>
<td>t_{L_HB}</td>
<td>Low time high bit</td>
<td>Logic 1</td>
<td>2</td>
<td>180</td>
</tr>
<tr>
<td>V_{ACKNL}</td>
<td>Acknowledge output voltage low</td>
<td>Open drain, R_{pullup} =15 kΩ to VIN</td>
<td>0.4</td>
<td></td>
</tr>
<tr>
<td>t_{valACKN}</td>
<td>Acknowledge valid time</td>
<td>See (1)</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>t_{ACKN}</td>
<td>Duration of acknowledge condition</td>
<td>See (1)</td>
<td>512</td>
<td></td>
</tr>
</tbody>
</table>

(1) Acknowledge condition active 0, this condition will only be applied in case the RFA bit is set. Open-drain output, line must be pulled high by the host with resistor load.
### 6.7 Typical Characteristics

#### Table 1. Table of Graphs

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Figure 1</td>
<td>Efficiency vs Output Current</td>
<td>3 LEDs (VOUT = 12 V); VIN = 3, 5, 8.5 V; L = 10 μH</td>
</tr>
<tr>
<td>Figure 2</td>
<td>Efficiency vs Output Current</td>
<td>6 LEDs (VOUT = 24 V); VIN = 5, 8.5, 12V; L = 10 μH</td>
</tr>
<tr>
<td>Figure 3</td>
<td>Current limit</td>
<td>T&lt;sub&gt;A&lt;/sub&gt; = 25°C</td>
</tr>
<tr>
<td>Figure 4</td>
<td>Current limit</td>
<td>T&lt;sub&gt;A&lt;/sub&gt; = 25°C</td>
</tr>
<tr>
<td>Figure 5</td>
<td>EasyScale step</td>
<td>VIN = 3.6 V; PWM Freq = 10 kHz and 32 kHz</td>
</tr>
<tr>
<td>Figure 6</td>
<td>Switch Current Limit vs Temperature</td>
<td>VIN = 3.6 V; VIN = 5 V; I&lt;sub&gt;LOAD&lt;/sub&gt; = 350 mA; PWM = 32 kHz</td>
</tr>
<tr>
<td>Figure 7</td>
<td>Output ripple at PWM dimming</td>
<td>3 LEDs; VIN = 5 V; VIN = 3.6 V; I&lt;sub&gt;LOAD&lt;/sub&gt; = 350 mA; PWM = 32 kHz</td>
</tr>
<tr>
<td>Figure 8</td>
<td>Switching waveform</td>
<td>3 LEDs; VIN = 5 V; VIN = 3.6 V; I&lt;sub&gt;LOAD&lt;/sub&gt; = 350 mA; PWM = 32 kHz</td>
</tr>
<tr>
<td>Figure 9</td>
<td>Start-up</td>
<td>3 LEDs; VIN = 5 V; VIN = 3.6 V; I&lt;sub&gt;LOAD&lt;/sub&gt; = 350 mA; PWM = 32 kHz</td>
</tr>
<tr>
<td>Figure 10</td>
<td>Open LED protection</td>
<td>8 LEDs; VIN = 3.6 V; I&lt;sub&gt;LOAD&lt;/sub&gt; = 20 mA</td>
</tr>
</tbody>
</table>

![Figure 1. Efficiency vs Output Current](image1.png)

![Figure 2. Efficiency vs Output Current](image2.png)

![Figure 3. Switch Current Limit vs Duty Cycle](image3.png)

![Figure 4. Switch Current Limit vs Temperature](image4.png)
Figure 5. FB Voltage vs EasyScale Step

Figure 6. FB Voltage vs PWM Duty Cycle

Figure 7. Output Ripple at PWM Dimming

Figure 8. Switching Waveform

Figure 9. Start-Up

Figure 10. Open LED Protection

TPS61165-Q1

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7 Detailed Description

7.1 Overview

The TPS61165-Q1 device is a high-efficiency, high-output voltage boost converter in small package size. The device is ideal for driving white LEDs in series. The serial LED connection provides even illumination by sourcing the same output current through all LEDs, eliminating the need for expensive factory calibration. The device integrates 40-V and 1.2-A switch FET and operates in pulse width modulation (PWM) with 1.2-MHz fixed switching frequency. For operation see Functional Block Diagram. The duty cycle of the converter is set by the error amplifier output and the current signal applied to the PWM control comparator. The control architecture is based on traditional current-mode control; therefore, slope compensation is added to the current signal to allow stable operation for duty cycles larger than 40%. The feedback loop regulates the FB pin to a low reference voltage (200 mV typical), reducing the power dissipation in the current sense resistor.

7.2 Functional Block Diagram

7.3 Feature Description

7.3.1 Soft Start-Up

Soft-start circuitry is integrated into the IC to avoid a high inrush current during start-up. After the device is enabled, the voltage at FB pin ramps up to the reference voltage in 32 steps; each step takes 213 $\mu$s. This ensures that the output voltage rises slowly to reduce the input current. Additionally, for the first 5 ms after the COMP voltage ramps, the current limit of the switch is set to half of the normal current limit specification. During this period, the input current is kept below 700 mA (typical). These two features ensure smooth start-up and minimize the inrush current. See the start-up waveform of a typical example (Figure 9).
Feature Description (continued)

7.3.2 Open LED Protection
Open LED protection circuitry prevents IC damage as the result of white LED disconnection. The TPS61165-Q1 device monitors the voltage at the SW pin and FB pin during each switching cycle. The circuitry turns off the switch FET and shuts down the IC when both of the following conditions persist for 8 switching clock cycles: (1) the SW voltage exceeds the V\text{OVP} threshold and (2) the FB voltage is less than half of regulation voltage. As a result, the output voltage falls to the level of the input supply. The device remains in shutdown mode until it is enabled by toggling the CTRL pin. The product of the number of external series LEDs and each LED’s maximum forward voltage plus the 200-mV reference voltage does not exceed the 38-V minimum OVP threshold or \((N_{\text{LEDs}} \times V_{\text{LED(MAX)}} + 200 \text{ mV} \leq 38 \text{ V})\).

7.3.3 Undervoltage Lockout
An undervoltage lockout prevents operation of the device at input voltages below 2.2 V (typical). When the input voltage is below the undervoltage threshold, the device shuts down and the internal switch FET is turned off. If the input voltage rises by undervoltage lockout hysteresis, the IC restarts.

7.3.4 Thermal Shutdown
An internal thermal shutdown turns off the device when the typical junction temperature exceeds 160°C. The device is released from shutdown automatically when the junction temperature decreases by 15°C.

7.4 Device Functional Modes

7.4.1 Shutdown
The TPS61165-Q1 enters shutdown mode when the CTRL voltage is logic low for more than 2.5 ms. During shutdown, the input supply current for the device is less than 1 \mu A (maximum). Although the internal FET does not switch in shutdown, there is still a DC current path between the input and the LEDs through the inductor and Schottky diode. The minimum forward voltage of the LED array must exceed the maximum input voltage to ensure that the LEDs remain off in shutdown.

7.5 Programming

7.5.1 Current Program
The FB voltage is regulated by a low 0.2-V reference voltage. The LED current is programmed externally using a current-sense resistor in series with the LED string. The value of the R\text{SET} is calculated using Equation 1.

\[
I_{\text{LED}} = \frac{V_{\text{FB}}}{R_{\text{SET}}}
\]

where
- \(I_{\text{LED}}\) = output current of LEDs
- \(V_{\text{FB}}\) = regulated voltage of FB
- \(R_{\text{SET}}\) = current sense resistor

The output current tolerance depends on the FB accuracy and the current sensor resistor accuracy.

7.5.2 LED Brightness Dimming Mode Selection
The CTRL pin is used for the control input for both dimming modes, PWM dimming and the 1 wire dimming. The dimming mode for the TPS61165-Q1 device is selected each time the device is enabled. The default dimming mode is PWM dimming. To enter 1-wire mode, the following digital pattern on the CTRL pin must be recognized by the IC every time the IC starts from the shutdown mode.

1. Pull CTRL pin high to enable the TPS61165-Q1 device, and to start the 1-wire detection window.
2. After the EasyScale detection delay (t\text{es\_delay}, 100 \mu s) expires, drive CTRL low for more than the EasyScale detection time (t\text{es\_detect}, 260 \mu s).
3. The CTRL pin must be low for more than EasyScale detection time before the EasyScale detection window (t\text{es\_win}, 1 ms) expires. EasyScale detection window starts from the first CTRL pin low to high transition.
Programming (continued)

The IC immediately enters the 1-wire mode once the above three conditions are met. The EasyScale
communication can start before the detection window expires. Once the dimming mode is
programmed, it cannot be changed without another start-up. This means the IC needs to be shut down
by pulling the CTRL low for 2.5 ms and restarts. See the Dimming Mode Detection and Soft Start
(see Figure 11) for a graphical explanation.

![Figure 11. Dimming Mode Detection and Soft Start PWM Brightness Dimming]

7.5.3 PWM Brightness Dimming

When the CTRL pin is constantly high, the FB voltage is regulated to 200 mV typically. However, the CTRL pin
allows a PWM signal to reduce this regulation voltage; therefore, it achieves LED brightness dimming. The
relationship between the duty cycle and FB voltage is given by Equation 2:

\[ V_{FB} = \text{Duty} \times 200 \text{ mV} \]

where
- Duty = duty cycle of the PWM signal
- 200 mV = internal reference voltage  

As shown in Figure 12, the IC chops up the internal 200-mV reference voltage at the duty cycle of the PWM
signal. The pulse signal is then filtered by an internal low pass filter. The output of the filter is connected to
the error amplifier as the reference voltage for the FB pin regulation. Therefore, although a PWM signal is used
for brightness dimming, only the WLED DC current is modulated, which is often referred as analog dimming.
This eliminates the audible noise which often occurs when the LED current is pulsed in replica of the frequency
and duty cycle of PWM control. Unlike other methods which filters the PWM signal for analog dimming, TPS61165-
Q1 device's regulation voltage is independent of the PWM logic voltage level which often has large variations.

For optimum performance, use the PWM dimming frequency in the range of 5 kHz to 100 kHz. The requirement
of minimum dimming frequency comes from the EasyScale detection delay and detection time specification in
the dimming mode selection. Because the CTRL pin is logic only pin, adding an external RC filter applied to the pin
does not work.

To use lower PWM dimming, add external RC network connected to the FB pin as shown in the additional typical
application, .
Programming (continued)

![Block Diagram of Programmable FB Voltage Using PWM Signal](image)

**Figure 12. Block Diagram of Programmable FB Voltage Using PWM Signal**

7.5.4 Digital 1 Wire Brightness Dimming

The CTRL pin features a simple digital interface to allow digital brightness control. The digital dimming can save the processor power and battery life as it does not require a PWM signal all the time, and the processor can enter idle mode if available.

The TPS61165-Q1 device adopts the EasyScale protocol for the digital dimming, which can program the FB voltage to any of the 32 steps with single command. The step increment increases with the voltage to produce pseudo logarithmic curve for the brightness step. See Table 2 for the FB pin voltage steps. The default step is full scale when the device is first enabled ($V_{FB} = 200 \text{ mV}$). The programmed reference voltage is stored in an internal register and will not be changed by pulling CTRL low for 2.5 ms and then re-enabling the IC by taking CTRL high. A power reset clears the register value and reset it to default.

7.5.5 EasyScale: 1 Wire Digital Dimming

EasyScale is a simple but flexible 1-pin interface to configure the FB voltage. The interface is based on a master-slave structure, where the master is typically a microcontroller or application processor. Figure 13 and Table 3 give an overview of the protocol. The protocol consists of a device specific address byte and a data byte. The device specific address byte is fixed to 72 hex. The data byte consists of 5 bits for information, 2 address bits, and the RFA bit. The RFA bit set to high indicates the **Request for Acknowledge** condition. The Acknowledge condition is applied only if the protocol was received correctly. The advantage of EasyScale compared with other 1-pin interfaces is that its bit detection is in a large extent independent from the bit transmission rate. It can automatically detect bit rates between 1.7 kbps and up to 160 kbps.

<table>
<thead>
<tr>
<th>FB voltage (mV)</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>5</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>8</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>11</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>14</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>17</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>6</td>
<td>20</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>7</td>
<td>23</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>8</td>
<td>26</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>9</td>
<td>29</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>10</td>
<td>32</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>11</td>
<td>35</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>12</td>
<td>38</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
Table 2. Selectable FB Voltage (continued)

<table>
<thead>
<tr>
<th>FB voltage (mV)</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>13</td>
<td>44</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>14</td>
<td>50</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>15</td>
<td>56</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>16</td>
<td>62</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>17</td>
<td>68</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>18</td>
<td>74</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>19</td>
<td>80</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>20</td>
<td>86</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>21</td>
<td>92</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>22</td>
<td>98</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>23</td>
<td>104</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>24</td>
<td>116</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>25</td>
<td>128</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>26</td>
<td>140</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>27</td>
<td>152</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>28</td>
<td>164</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>29</td>
<td>176</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>30</td>
<td>188</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>31</td>
<td>200</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 3. EasyScale Bit Description

<table>
<thead>
<tr>
<th>BYTE NUMBER</th>
<th>NAME</th>
<th>TRANSMISSION DIRECTION</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device Address Byte</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>DA7</td>
<td>IN</td>
<td>0 MSB device address</td>
</tr>
<tr>
<td>6</td>
<td>DA6</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>5</td>
<td>DA5</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>4</td>
<td>DA4</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>DA3</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>DA2</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>DA1</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>DA0</td>
<td></td>
<td>0 LSB device address</td>
</tr>
</tbody>
</table>
Table 3. EasyScale Bit Description (continued)

<table>
<thead>
<tr>
<th>BYTE</th>
<th>BIT NUMBER</th>
<th>NAME</th>
<th>TRANSMISSION DIRECTION</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data byte</td>
<td>7 (MSB)</td>
<td>RFA</td>
<td>IN</td>
<td>Request for acknowledge. If high, acknowledge is applied by device</td>
</tr>
<tr>
<td></td>
<td>6</td>
<td>A1</td>
<td></td>
<td>0 Address bit 1</td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>A0</td>
<td></td>
<td>0 Address bit 0</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>D4</td>
<td></td>
<td>Data bit 4</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>D3</td>
<td></td>
<td>Data bit 3</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>D2</td>
<td></td>
<td>Data bit 2</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>D1</td>
<td></td>
<td>Data bit 1</td>
</tr>
<tr>
<td></td>
<td>0 (LSB)</td>
<td>D0</td>
<td></td>
<td>Data bit 0</td>
</tr>
<tr>
<td>ACK</td>
<td></td>
<td></td>
<td>OUT</td>
<td>Acknowledge condition active 0, this condition will only be applied in case RFA bit is set. Open-drain output, Line needs to be pulled high by the host with a pullup resistor. This feature can only be used if the master has an open-drain output stage. In case of a push-pull output stage Acknowledge condition may not be requested!</td>
</tr>
</tbody>
</table>

EasyScale Timing, without acknowledge RFA = 0

EasyScale Timing, with acknowledge RFA = 1

Figure 14. EasyScale—Bit Coding

All bits are transmitted MSB first and LSB last. Figure 14 shows the protocol without acknowledge request (Bit RFA = 0), Figure 14 with acknowledge (Bit RFA = 1) request. Before both bytes, device address byte and data byte, a start condition must be applied. For this, the CTRL pin must be pulled high for at least $t_{\text{start}}$ (2 $\mu$s) before the bit transmission starts with the falling edge. If the CTRL pin is already at a high level, no start condition is needed before the device address byte. The transmission of each byte is closed with an End of Stream condition for at least $t_{\text{EOS}}$ (2 $\mu$s).
The bit detection is based on a Logic Detection scheme, where the criterion is the relation between \( t_{\text{LOW}} \) and \( t_{\text{HIGH}} \). It can be simplified to:

- **High Bit:** \( t_{\text{HIGH}} > t_{\text{LOW}} \), but with \( t_{\text{HIGH}} \) at least 2x \( t_{\text{LOW}} \), see Figure 14.
- **Low Bit:** \( t_{\text{HIGH}} < t_{\text{LOW}} \), but with \( t_{\text{LOW}} \) at least 2x \( t_{\text{HIGH}} \), see Figure 14.

The bit detection starts with a falling edge on the CTRL pin and ends with the next falling edge. Depending on the relation between \( t_{\text{HIGH}} \) and \( t_{\text{LOW}} \), the logic 0 or 1 is detected.

The acknowledge condition is only applied if:

- Acknowledge is requested by a set RFA bit.
- The transmitted device address matches with the device address of the device.
- 16 bits is received correctly.

If the device turns on the internal ACKN-MOSFET and pulls the CTRL pin low for the time \( t_{\text{ACKN}} \), which is 512 µs maximum then the Acknowledge condition is valid after an internal delay time \( t_{\text{valACK}} \). This means that the internal ACKN-MOSFET is turned on after \( t_{\text{valACK}} \), when the last falling edge of the protocol was detected. The master controller keeps the line low in this period. The master device can detect the acknowledge condition with its input by releasing the CTRL pin after \( t_{\text{valACK}} \) and read back a logic 0. The CTRL pin can be used again after the acknowledge condition ends.

The acknowledge condition may only be requested if the master device has an open-drain output. For a push-pull output stage, the use a series resistor in the CRTL line to limit the current to 500 µA is recommended to for such cases as:

- Accidentally requested acknowledge.
- Protect the internal ACKN-MOSFET.
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information
The TPS61165-Q1 device drives 6 high-brightness LEDs; the LED current is set at 350 mA. A 12-V Zener diode is used to clamp the input voltage, which makes the TPS61165-Q1 device suitable for car battery supply applications.

8.2 Typical Application

For assistance in selecting the proper values, the detailed external PWM dimming network for the specific application, see SLVA471 and/or SLVC366.

8.2.1 Design Requirements
Table 4 lists the input parameters for this design example.

<table>
<thead>
<tr>
<th>DESIGN PARAMETER</th>
<th>EXAMPLE VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Brightness control</td>
<td>PWM Dimming</td>
</tr>
<tr>
<td>Input voltage</td>
<td>12 V</td>
</tr>
<tr>
<td>Output current</td>
<td>350 mA</td>
</tr>
<tr>
<td>LED loads</td>
<td>6 LEDs</td>
</tr>
</tbody>
</table>
8.2.2 Detailed Design Procedures

8.2.2.1 Maximum Output Current

The overcurrent limit in a boost converter limits the maximum input current and thus maximum input power for a given input voltage. Maximum output power is less than maximum input power due to power conversion losses. Therefore, the current limit setting, input voltage, output voltage and efficiency can all change maximum current output. The current limit clamps the peak inductor current; therefore, the ripple must be subtracted to derive maximum DC current. The ripple current is a function of switching frequency, inductor value and duty cycle. Use Equation 3 and Equation 4 consider of all the above factors for maximum output current calculation.

\[
I_p = \frac{1}{L \times F_s \times \left(\frac{1}{V_{out} + V_f - V_i} + \frac{1}{V_i}\right)}
\]

where
- \(I_p\) = inductor peak to peak ripple
- \(L\) = inductor value
- \(V_f\) = Schottky diode forward voltage
- \(F_s\) = switching frequency
- \(V_{out}\) = output voltage of the boost converter. It is equal to the sum of VFB and the voltage drop across LEDs.

\[
I_{out_{-max}} = \frac{V_{in} \times (I_{lim} - I_p/2) \times \eta}{V_{out}}
\]

where
- \(I_{out_{-max}}\) = Maximum output current of the boost converter
- \(I_{lim}\) = over current limit
- \(\eta\) = efficiency

For instance, when \(V_{IN}\) is 3 V, 8 LEDs output equivalent to \(V_{OUT}\) of 26 V, the inductor is 22 \(\mu\)H, the Schottky forward voltage is 0.2 V; and then the maximum output current is 110 mA in typical condition. When \(V_{IN}\) is 5 V, 10 LEDs output equivalent to \(V_{OUT}\) of 32 V, the inductor is 22 \(\mu\)H, the Schottky forward voltage is 0.2 V; and then the maximum output current is 150 mA in typical condition.

8.2.2.2 Inductor Selection

The selection of the inductor affects steady state operation as well as transient behavior and loop stability. These factors make it the most important component in power regulator design. There are three important inductor specifications, inductor value, DC resistance and saturation current. Considering inductor value alone is not enough.

The inductor value determines the inductor ripple current. Choose an inductor that can handle the necessary peak current without saturating, according to half of the peak-to-peak ripple current given by Equation 3, pause the inductor DC current given by:

\[
I_{in_{-DC}} = \frac{V_{out} \times I_{out}}{V_{in} \times \eta}
\]

Inductor values can have \(\pm\)20% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the 0 A value depending on how the inductor vendor defines saturation current. Using an inductor with a smaller inductance value forces discontinuous PWM when the inductor current ramps down to zero before the end of each switching cycle. This reduces the boost converter’s maximum output current, causes large input voltage ripple and reduces efficiency. Large inductance value provides much more output current and higher conversion efficiency. For these reasons, a 10 \(\mu\)H to 22 \(\mu\)H inductor value range is recommended. A 22 \(\mu\)H inductor optimized the efficiency for most application while maintaining low inductor peak to peak ripple. Table 5 lists the recommended inductor for the TPS61165-Q1 device. When recommending inductor value, the factory has considered –40% and +20% tolerance from its nominal value.
TPS61165-Q1 device has built-in slope compensation to avoid subharmonic oscillation associated with current mode control. If the inductor value is lower than 10 μH, the slope compensation may not be adequate, and the loop can be unstable. Therefore, customers need to verify the inductor in their application if it is different from the recommended values.

### Table 5. Recommended Inductors for TPS61165-Q1

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>L  (μH)</th>
<th>DCR MAX (mΩ)</th>
<th>SATURATION CURRENT (A)</th>
<th>SIZE (L x W x H mm)</th>
<th>VENDOR</th>
</tr>
</thead>
<tbody>
<tr>
<td>A915_Y-100M</td>
<td>10</td>
<td>90</td>
<td>1.3</td>
<td>5.2 x 5.2 x 3</td>
<td>TOKO</td>
</tr>
<tr>
<td>VLCF5020T-100M1R1-1</td>
<td>10</td>
<td>237</td>
<td>1.1</td>
<td>5 x 5 x 2</td>
<td>TDK</td>
</tr>
<tr>
<td>CDRH4D22/HP</td>
<td>10</td>
<td>144</td>
<td>1.2</td>
<td>5 x 5 x 2.4</td>
<td>Sumida</td>
</tr>
<tr>
<td>LQH43PN100MR0</td>
<td>10</td>
<td>247</td>
<td>0.84</td>
<td>4.5 x 3.2 x 2</td>
<td>Murata</td>
</tr>
</tbody>
</table>

### 8.2.2.3 Schottky Diode Selection

The high switching frequency of the TPS61165-Q1 device demands a high-speed rectification for optimum efficiency. Ensure that the diode’s average and peak current rating exceeds the average output current and peak inductor current. In addition, the reverse breakdown voltage of the diode must exceed the open LED protection voltage. The ONsemi MBR0540 and the ZETEX ZHCS400 are recommended for the TPS61165-Q1 device.

### 8.2.2.4 Compensation Capacitor Selection

The compensation capacitor C3 (see Functional Block Diagram), connected from COMP pin to GND, is used to stabilize the feedback loop of the TPS61165-Q1 device. A 220-nF ceramic capacitor is suitable for most applications.

### 8.2.2.5 Input and Output Capacitor Selection

The output capacitor is mainly selected to meet the requirements for the output ripple and loop stability. This ripple voltage is related to the capacitance of the capacitor and its equivalent series resistance (ESR). Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated using Equation 6.

$$C_{out} = \frac{(V_{out} - V_{in})I_{out}}{V_{out} \times F_s \times V_{ripple}}$$

where
- $V_{ripple}$ = peak-to-peak output ripple

The additional output ripple component caused by ESR is calculated using Equation 7

$$V_{ripple_{ESR}} = I_{out} \times R_{ESR}$$

Due to its low ESR, $V_{ripple_{ESR}}$ can be neglected for ceramic capacitors, but must be considered if tantalum or electrolytic capacitors are used.

Care must be taken when evaluating a ceramic capacitors derating under DC bias, aging and AC signal. For example, larger form factor capacitors (in 1206 size) have a self resonant frequencies in the range of the switching frequency. So the effective capacitance is significantly lower. The DC bias can also significantly reduce capacitance. Ceramic capacitors can loss as much as 50% of its capacitance at its rated voltage. Therefore, leave the margin on the voltage rating to ensure adequate capacitance at the required output voltage.

The capacitor in the range of 1 μF to 4.7 μF is recommended for input side. The output requires a capacitor in the range of 1 μF to 10 μF. The output capacitor affects the loop stability of the boost regulator. If the output capacitor is below the range, the boost regulator can potentially become unstable.

The popular vendors for high value ceramic capacitors are:
- TDK (http://www.component.tdk.com/components.php)
- Murata (http://www.murata.com/cap/index.html)
8.2.3 Application Curves

Figure 16. Start-Up Waveform

Figure 17. 100 kHz PWM Dimming Waveform Under 50% Duty Cycle

8.3 Do’s and Don’ts

There is a known issue with the TPS61165-Q1 device when using the EasyScale interface to increase the feedback voltage. When VFB is increased from 0 mV to any value more than 0 mV, some ICs do not properly soft-start during this transition and the voltage on their SW pin overshoots. If the overshoot exceeds the absolute maximum voltage rating on the SW pin, the IC is damaged.

With VFB set below 10 mV through EasyScale, the parasitic offsets on the input pins of the internal transconductance amplifier determine the value of output of the amplifier. IC process variations are causing the offset to be larger and in the opposite polarity than expected. If the amplifier’s output is already high before a transition from VFB = 0 mV to any other voltage, then the modulator turns on full, bypassing soft start, and causes the SW pin and output voltage to overshoot.

To avoid this issue do not use EasyScale to change the feedback voltage from 0 mV, effectively disabling the device, to any other voltage. One alternative is to start with VFB = 10 mV and go to a higher voltage. Another alternative is to disable the IC by taking the CTRL pin low for 2.5 ms and then re-enter EasyScale to force a soft start from VFB = 0 mV to the default 200 mV.

9 Power Supply Recommendations

The TPS61165-Q1 device requires a single supply input voltage. This voltage can range from 3 V to 18 V and be able to supply enough current for a given application.

10 Layout

10.1 Layout Guidelines

As for all switching power supplies, especially those high frequency and high current ones, layout is an important design step. If layout is not carefully done, the regulator could suffer from instability as well as noise problems. To reduce switching losses, the SW pin rise and fall times are made as short as possible. To prevent radiation of high frequency resonance problems, proper layout of the high frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin and always use a ground plane under the switching regulator to minimize inter-plane coupling. The loop including the PWM switch, Schottky diode, and output capacitor, contains high current rising and falling in nanosecond and should be kept as short as possible. The input capacitor needs not only to be close to the VIN pin, but also to the GND pin to reduce the IC supply ripple.
10.2 Layout Example

![Recommended Layout Example](image)

**Figure 18. Recommended Layout Example**

10.3 Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation of the TPS61165-Q1 device. Calculate the maximum allowable dissipation, $P_{D(\text{max})}$, and keep the actual dissipation less than or equal to $P_{D(\text{max})}$. The maximum-power-dissipation limit is determined using Equation 8:

$$P_{D(\text{max})} = \frac{125^\circ\text{C} - T_A}{R_{\text{JA}}},$$

where

- $T_A$ is the maximum ambient temperature for the application
- $R_{\text{JA}}$ is the thermal resistance junction-to-ambient given in Thermal Information Table

Equation 8
11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer
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11.2 Documentation Support

11.2.1 Related Documentation
For related documentation see the following:
• How to Use Analog Dimming With the TPS6116x, SLVA471
• Design Tool for Analog Dimming using a PWM Signal, SLVC366

11.3 Community Resource
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI’s Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support TI’s Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks
EasyScale, E2E are trademarks of Texas Instruments. All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — TI Glossary.
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS61165TDBVRQ1</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>6</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 105</td>
<td>SBM</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS61165-Q1:
- Catalog: TPS61165

NOTE: Qualified Version Definitions:
  - Catalog - TI's standard catalog product
TAPE AND REEL INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS61165TDBVRQ1</td>
<td>SOT-23</td>
<td>DBV</td>
<td>6</td>
<td>3000</td>
<td>179.0</td>
<td>8.4</td>
<td>3.2</td>
<td>3.2</td>
<td>1.4</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

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Pack Materials-Page 1
TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS61165TDBVRQ1</td>
<td>SOT-23</td>
<td>DBV</td>
<td>6</td>
<td>3000</td>
<td>203.0</td>
<td>203.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

2. This drawing is subject to change without notice.

3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.

4. Leads 1, 2, 3 may be wider than leads 4, 5, 6 for package orientation.

5. Refernce JEDEC MO-178.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
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