

TPS27081A 1.2-V to 8-V, 3-A PFET High-Side Load Switch With Level Shift and Adjustable Slew Rate Control

1 Features

- Low ON-Resistance, High-Current PFET
 - $R_{DS(on)} = 32\text{ m}\Omega$ at $V_{GS} = -4.5\text{ V}$
 - $R_{DS(on)} = 44\text{ m}\Omega$ at $V_{GS} = -3\text{ V}$
 - $R_{DS(on)} = 82\text{ m}\Omega$ at $V_{GS} = -1.8\text{ V}$
 - $R_{DS(on)} = 93\text{ m}\Omega$ at $V_{GS} = -1.5\text{ V}$
 - $R_{DS(on)} = 155\text{ m}\Omega$ at $V_{GS} = -1.2\text{ V}$
- Adjustable Turnon and Turnoff Slew Rate Control Through External R1, R2, and C1
- Supports a Wide Range of 1.2-V to 8-V Supply Inputs
- Integrated NMOS for PFET Control
- NMOS ON/OFF Supports a Wide Range of 1-V to 8-V Control Logic Interface
- Full ESD Protection (All Pins)
 - HBM 2 kV, CDM 500 V
- Ultra-Low Leakage Current in Standby (Typical 100 nA)
- Available in Tiny 6-Pin Package
 - 2.9 mm × 2.8 mm × 0.75 mm SOT (DDC)

2 Applications

- High-Side Load Switches
- Inrush Current Control
- Power Sequencing and Control
- Standby Power Isolation
- Portable Power Switches

3 Description

The TPS27081A device is a high-side load switch that integrates a Power PFET and a Control NFET in a tiny package.

The TPS27081A features industry-standard ESD protection on all pins providing better ESD compatibility with other onboard components.

The TPS27081A level shifts ON/OFF logic signal to VIN levels and supports as low as 1-V CPU or MCU logic to control higher voltage power supplies without requiring an external level-shifter.

Switching a large value output capacitor CL through a fast ON/OFF logic signal may result in an excessive inrush current. To control the load inrush current, connect a resistor R2 and add an external capacitor C1 as shown in the [Simplified Schematic](#). To configure the TPS27081A to achieve a specific slew rate, refer to the [Application and Implementation](#) section.

A single pullup resistor R1 is required in standby power switch applications. In such applications connect the R2 pin of the TPS27081A to the system ground when inrush current control is not required.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS27081A	SOT (6)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

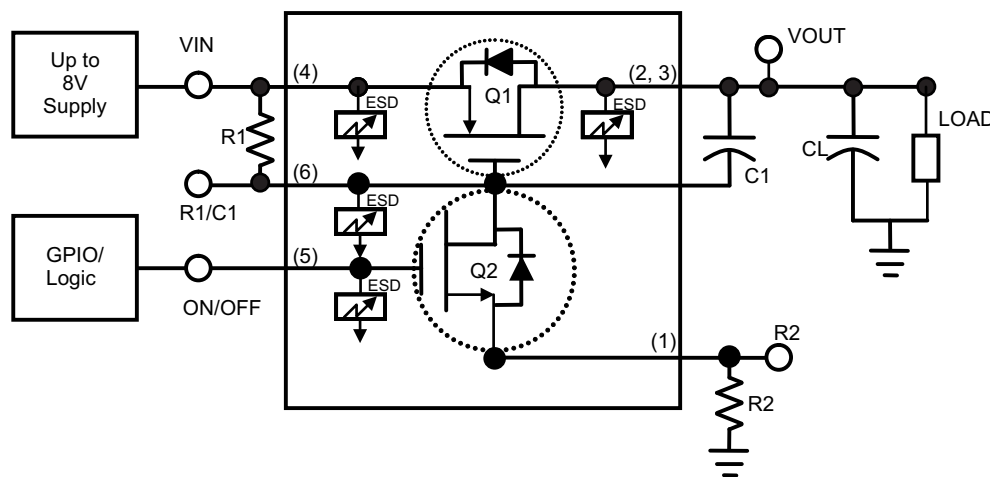


Table of Contents

1 Features	1	8 Application and Implementation	10
2 Applications	1	8.1 Application Information.....	10
3 Description	1	8.2 Typical Application	10
4 Revision History	2	8.3 System Examples	14
5 Pin Configuration and Functions	3	9 Power Supply Recommendations	17
6 Specifications	3	10 Layout	17
6.1 Absolute Maximum Ratings	3	10.1 Layout Guidelines	17
6.2 ESD Ratings.....	4	10.2 Layout Example	17
6.3 Recommended Operating Conditions.....	4	10.3 Thermal Reliability.....	18
6.4 Thermal Information	4	10.4 Improving Package Thermal Performance	18
6.5 Electrical Characteristics.....	5	11 Device and Documentation Support	19
6.6 Typical Characteristics.....	6	11.1 Community Resources.....	19
7 Detailed Description	9	11.2 Trademarks	19
7.1 Overview	9	11.3 Electrostatic Discharge Caution.....	19
7.2 Functional Block Diagram	9	11.4 Glossary	19
7.3 Feature Description.....	9	12 Mechanical, Packaging, and Orderable Information	19
7.4 Device Functional Modes.....	9		

4 Revision History

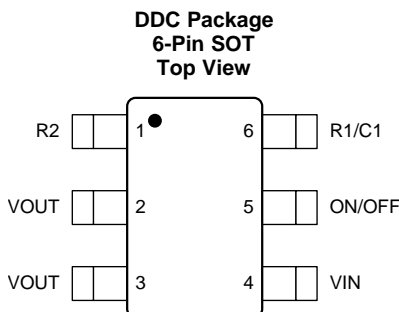
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (April 2013) to Revision E	Page
<ul style="list-style-type: none"> Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section 	1

Changes from Revision C (January 2013) to Revision D	Page
<ul style="list-style-type: none"> Updated wording in document..... 	1

Changes from Revision B (September 2012) to Revision C	Page
<ul style="list-style-type: none"> Removed DRV package preview from datasheet. 	1

5 Pin Configuration and Functions



Pin Functions

PIN		I/O ⁽¹⁾	DESCRIPTION
NAME	NO.		
ON/OFF	5	I	Active high enable. When driven with a high-impedance driver, connect an external pull down resistor to GND
R1/C1	6	I	Gate terminal of power PFET (Q1)
R2	1	O	Source terminal of NMOS (Q2) . Connect to system GND directly or through a slew rate control resistor
VIN	4	I	Source terminal of power PFET (Q1). Connect a pull-up resistor between the pins VIN/R1 and R1/C1
VOUT	2 3	O	Drain terminal of power PFET (Q1). Connect a slew control capacitor between pins VOUT and R1/C1

(1) I = Input, O = Output

6 Specifications

6.1 Absolute Maximum Ratings

Specified at $T_J = -40^{\circ}\text{C}$ to 105°C unless otherwise noted.⁽¹⁾⁽²⁾

		MIN	MAX	UNIT
$V_{IN(max)}$	VIN pin maximum voltage with reference to pin R2	-0.1	8	V
$V_{OUT(max)}$	VOUT pin maximum voltage with reference to pin R2	-0.1	8	V
$V_{ON/OFF}$	ON/OFF in maximum voltage with respect to pin R2	-0.3	8	V
$I_{Q1(on)}$	Maximum continuous drain current of Q1 at $T_J = 105^{\circ}\text{C}$		3	A
	Maximum pulsed drain current of Q1 ⁽³⁾ at $T_J = 105^{\circ}\text{C}$		9.5	
P_D	Maximum power dissipation at $T_A = 25^{\circ}\text{C}$, $T_J = 150^{\circ}\text{C}$, $R_{\theta JA} = 105^{\circ}\text{C/W}$		1190	mW
T_A	Operating free-air ambient temperature	-40	85 ⁽⁴⁾	$^{\circ}\text{C}$
$T_{J(max)}$ ⁽⁵⁾	Operating virtual junction temperature		150	$^{\circ}\text{C}$
T_{stg}	Storage temperature	-65	150	$^{\circ}\text{C}$

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Refer to TI's design support web page at www.ti.com/thermal for improving device thermal performance.
- (3) Pulse width <300 μs , duty cycle < 2%
- (4) $T_{J(max)}$ limits and other related conditions apply. Refer to SOA charts, [Figure 8](#) through [Figure 12](#).
- (5) Operating at the absolute $T_{J(max)} = 150^{\circ}\text{C}$ can affect reliability. For higher reliability, TI recommends maintaining $T_J < 105^{\circ}\text{C}$.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±500

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	1		8	V
T_A	Operating free-air ambient temperature	–40		85	°C
T_J	Junction temperature	–40		105	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS27081A	UNIT
		DDC (SOT)	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	105	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	6.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	16.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

Specified over the recommended junction temperature range $T_J = -40^{\circ}\text{C}$ to 105°C unless otherwise noted. Typical values specified at $T_A = T_J = 25^{\circ}\text{C}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF-TIME CHARACTERISTICS						
BV_{IN1}	Q1 drain-to-source breakdown voltage	$V_{ON/OFF} = 0\text{ V}$, $V_{GS(Q1)} = 0\text{ V}$, $I_{D(Q1)} = 250\ \mu\text{A}$	-8			V
$I_{LOAD}^{(1)}$	VIN pin total leakage current	$V_{IN} = 8\text{ V}$, $V_{ON/OFF} = 0\text{ V}$, $R_{R1} = 10\text{ k}\Omega$	$T_J = 25^{\circ}\text{C}$	0.15	0.75	μA
			$T_J = 85^{\circ}\text{C}^{(2)}$	5	20	
		$V_{IN} = 5\text{ V}$, $V_{ON/OFF} = 0\text{ V}$, $R_{R1} = 10\text{ k}\Omega$	$T_J = 25^{\circ}\text{C}$	0.05		
			$T_J = 85^{\circ}\text{C}^{(2)}$	2		
I_{FQ2}	Q2 drain-to-source leakage current	$V_{IN} = 8\text{ V}$, $V_{ON/OFF} = 0\text{ V}$	$T_J = 25^{\circ}\text{C}$	0.03	0.05	μA
			$T_J = 85^{\circ}\text{C}^{(2)}$	0.35	0.6	
		$V_{IN} = 5\text{ V}$, $V_{ON/OFF} = 0\text{ V}$	$T_J = 25^{\circ}\text{C}$	0.025		μA
			$T_J = 85^{\circ}\text{C}^{(2)}$	0.25		
ON-TIME CHARACTERISTICS⁽³⁾						
V_{IL}	ON/OFF pin low-level input voltage	$V_{IN} = 5\text{ V}$, $I_{D(Q1)} < 2\ \mu\text{A}$, $R_{R1} = 10\text{ k}\Omega$, $R_{R2} = R_L = 0\ \Omega$	$T_J = 25^{\circ}\text{C}$		0.3	V
		$V_{IN} = 5\text{ V}$, $I_{D(Q1)} < 20\ \mu\text{A}$, $R_{R1} = 10\text{ k}\Omega$, $R_{R2} = R_L = 0\ \Omega$	$T_J = 85^{\circ}\text{C}^{(2)}$		0.2	
V_{IH}	ON/OFF pin high-level input voltage	$V_{IN} = 5\text{ V}$, $R_{R1} = 10\text{ k}\Omega$	1			V
$R_{Q1(on)}$	Q1 Channel ON-resistance ⁽⁴⁾	$V_{GS} = -4.5\text{ V}$, $I_{D(Q1)} = 3\text{ A}$		32	55	m Ω
		$V_{GS} = -3\text{ V}$, $I_{D(Q1)} = 2.5\text{ A}$		44	77	
		$V_{GS} = -2.5\text{ V}$, $I_{D(Q1)} = 2.5\text{ A}$		50	85	
		$V_{GS} = -1.8\text{ V}$, $I_{D(Q1)} = 2\text{ A}$		82	147	
		$V_{GS} = -1.5\text{ V}$, $I_{D(Q1)} = 1\text{ A}$		93	166	
		$V_{GS} = -1.2\text{ V}$, $I_{D(Q1)} = 0.5\text{ A}$		155	260	
$R_{Q2(on)}$	Q2 Channel ON-resistance	$V_{GS} = 4.5\text{ V}$, $I_{D(Q2)} = 0.4\text{ A}$		1.8	3	Ω
		$V_{GS} = 3.0\text{ V}$, $I_{D(Q2)} = 0.3\text{ A}$		2.3	6.2	
		$V_{GS} = 2.5\text{ V}$, $I_{D(Q2)} = 0.2\text{ A}$		2.6	6.1	
		$V_{GS} = 1.8\text{ V}$, $I_{D(Q2)} = 0.1\text{ A}$		3.8	10	
		$V_{GS} = 1.5\text{ V}$, $I_{D(Q2)} = 0.05\text{ A}$		4.4	8.5	
		$V_{GS} = 1.2\text{ V}$, $I_{D(Q2)} = 0.03\text{ A}$		6.25	13.5	
Q1 DRAIN-SOURCE DIODE PARAMETERS⁽³⁾⁽⁵⁾						
I_{FSD}	Source-drain diode peak forward current	$V_{FSD} = 0.8\text{ V}$, $V_{ON/OFF} = 0\text{ V}$		1		A
V_{FSD}	Source-drain diode forward voltage	$V_{ON/OFF} = 0\text{ V}$, $I_{FSD} = -0.6\text{ A}$			1	V

(1) Pullup resistor (R_{R1}) dependent.

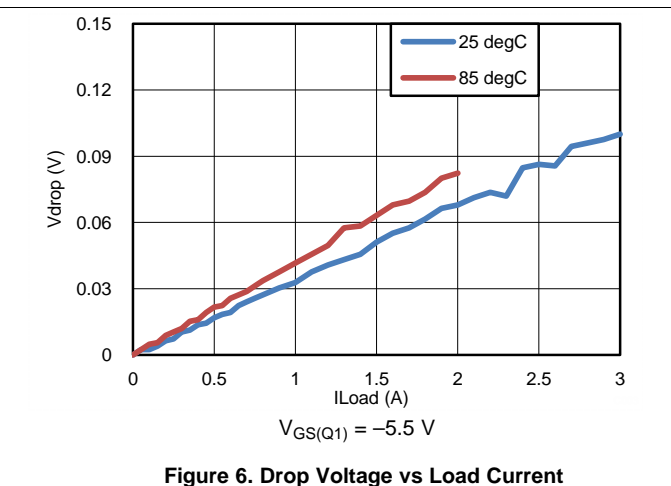
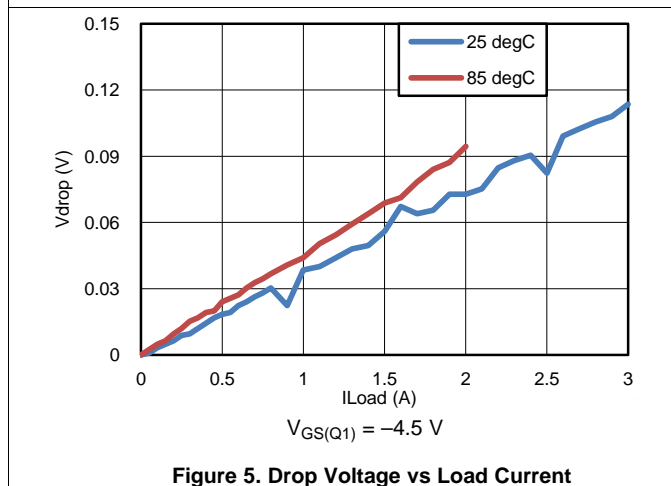
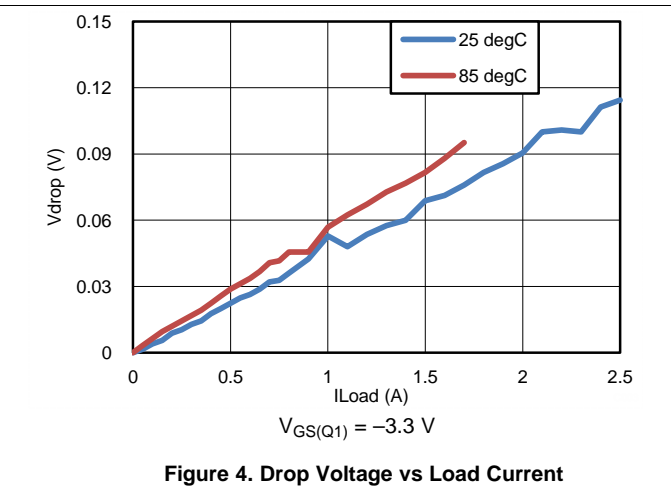
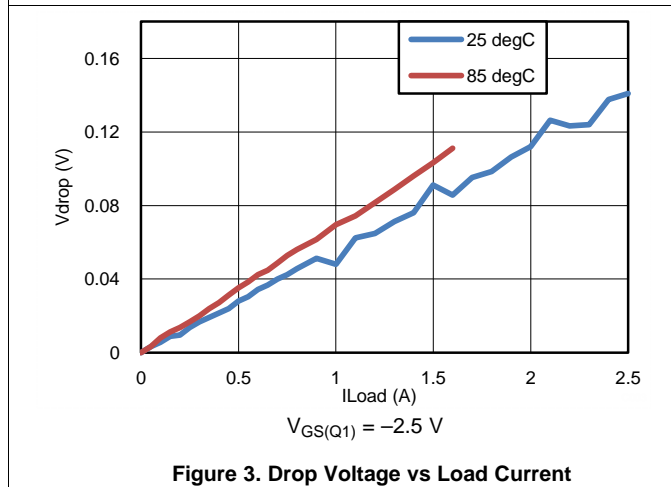
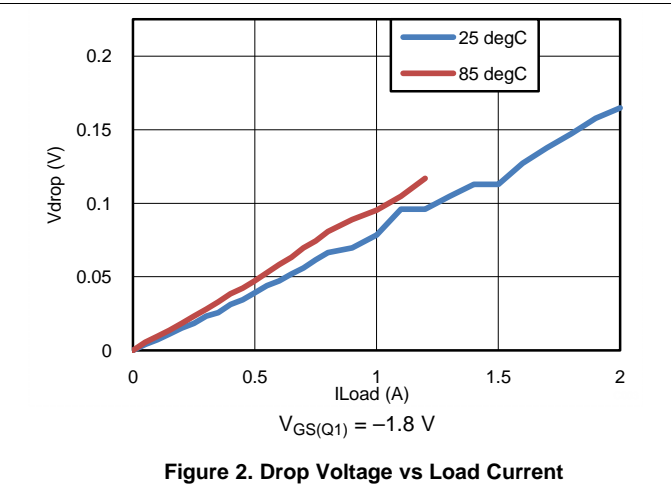
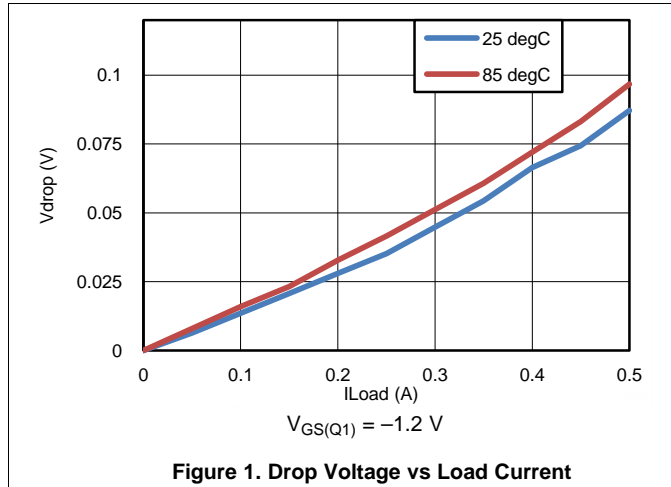
(2) Specified by design. Not production tested.

(3) Pulse width $< 300\ \mu\text{s}$, duty cycle $< 2.0\%$

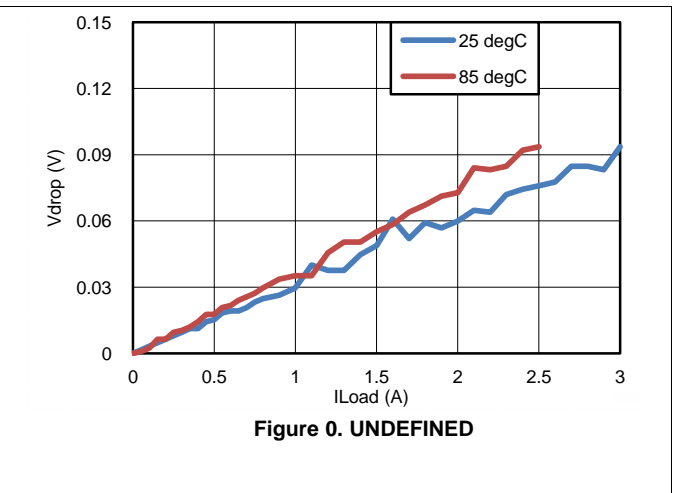
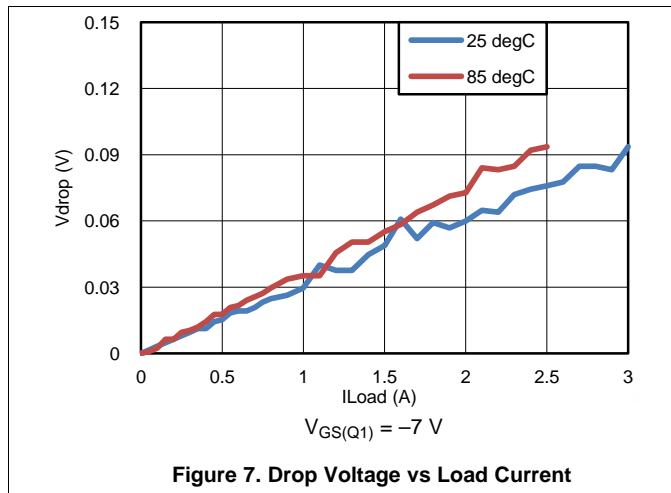
(4) Refer to [PFET Q1 Minimum Safe Operating Area \(SOA\)](#) section for current rating.

(5) Not rated for continuous current operation.

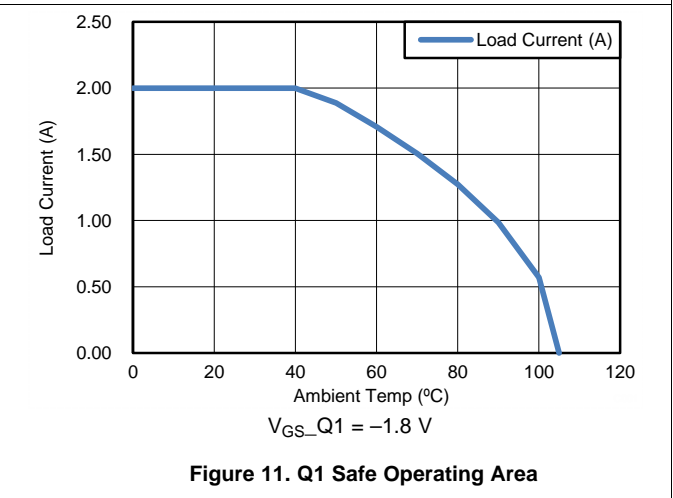
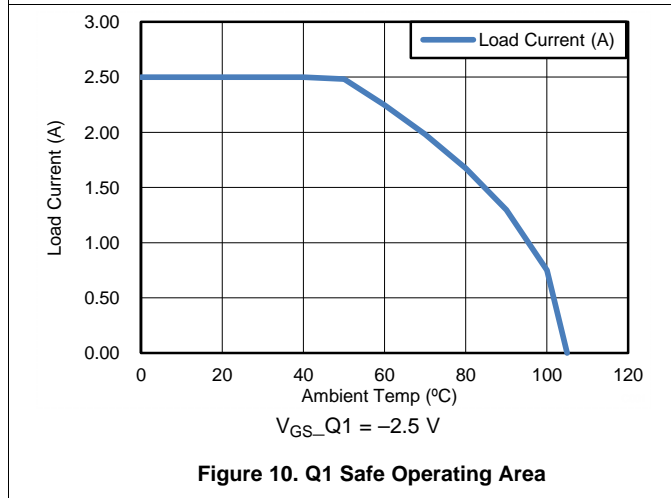
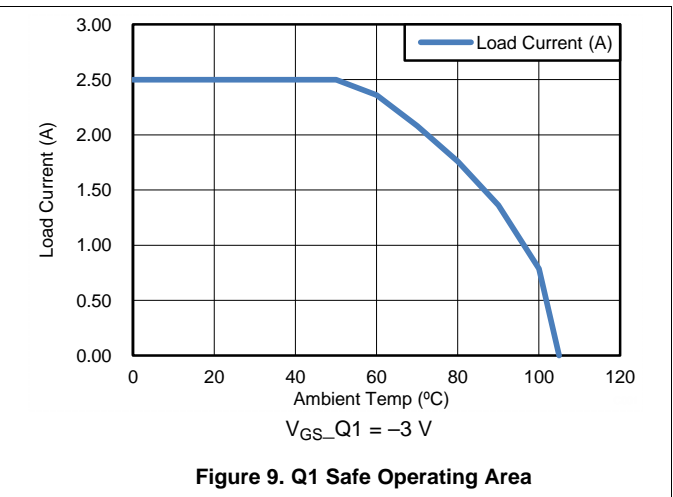
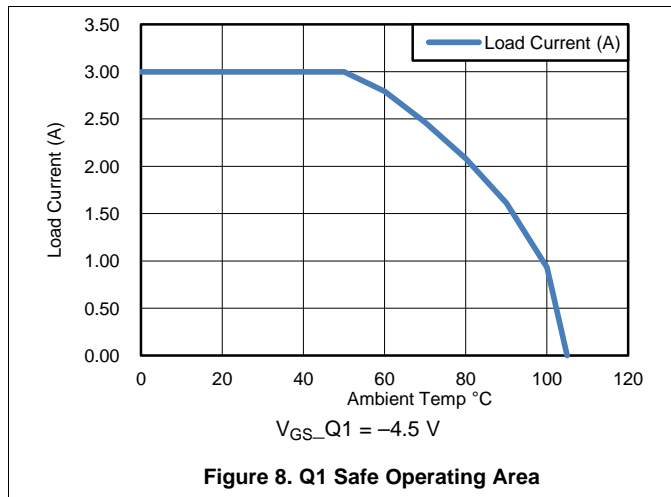
6.6 Typical Characteristics



Typical Characteristics (continued)



6.6.1 PFET Q1 Minimum Safe Operating Area (SOA)



PFET Q1 Minimum Safe Operating Area (SOA) (continued)

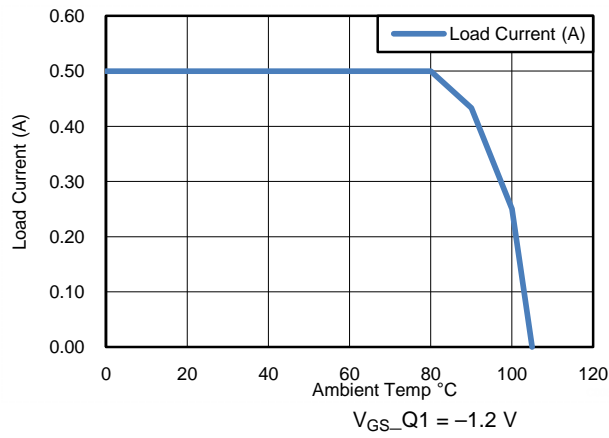


Figure 12. Q1 Safe Operating Area

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications.

8.2 Typical Application

8.2.1 Standard Load Switching Application

The TPS27081A device is a high-side load switch that integrates a power PFET and a control NMOS in a tiny package. The device internal components are rated for up to 8-V supply and support up to 3 A of load current. The device can be used in a variety applications. Figure 13 shows a general application of the TPS27081A device to control the load inrush current.

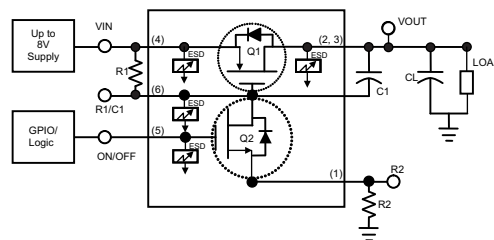


Figure 13. Standard Application Diagram

8.2.1.1 Design Requirements

Table 1. Component Table

COMPONENT	DESCRIPTION
R1	Level shift and pullup resistor
R2	Optional ⁽¹⁾
C1	Optional ⁽¹⁾

(1) Required for load inrush current (slew rate) control.

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Configuring Q1 ON Resistance

The $V_{GS(Q1)}$ gate-to-source voltage across the PMOS transistor Q1 sets its ON-resistance $R_{Q1(on)}$. Directly connecting the pin R2 to ground maximizes the ON state $V_{GS(Q1)}$ and thus minimizes the VIN to VOUT voltage dropout. Equation 1 describes the $V_{GS(Q1)}$ when a resistor R2 is installed to control the turnon slew rate.

$$V_{GS(Q1)} = -V_{VIN} \times \frac{R_{R1}}{(R_{R1} + R_{R2})} \quad (V)$$

(1)

For example, when $R_{R1} = 10 \times R_{R2}$ and $V_{VIN} = 5\text{ V}$, $V_{GS(Q1)} = -4.5\text{ V}$

NOTE

TI recommends maintaining $R_{R1} > 10 \times R_{R2}$. The higher value of resistor R1 minimizes quiescent current when PMOS is on, however, the higher value may adversely impact OFF-state leakage current. Refer to the load current (I_{LOAD}) specifications in the [Electrical Characteristics](#) table.

8.2.1.2.2 Configuring Turnon Slew Rate

Switching a large capacitive load C_{LOAD} instantaneously results in a load inrush current given by [Equation 2](#).

$$I_{INRUSH} = C_{LOAD} \times \frac{dv}{dt} = C_{LOAD} \times \frac{V_{OUT(final)} - V_{OUT(initial)}}{V_{OUT(SR)}}$$

where

- $V_{OUT(SR)}$ is the output voltage slew rate (2)

An uncontrolled fast rising ON/OFF logic input may result in a high slew rate at the output resulting in a very high dv/dt , thus, leading to a higher inrush current. To control the inrush current, connect a resistor R2 and a capacitor C1 as shown in [Figure 13](#). Use the following equation to configure the TPS27081A slew rate to a specific value. Refer to [Table 2](#) for component values to configure TPS27081A to achieve standard slew rates.

$$t_{RISE} = \frac{3.9 \times R_{R2} \times C_{C1}}{(V_{VIN})^{2/3}} \text{ (s)}$$

where

- t_{RISE} is the time delta starting from the rising edge of the ON/OFF signal to charge up the load capacitor C_{LOAD} from 10% to 90% of V_{IN} voltage. (3)

NOTE

[Equation 3](#) is accurate to within $\pm 20\%$ across full V_{IN} range supported by TPS27081A. Ensure that $R1 > 10 \times R2$.

Table 2. Component Values for VOUT Rise Time

C_{C1}	RISE TIME (μs) ⁽¹⁾⁽²⁾							
	$R_{R1} = 10 \text{ k}\Omega, R_{R2} = 1 \text{ k}\Omega$				$R_{R1} = 5.1 \text{ k}\Omega, R_{R2} = 510 \Omega$			
	$V_{VIN} \text{ (V)}$				$V_{VIN} \text{ (V)}$			
	7	5	3.3	1.2	7	5	3.3	1.2
220 pF	0.253	0.316	0.416	0.810	0.129	0.161	0.212	0.413
1000 pF	1.15	1.44	1.89	3.68	.586	.732	.963	1.88
4700 pF	5.4	6.75	8.88	17.3	2.76	3.44	4.53	8.83
0.18 μF	207	258	340	663	106	132	173	338
0.27 μF	310	388	510	994	158	198	260	507
0.33 μF	379	474	623	1220	194	242	318	620
1 μF	1150	1440	1890	3680	586	732	963	1880

(1) $C_{LOAD} = 10 \mu\text{F}$. Output rise time is independent of C_{LOAD} when $C_{LOAD} \gg C_{C1}$.

(2) Rise time is 250 ns for $R_{R2} = 0 \Omega$ and $C_{C1} = C_{LOAD} = 0 \text{ F}$.

8.2.1.2.3 Configuring Turnoff Delay

TPS27081A PMOS turnoff delay from the falling edge of ON/OFF logic signal depends upon the component values of resistor R1 and capacitor C1. Lower values of resistor R1 ensures quicker turnoff.

$$t_{off} > 2 \times R1 \times C1 \text{ sec} \quad (4)$$

8.2.1.2.4 Low Voltage ON/OFF Interface

The $V_{GS(Q2)}$ is set by the ON/OFF logic level. To turn ON, the transistor Q2 requires a $V_{GS} > 1.0$ V (typical). For reliable operation, apply ON/OFF logic following the high-level input voltage (V_{IH}) and low-level input voltage (V_{IL}) limits expressed in [Equation 5](#) and [Equation 6](#).

$$V_{IH(on)} > 1.0 \text{ V} + I_{Q2} \times R2 \text{ V} \quad (5)$$

$$V_{IL(off)} < 0.2 \text{ V} \quad (6)$$

Minimizing $I_{Q2} \times R2$ drop helps achieve a direct interface with a low voltage ON/OFF logic. To minimize $I_{Q2} \times R2$ voltage drop, select a high R1 and R2 ratio. For example, when $V_{VIN} = 1.8$ V, selecting R1 and R2 = 40 requires $V_{IH} > 1 + 45$ mV and thus allowing a 1.2-V GPIO interface.

In applications where ON/OFF signal is not available, connect ON/OFF pin to VIN. The TPS27081A turns ON/OFF in sync with the input supply connected to the VIN pin.

NOTE

Connect a pulldown resistor between ON/OFF pin to GND when ON/OFF is driven by a high-impedance (tri-state) driver.

8.2.1.2.5 ON-Chip Power Dissipation

Use [Equation 7](#) to calculate TPS27081A ON-chip power dissipation P_D :

$$PD = ID_{Q1}^2 \times R_{Q1(on)} + ID_{Q2}^2 \times R_{Q2(on)}$$

where

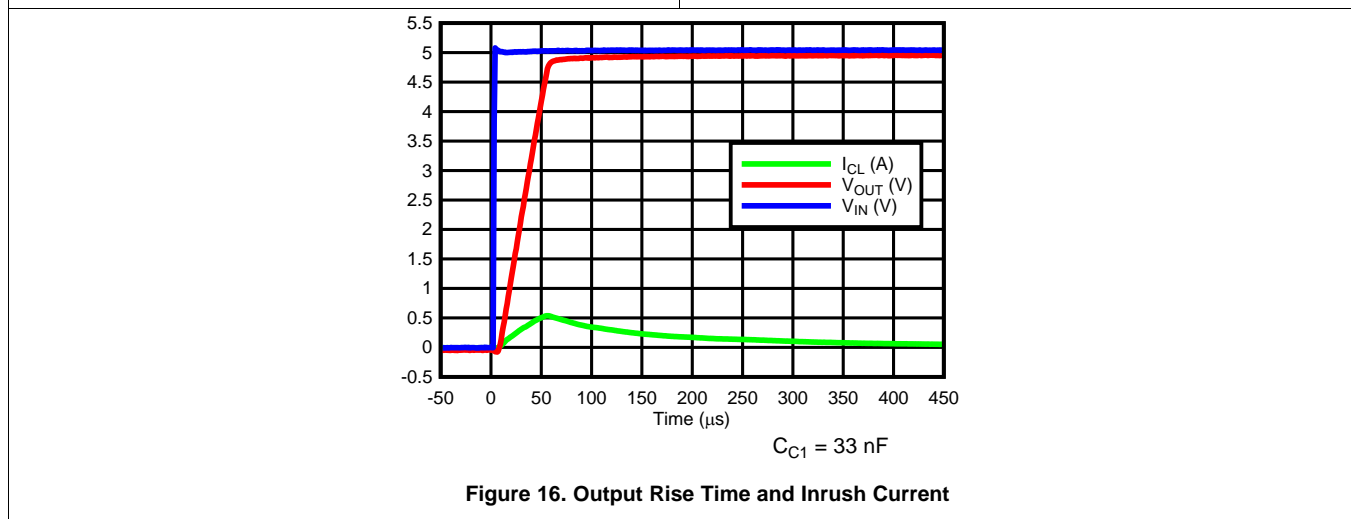
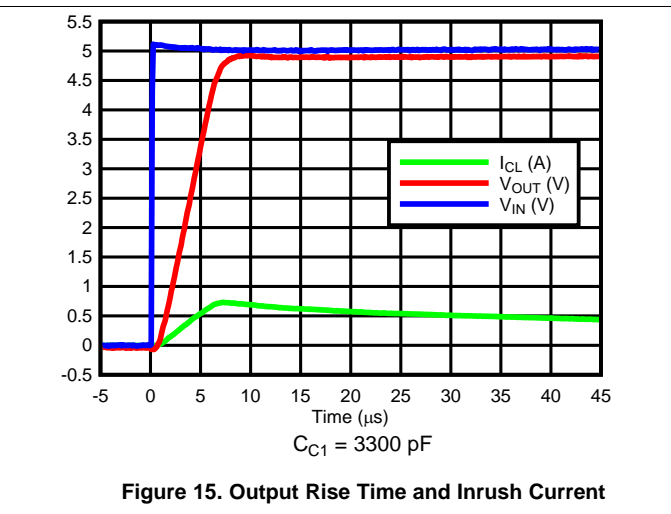
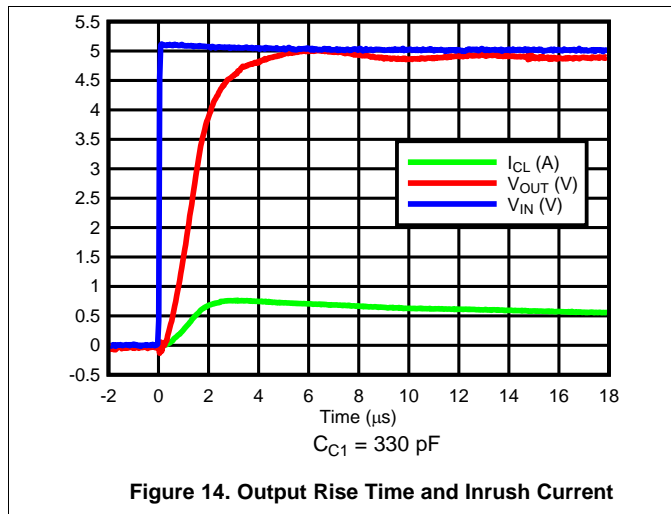
- ID_{Q1} and ID_{Q2} are the DC current flowing through the transistors Q1 and Q2, respectively. (7)

Refer to [Electrical Characteristics](#) and/or [Figure 1](#) through [Figure 7](#) to estimate $R_{Q1(on)}$ and $R_{Q2(on)}$ for various values of $V_{GS(Q1)}$ and $V_{GS(Q2)}$, respectively.

NOTE

MOS switches can get extremely hot when operated in saturation region. As a general guideline, to avoid transistors Q1 and Q2 going into saturation region, set $V_{GS} > V_T + V_{DS}$. For example, $V_{GS} > 1.5$ V and $V_{DS} < 200$ mV ensures operation as a switch.

8.2.1.3 Application Curves



8.3 System Examples

8.3.1 Standby Power Isolation

Many applications have some always ON modules to support various core functions. However, some modules are selectively powered ON or OFF to save power and multiplexing of various on board resources. Such modules that are selectively turned ON or OFF require standby power generation. In such applications TPS27081A requires only a single pull-up resistor. In the configuration shown in [Figure 17](#), the VOUT voltage rise time is approximately 250 ns when $V_{VIN} = 5\text{ V}$.

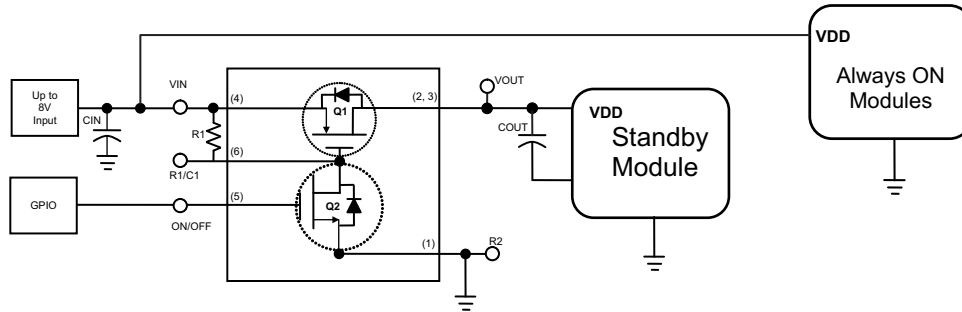


Figure 17. Standby Power Generation Using TPS27081A

8.3.2 Boost Regulator With True Shutdown

The most common boost regulator topology provides a current leakage path through inductor and diode into the feedback resistor even when the regulator shuts down. Adding a TPS27081A device in the input-side power path prevents this leakage current and thus providing a true shutdown, as shown in [Figure 18](#).

LCD panels require inrush current control to prevent permanent system damages during turnon and turnoff events.

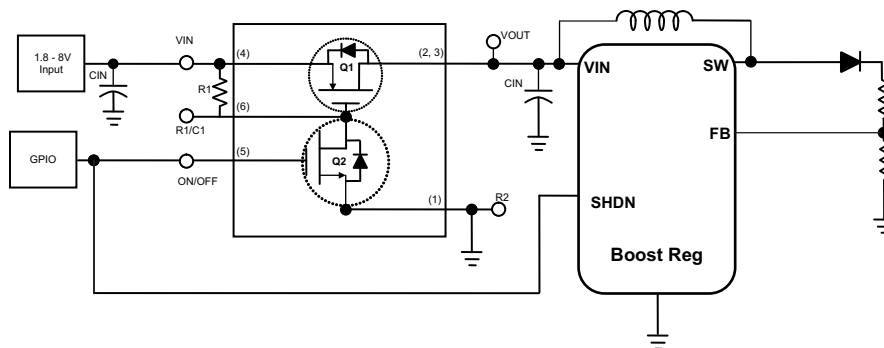


Figure 18. True Shutdown Using TPS27081A

System Examples (continued)

8.3.3 Single Module Multiple Power Supply Sequencing

Most modern SOC and CPUs require multiple voltage inputs for its analog cores, digital cores, and I/O interfaces. These devices require that these supplies be applied simultaneously or in a certain sequence. The TPS27081A device, when configured as shown in Figure 19 with the VOUT1 rise time adjusted appropriately through resistor R2 and capacitor C1, delays the early arriving LDO output to match up with late-arriving DC-DC output and thus, achieving power sequencing.

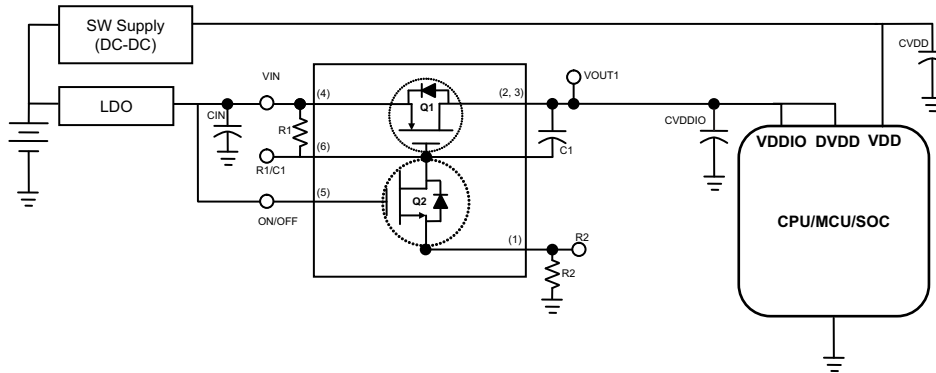


Figure 19. Power Sequencing Using TPS27081A

8.3.4 Multiple Modules Interdependent Power Supply Sequencing

For system integrity reasons, a certain power sequencing may be required among various modules. As shown in Figure 20, Module 2 powers up only after Module 1 is powered up and the Module 1 GPIO output is enabled to turn ON Module 2. The TPS27081A device, when used as shown in this example does not only sequence the Module 2 power, but it also helps prevent inrush current into the power path of Module 1 and 2.

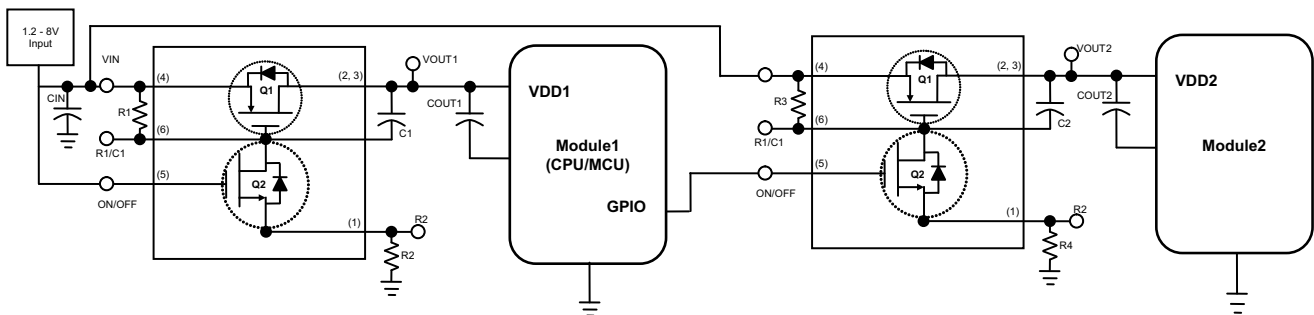


Figure 20. Power Sequencing Using TPS27081A

System Examples (continued)

8.3.5 TFT LCD Module Inrush Current Control

As shown in Figure 21, LCD panels require inrush current control to prevent permanent system damages during turnon and turnoff events.

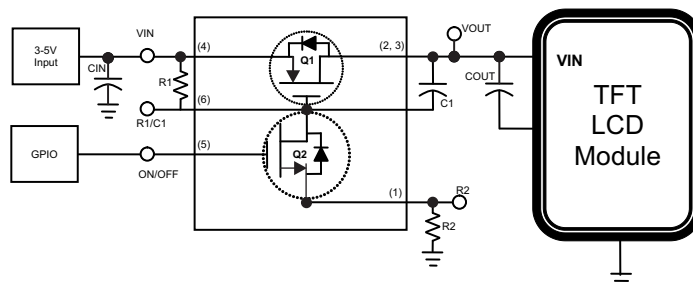


Figure 21. Inrush Current Control Using TPS27081A

8.3.6 Multiple Modules Interdependent Supply Sequencing Without a GPIO Input

When a GPIO signal is not available, connecting the ON/OFF pin of the TPS27081 device as connected to Module 2 powers up Module 2 after powering up Module 1 when the values for resistor R4 and capacitor C1 are chosen appropriately. The two TPS27081A in this configuration as shown in Figure 22 can control load inrush current.

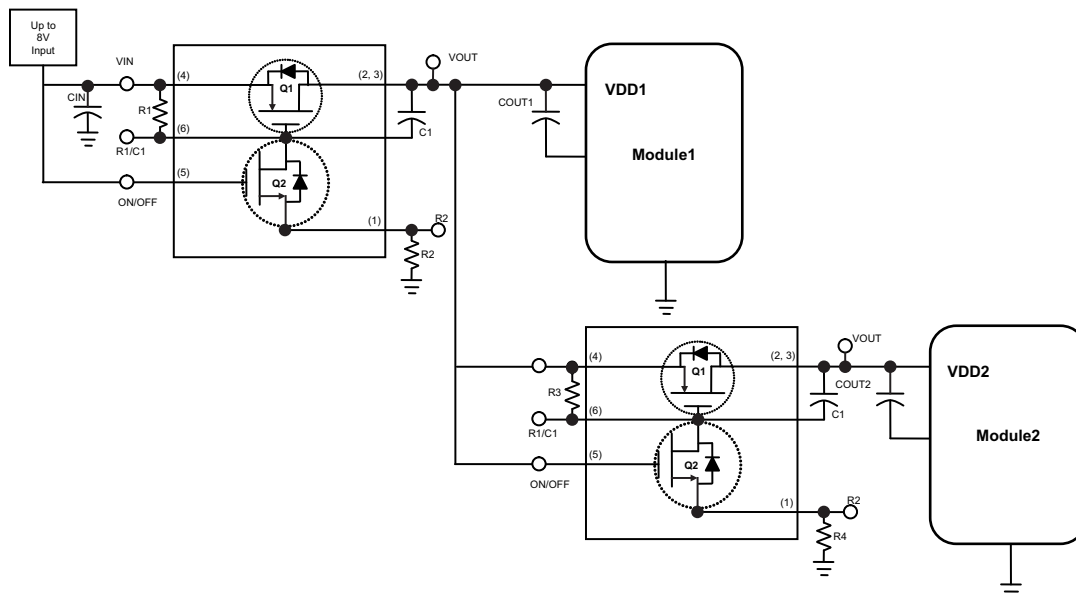


Figure 22. Power Sequencing Using TPS27081A

9 Power Supply Recommendations

The device is designed to operate from a VIN range of 1 V to 8 V. This supply must be well regulated and placed as close to the device terminal as possible with the recommended 1- μ F bypass capacitor. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 1 μ F may be sufficient.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- VIN and VOUT traces should be as short and wide as possible to accommodate for high current.
- The VIN pin should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 1- μ F ceramic with X5R or X7R dielectric. This capacitor should be placed as close to the device pins as possible.
- The VOUT pin should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is one-tenth of the VIN bypass capacitor of X5R or X7R dielectric rating. This capacitor should be placed as close to the device pins as possible.

10.2 Layout Example

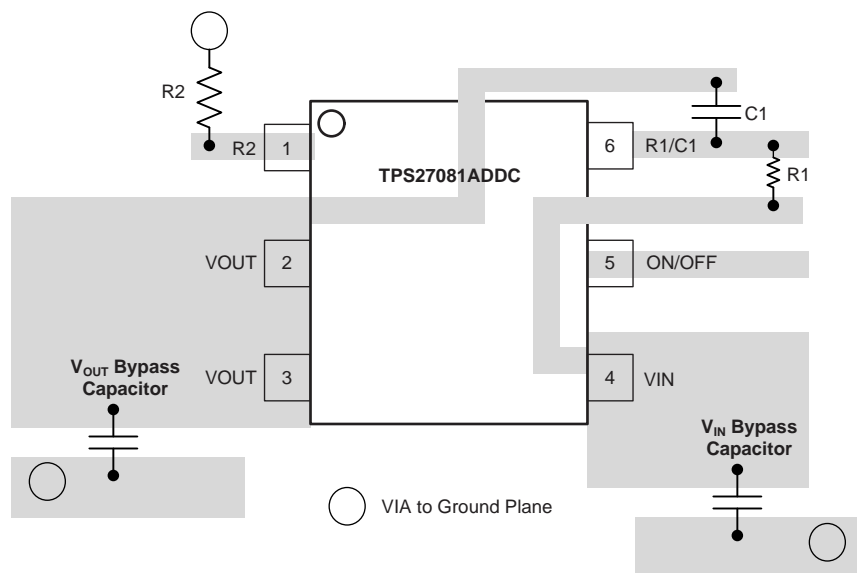


Figure 23. Layout Example

10.3 Thermal Reliability

For higher reliability, TI recommends limiting the TPS27081A die junction temperature to less than 105°C. The device junction temperature is directly proportional to the ON-chip power dissipation. Use the following equation to calculate maximum ON-chip power dissipation to achieve the maximum die junction temperature target:

$$PD_{MAX} = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

where

- $T_{J(max)}$ is the target maximum junction temperature
- T_A is the operating ambient temperature
- $R_{\theta JA}$ is the package junction to ambient thermal resistance (8)

10.4 Improving Package Thermal Performance

The package $R_{\theta JA}$ value under standard conditions on a High-K board is listed in . $R_{\theta JA}$ value depends on the PC board layout. An external heat sink and/or a cooling mechanism, like a cold air fan, can help reduce $R_{\theta JA}$ and thus improve device thermal capabilities. Refer to TI's design support web page at www.ti.com/thermal for a general guidance on improving device thermal performance.

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS27081ADDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	AUA	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

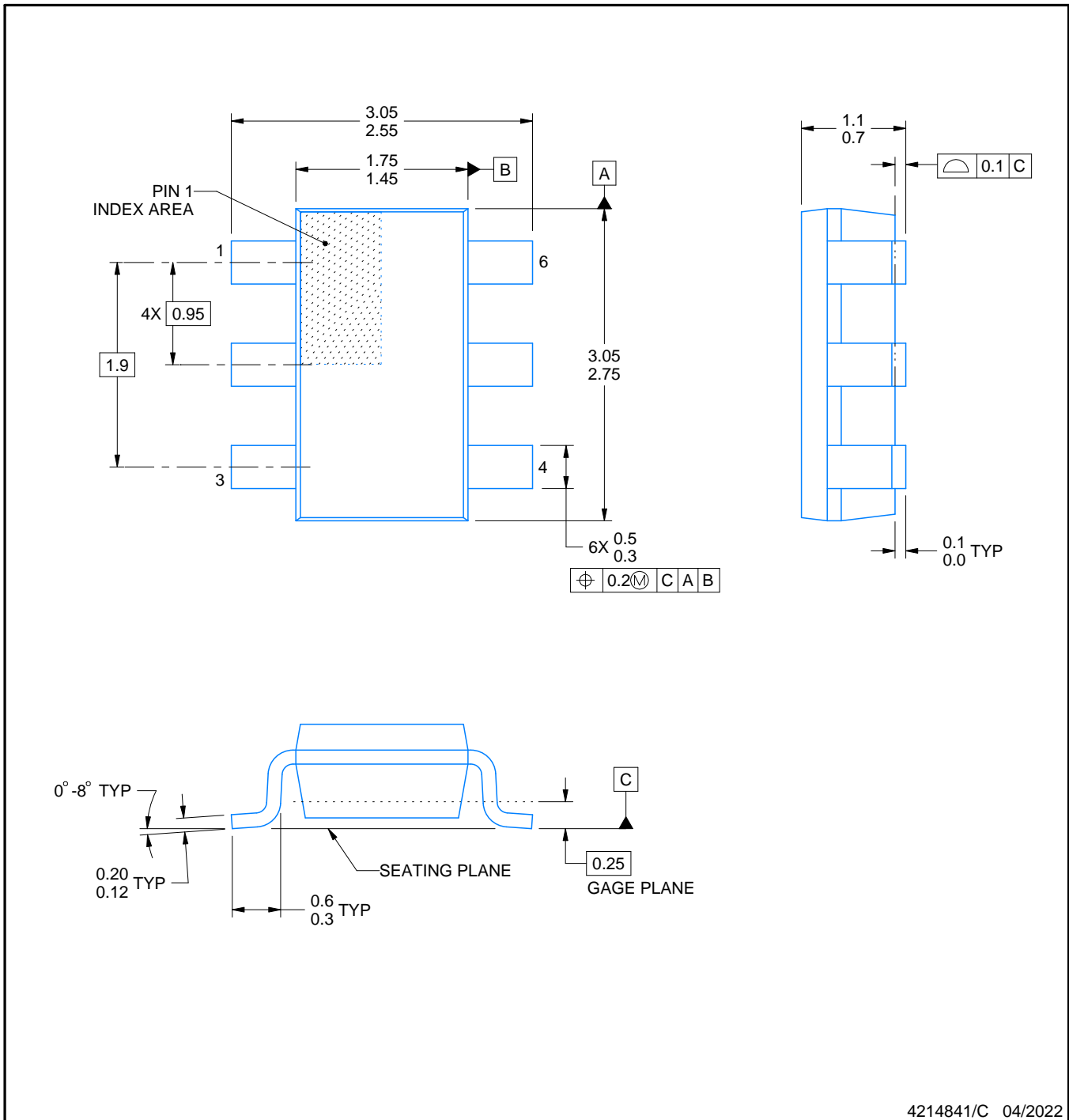

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS27081ADDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

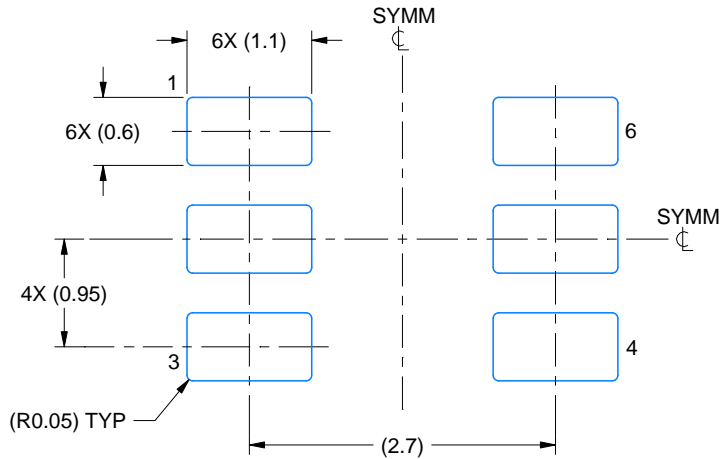
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS27081ADDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0



4214841/C 04/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLODED METAL SHOWN
SCALE:15X



SOLDEMASK DETAILS

4214841/C 04/2022

NOTES: (continued)

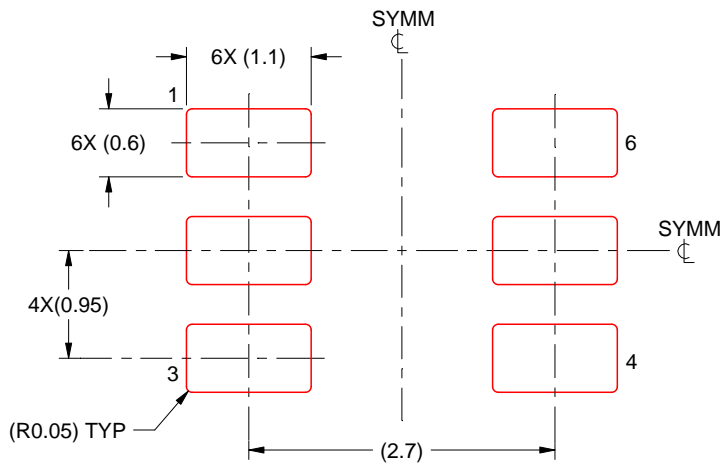
- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/C 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2023, Texas Instruments Incorporated