6-CHANNEL POWER MGMT IC WITH TWO STEP-DOWN CONVERTERS AND 4 LOW-INPUT-VOLTAGE LDOs

, TPS65051-Q1

FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Qualified With the Following Results:**
  - **Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range**
  - **Device HBM ESD Classification Level H2**
  - **Device CDM ESD Classification Level C3B**
- **Up To 95% Efficiency**
- **Output Current for DC-DC Converters:**
  - **TPS65050-Q1: 2 × 0.6 A**
  - **TPS65051-Q1: DCDC1 = 1 A; DCDC2 = 0.6 A**
  - **TPS65052-Q1: DCDC1 = 1 A; DCDC2 = 0.6 A**
  - **TPS65054-Q1: 2 × 0.6 A**
  - **TPS65056-Q1: DCDC1 = 1 A; DCDC2 = 0.6 A**
- **Output Voltages for DC-DC Converters:**
  - **TPS65050-Q1: Externally Adjustable**
  - **TPS65051-Q1: Externally Adjustable**
  - **TPS65052-Q1: DCDC1 = Fixed at 3.3 V; DCDC2 = 1 V or 1.3 V for Samsung Application Processors**
  - **TPS65054-Q1: DCDC1 = Externally Adjustable; DCDC2 = 1.3 V or 1.05 V for OMAP™1710 Processor**
  - **TPS65056-Q1: DCDC1 = Fixed at 3.3 V; DCDC2 = 1 V or 1.3 V for Samsung Application Processors**
- **V_I Range for DC-DC Converters From 2.5 V to 6 V**
- **2.25-MHz Fixed-Frequency Operation**
- **Power-Save Mode at Light Load Current**
- **180° Out-of-Phase Operation**
- **Output-Voltage Accuracy in PWM Mode ±1%**
- **Low-Ripple PFM Mode**
- **Total Typical 32-μA Quiescent Current for Both DC-DC Converters**
- **100% Duty Cycle for Lowest Dropout**
- **Two General-Purpose 400-mA, High-PSRR LDOs**
- **Two General-Purpose 200-mA, High-PSRR LDOs**
- **V_I Range for LDOs from 1.5 V to 6.5 V**
- **Digital Voltage Selection for the LDOs**
- **Available in a 4-mm × 4-mm 32-Pin QFN Package**

APPLICATIONS

Automotive

DESCRIPTION

The TPS6505x-Q1 devices are integrated power-management ICs for applications powered by one Li-Ion or Li-Polymer cell, which require multiple power rails. The TPS6505x-Q1 provides two efficient, 2.25-MHz step-down converters targeted at providing the core voltage and I/O voltage in a processor-based system. Both step-down converters enter a low-power mode at light load for maximum efficiency across the widest possible range of load currents.

For low-noise applications, the user can force the devices into fixed-frequency PWM mode by pulling the MODE pin high. Operating in the shutdown mode reduces the current consumption to less than 1 μA. The devices allow the use of small inductors and capacitors to achieve a small solution size. The TPS6505x-Q1 provides an output current of up to 1 A on each dc-dc converter. The TPS6505x-Q1 also integrates two 400-mA LDO and two 200-mA LDO voltage regulators, which one can turn on or off using separate enable pins on each LDO. Each LDO operates with an input voltage range between 1.5 V and 6.5 V, allowing their supply to be from one of the step-down converters or directly from the main battery.

Four digital input pins set the output voltage of the LDOs from a set of 16 different combinations for LDO1 to LDO4 on TPS65050-Q1 and TPS65052-Q1. In TPS65051-Q1, TPS65054-Q1, and TPS65056-Q1, the LDO voltages are adjustable using external resistor dividers.

The TPS6505x-Q1 devices come in a small 32-pin leadless package (4-mm × 4-mm QFN) with a 0.4-mm pitch.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PART NUMBER	OPTION	OUTPUT CURRENT FOR DC-DC CONVERTERS	QFN[1] PACKAGE[2]	PACKAGE MARKING
–40°C to 125°C	TPS65050QRSMRQ1 TPS65050-Q1	LDO voltages according to Table 1 DC-DC converters externally adjustable	2 x 600 mA	RSM	On demand
	TPS65051QRSMRQ1 TPS65051-Q1	LDO voltages externally adjustable DC-DC converters externally adjustable	DCDC1 = 1 A DCDC2 = 600 mA		TPS65051Q
	TPS65052QRSMRQ1 TPS65052-Q1	LDO voltages according to Table 1 DCDC1 = 3.3 V; DCDC2 = 1 V or 1.3 V	DCDC1 = 1 A DCDC2 = 600 mA		On demand
	TPS65054QRSMRQ1 TPS65054-Q1	LDO voltages externally adjustable DCDC1 = externally adjustable DCDC2 = 1.3 V or 1.05 V	2 x 600 mA		On demand
	TPS65056QRSMRQ1 TPS65056-Q1	LDO voltages externally adjustable DCDC1 = 3.3 V DCDC2 = 1 V or 1.3 V	DCDC1 = 1A DCDC2 = 600 mA		On demand

(1) The RSM package is available in tape and reel. Add the R suffix (TPS65050RSMR) to order quantities of 3000 parts per reel. Add the T suffix (TPS65050RSMT) to order quantities of 250 parts per reel.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)[1]

		UNITS
V_I	Input voltage range on all pins except AGND, PGND, and EN_LDO1 pins with respect to AGND	–0.3 V to 7 V
	Input voltage range on EN_LDO1 pins with respect to AGND	–0.3 V to V_{CC} + 0.5 V
I_I	Current at VINDCDC1/2, L1, PGND1, L2, PGND2	1800 mA
	Current at all other pins	1000 mA
V_O	Output voltage range for LDO1, LDO2, LDO3, and LDO4	–0.3 V to 4.0 V
	Continuous total power dissipation	See the Thermal Table
ESD rating	Human-body model (HBM) AEC-Q100 Classification Level H2	2 kV
	Charged-device model (CDM) AEC-Q100 Classification Level C3B	750 V
T_A	Operating free-air temperature	–40°C to 125°C
T_{stg}	Storage temperature range	–65°C to 150°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC[(1)]		TPS6505x-Q1 RSM 32 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance[(2)]	37.2	°C / W
θ_{JCtop}	Junction-to-case (top) thermal resistance[(3)]	30.1	°C / W
θ_{JB}	Junction-to-board thermal resistance[(4)]	7.8	°C / W
ψ_{JT}	Junction-to-top characterization parameter[(5)]	0.4	°C / W
ψ_{JB}	Junction-to-board characterization parameter[(6)]	7.6	°C / W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[(7)]	2.3	°C / W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_I	Input voltage range for step-down converters, VINDCDC1/2	2.5		6	V
V_O	Output voltage range for step-down converter, VDCDC1	0.6		VINDCDC1/2	V
	Output voltage range for step-down converter, VDCDC2	0.6		VINDCDC1/2	V
V_I	Input voltage range for LDOs, VINLDO1, VINLDO2, VINLDO3/4	1.5		6.5	V
V_O	Output voltage range for LDO1 and LDO2	1		3.6	V
	Output voltage range for LDO3 and LDO4	1		3.6	V
I_O	Output current at L1 (DCDC1) for TPS65051-Q1, TPS65052-Q1			1000	mA
	Output current at L1 (DCDC1) for TPS65050-Q1, TPS65054-Q1			600	mA
	Output current at L1 (DCDC2)			600	mA
	Output current at VLDO1, VLDO2			400	mA
	Output current at VLDO3, VLDO4			200	mA
	Inductor at L1, L2[(1)]	1.5	2.2		μH
C_O	Output capacitor at VDCDC1, VDCDC2[(1)]	10	22		μF
	Output capacitor at VLDO1, VLDO2, VLDO3, VLDO4[(1)]	2.2			μF
C_I	Input capacitor at VCC[(1)]	1			μF
	Input capacitor at VINLDO1, VINLDO2[(1)]	2.2			μF
	Input capacitor at VINLDO3/4[(1)]	2.2			μF
T_A	Operating ambient temperature range	–40		125	°C
	Resistor from battery voltage to V_{CC} used for filtering[(2)]		1	10	Ω

(1) See the *Application Information* section of this data sheet for more details.
(2) Up to 2 mA can flow into V_{CC}; when both converters are running in PWM, this resistor causes the UVLO threshold to shift accordingly.

ELECTRICAL CHARACTERISTICS

V_{CC} = VINDCDC1/2 = 3.6 V, EN = V_{CC}, MODE = GND, L = 2.2 µH, C_O = 10 µF, T_A = –40°C to 125°C, typical values are at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
V_I	Input voltage range at VINDCDC1/2			2.5		6	V
I_Q	Operating quiescent current Total current into V_{CC}, VINDCDC1/2, VINLDO1, VINLDO2, VINLDO3/4	One converter, I_O = 0 mA. PFM mode enabled (Mode = GND) device not switching, EN_DCDC1 = V_I OR EN_DCDC2 = V_I; EN_LDO1= EN_LDO2 = EN_LDO3 = EN_LDO = GND			20	30	µA
		Two converters, I_O = 0 mA PFM mode enabled (Mode = 0) device not switching, EN_DCDC1 = V_I AND EN_DCDC2 = V_I; EN_LDO1 = EN_LDO2 = EN_LDO3 = EN_LDO4 = GND			32	40	µA
		One converter, I_O = 0 mA. PFM mode enabled (Mode = GND) device not switching, EN_DCDC1 = V_I OR EN_DCDC2 = V_I; EN_LDO1 = EN_LDO2 = EN_LDO3 = EN_LDO4 = V_I			180	250	µA
I_Q	Operating quiescent current into V_{CC}	One converter, I_O = 0 mA. Switching with no load (Mode = V_I), PWM operation EN_DCDC1 = V_I OR EN_DCDC2 = V_I; EN_LDO1 = EN_LDO2 = EN_LDO3 = EN_LDO = GND			0.85		mA
		Two converters, I_O = 0 mA Switching with no load (Mode = V_I), PWM operation EN_DCDC1 = V_I AND EN_DCDC2 = V_I; EN_LDO1 = EN_LDO2 = EN_LDO3 = EN_LDO = GND			1.25		mA
$I_{(SD)}$	Shutdown current	EN_DCDC1 = EN_DCDC2 = GND EN_LDO1 = EN_LDO2 = EN_LDO3 = EN_LDO4 = GND			9	12	µA
$V_{(UVLO)}$	Undervoltage lockout threshold for DCDC converters and LDOs	Voltage at V_{CC}			1.8	2	V
EN_DCDC1, EN_DCDC2, DEFDCDC2, DEFLDO1, DEFLDO2, DEFLDO3, DEFLDO4, EN_LDO1, EN_LDO2, EN_LDO3, EN_LDO4							
V_{IH}	High-level input voltage	MODE, EN_DCDC1, EN_DCDC2, DEFDCDC2, DEFLDO1, DEFLDO2, DEFLDO3, DEFLDO4, EN_LDO1, EN_LDO2, EN_LDO3, EN_LDO4		1.2		V_{CC}	V
V_{IL}	Low-level input voltage	MODE, EN_DCDC1, EN_DCDC2, DEFLDO1, DEFLDO2, DEFLDO3, DEFLDO4, EN_LDO1, EN_LDO2, EN_LDO3, EN_LDO4, DEFDCDC2		0		0.4	V
I_{IB}	Input bias current	MODE = GND or V_I MODE, EN_DCDC1, EN_DCDC2, DEFDCDC2, DEFLDO1, DEFLDO2, DEFLDO3, DEFLDO4, EN_LDO1, EN_LDO2, EN_LDO3, EN_LDO4			0.01	1	µA
		TPS65051-Q1 and TPS65052-Q1 only V_FB_LDOx = 1 V FB_LDO1, FB_LDO2, FB_LDO3, FB_LDO4				100	nA
POWER SWITCH							
$r_{DS(on)}$	P-channel MOSFET on-resistance	DCDC1	VINDCDC1/2 = 3.6 V		280	630	mΩ
			VINDCDC1/2 = 2.5 V		400		
		DCDC2	VINDCDC1/2 = 3.6 V		280	630	
			VINDCDC1/2 = 2.5 V		400		
I_{lkg}	P-channel leakage current	VDCDCx = $V_{(DS)}$ = 6 V				1	µA
$r_{DS(on)}$	N-channel MOSFET on-resistance	DCDC1	VINDCDC1/2 = 3.6 V		220	450	mΩ
			VINDCDC1/2 = 2.5 V		320		
		DCDC2	VINDCDC1/2 = 3.6 V		220	450	
			VINDCDC1/2 = 2.5 V		320		
I_{lkg}	N-channel leakage current	VDCDCx = $V_{(DS)}$ = 6 V			7	10	µA
$I_{(LIMF)}$	Forward current limit PMOS (high side) and NMOS (low side) — DCDC1:	TPS65050-Q1, TPS65054-Q1	2.5 V ≤ VINDCDC1/2 ≤ 6 V	0.85	1	1.15	A
		TPS65051-Q1, TPS65052-Q1, TPS65056-Q1		1.19	1.4	1.65	
	DCDC2:	TPS65050-Q1–TPS65056-Q1	2.5 V ≤ VINDCDC1/2 ≤ 6 V	0.85	1	1.15	A
	Thermal shutdown	Increasing junction temperature			150		°C
	Thermal shutdown hysteresis	Decreasing junction temperature			20		°C

ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = VINDCDC1/2 = 3.6 V, EN = V_{CC}, MODE = GND, L = 2.2 µH, C_O = 10 µF, T_A = –40°C to 125°C, typical values are at T_A = 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
OSCILLATOR							
f_{SW}	Oscillator frequency			2.025	2.25	2.475	MHz
OUTPUT							
V_O	Output-voltage range for DCDC1, DCDC2		Externally adjustable versions	0.6		VINDCDC1/2	V
V_{ref}	Reference voltage		Externally adjustable versions		600		mV
V_O	DC output-voltage accuracy	DCDC1, DCDC2[1]	VINDCDC1/2 = 2.5 V to 6 V, 0 mA < I_O = < I_O(maximum) MODE = GND, PFM operation	–2%	0	2%	
			VINDCDC1/2 = 2.5 V to 6 V, 0 mA < I_O = < I_O(maximum) MODE = V_I, PWM operation	–1%	0	1%	
ΔV_O	Power-save-mode ripple voltage[2]		I_O = 1 mA, MODE = GND, V_O = 1.3 V, bandwith = 20 MHz		25		mV_{PP}
t_{Start}	Start-up time		Time from active EN to start switching		170		µs
t_{Ramp}	VOUT ramp-up time		Time to ramp from 5% to 95% of V_O		750		µs
	$\overline{RESET}$ delay time		Input voltage at threshold pin rising	80	100	120	ms
	PB-ONOFF debounce time			26	32	38	ms
V_{OL}	$\overline{RESET}$, PB_OUT output low voltage		I_{OL} = 1 mA, Vhysteresis < 1 V, Vthreshold < 1 V			0.2	V
I_{OL}	$\overline{RESET}$, PB_OUT sink current				1		mA
	$\overline{RESET}$, PB_OUT output leakage current		After PB_IN has been pulled high once; Vthreshold > 1 V and Vhysteresis > 1 V, V_{OH} = 6 V		10		nA
V_{th}	Vthreshold, Vhysteresis threshold			0.98	1	1.02	V
VLDO1, VLDO2, VLDO3 and VLDO4 Low-Dropout Regulators							
V_I	Input-voltage range for LDO1, LDO2, LDO3, LDO4			1.5		6.5	V
V_O	LDO1 output-voltage range		TPS65050-Q1, TPS65052-Q1 only	1.2		3.3	V
	LDO2 output-voltage range		TPS65050-Q1, TPS65052-Q1 only	1.8		3.3	
	LDO3 output-voltage range		TPS65050-Q1, TPS65052-Q1 only	1.1		3.3	
	LDO4 output-voltage range		TPS65050-Q1, TPS65052-Q1 only	1.2		2.85	
$V_{(FB)}$	Feedback voltage for FB_LDO1, FB_LDO2, FB_LDO3, and FB_LDO4		TPS65051-Q1, TPS65054-Q1, and TPS65056-Q1 only		1		V
I_O	Maximum output current for LDO1, LDO2			400			mA
	Maximum output current for LDO3, LDO4			200			
$I_{(SC)}$	LDO1 short-circuit current limit		VLDO1 = GND			750	mA
	LDO2 short-circuit current limit		VLDO2 = GND			850	
	LDO3 and LDO4 short-circuit current limit		VLDO3 = GND, VLDO4 = GND			420	
	Dropout voltage at LDO1		I_O = 400 mA, VINLDO = 3.4 V			400	mV
	Dropout voltage at LDO2		I_O = 400 mA, VINLDO = 1.8 V			280	
	Dropout voltage at LDO3, LDO4		I_O = 200 mA, VINLDO = 1.8 V			280	
I_{lkg}	Leakage current from VinLDOx to VLDOx		LDO enabled, VINLDO = 6.5 V, V_O = 1 V at T_A = 140°C		3		µA
V_O	Output voltage accuracy for LDO1, LDO2, LDO3, LDO4		I_O = 10 mA	–2%		1%	
	Line regulation for LDO1, LDO2, LDO3, LDO4		VINLDO1,2 = VLDO1,2 + 0.5 V (minimum 2.5 V) to 6.5 V, VINLDO3,4 = VLDO3,4 + 0.5 V (minimum 2.5 V) to 6.5 V, I_O = 10 mA	–1%		1%	
	Load regulation for LDO1, LDO2, LDO3, LDO4		I_O = 0 mA to 400 mA for LDO1, LDO2 I_O = 0 mA to 200 mA for LDO3, LDO4	–1%		1%	
	Regulation time for LDO1, LDO2, LDO3, LDO4		Load change from 10% to 90%		10		µs
PSRR	Power-supply rejection ratio		f = 10 kHz; I_O = 50 mA; V_I = V_O + 1 V		70		dB

(1) Output voltage specification does not include tolerance of external voltage-programming resistors.
(2) In power-save mode, device typically enters operation at I_{PSM} = V_I / 32 Ω.

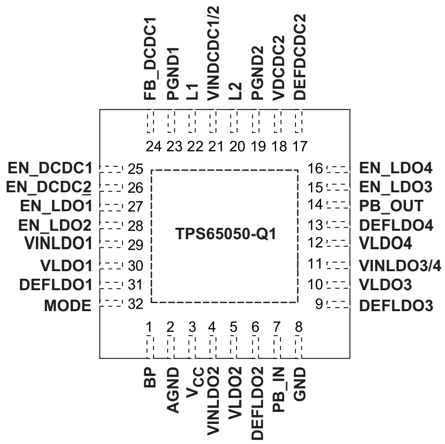
ELECTRICAL CHARACTERISTICS (continued)

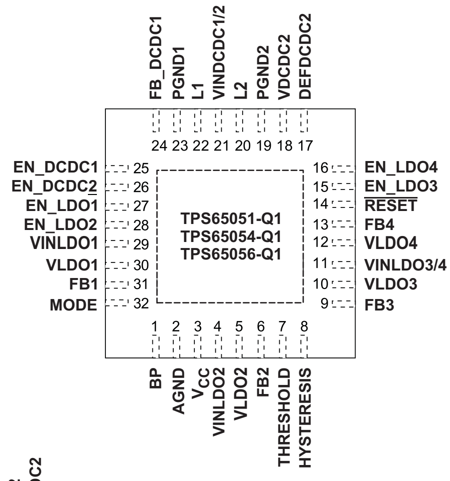
V_{CC} = VINDCDC1/2 = 3.6 V, EN = V_{CC}, MODE = GND, L = 2.2 µH, C_O = 10 µF, T_A = –40°C to 125°C, typical values are at T_A = 25°C (unless otherwise noted).

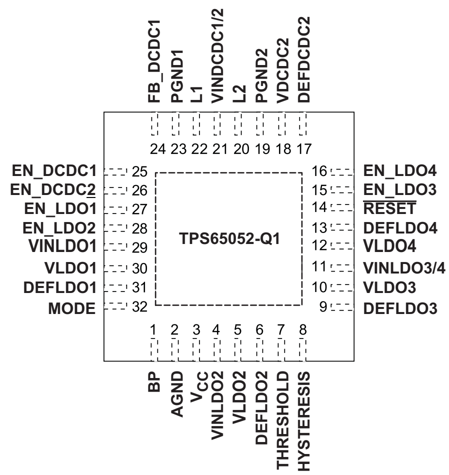
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{(DIS)}$	Internal discharge resistor at VLDO1, VLDO2, VLDO3, VLDO4	Active when LDO is disabled		350		R
	Thermal shutdown	Increasing junction temperature		140		°C
	Thermal shutdown hysteresis	Decreasing junction temperature		20		°C

PIN ASSIGNMENTS

RSM PACKAGE
(TOP VIEW)







TERMINAL FUNCTIONS

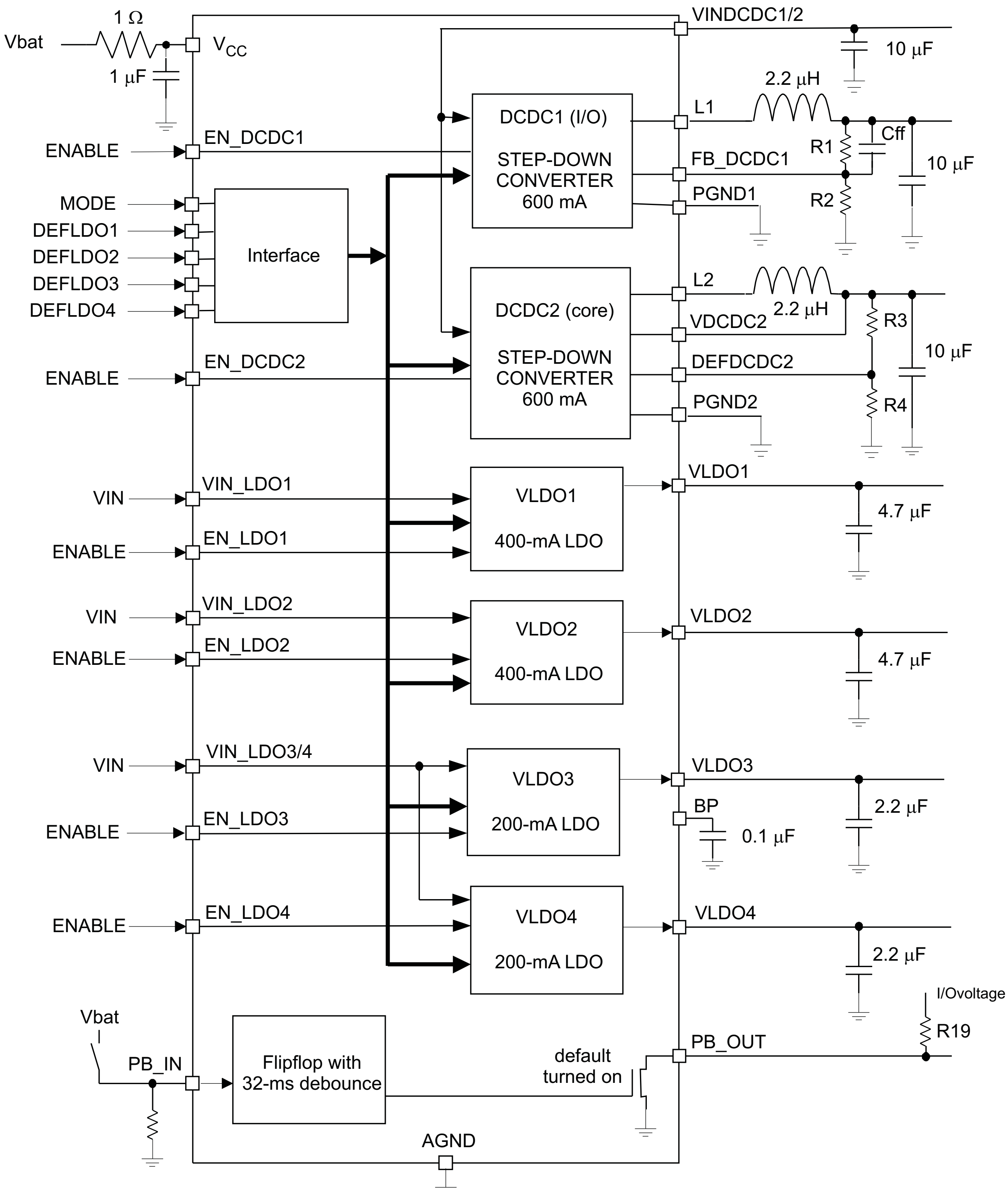
TERMINAL						I/O	DESCRIPTION
NAME	TPS65050-Q1	TPS65051-Q1	TPS65052-Q1	TPS65054-Q1	TPS65056-Q1		
AGND	2	2	2	2	2	I	Analog GND, connect to PGND and thermal pad
BP	1	1	1	1	1	I	Input for bypass capacitor for internal reference
DEFDCDC2	17	17	17	17	17	I	TPS65050-Q1 and TPS65051-Q1: Feedback pin for converter 2. Connect DEFDCDC2 to the center of the external resistor divider. TPS65052-Q1 and TPS65056-Q1: Select pin of converter 2 output voltage. High = 1.3 V, Low = 1 V TPS65054-Q1: Select pin of converter 2 output voltage. High = 1.05 V, Low = 1.3 V
DEFLDO1	31	--	31	--	--	I	Digital input, used to set the default output voltage of LDO1 to LDO4; LSB
DEFLDO2	6	--	6	--	--	I	Digital input, used to set the default output voltage of LDO1 to LDO4
DEFLDO3	9	--	9	--	--	I	Digital input, used to set the default output voltage of LDO1 to LDO4
DEFLDO4	13	--	13	--	--	I	Digital input, used to set the default output voltage of LDO1 to LDO4; MSB
EN_DCDC1	25	25	25	25	25	I	Enable input for converter 1, active-high
EN_DCDC2	26	26	26	26	26	I	Enable input for converter 2, active-high
EN_LDO1	27	27	27	27	27	I	Enable input for LDO1. Logic high enables the LDO, logic low disables the LDO.
EN_LDO2	28	28	28	28	28	I	Enable input for LDO2. Logic high enables the LDO, logic low disables the LDO.
EN_LDO3	15	15	15	15	15	I	Enable input for LDO3. Logic high enables the LDO, logic low disables the LDO.
EN_LDO4	16	16	16	16	16	I	Enable input for LDO4. Logic high enables the LDO, logic low disables the LDO.
FB1	--	31	--	31	31	I	Feedback input for the external voltage divider
FB2	--	6	--	6	6	I	Feedback input for the external voltage divider
FB3	--	9	--	9	9	I	Feedback input for the external voltage divider
FB4	--	13	--	13	13	I	Feedback input for the external voltage divider
FB_DCDC1	24	24	24	24	24	I	Input to adjust output voltage of converter 1 between 0.6 V and V_I. Connect an external resistor divider between VOUT1, this pin, and GND.
GND	8	--	--	--	--	-	Connect to GND
HYSTERESIS	--	8	8	8	8	I	Input for hysteresis on reset threshold
L1	22	22	22	22	22	O	Switch pin of converter 1. Connected to inductor
L2	20	20	20	20	20	O	Switch pin of converter 2. Connected to inductor
MODE	32	32	32	32	32	I	Select between power-safe mode and forced-PWM mode for DCDC1 and DCDC2. In power-safe mode, the device uses PFM at light loads, PWM for higher loads. Setting this pin to high level selects forced-PWM mode. If this pin has low level, then the device operates in power-safe mode.
PB_IN	7	--	--	--	--	I	Input for the pushbutton ON-OFF function
PB_OUT	14	--	--	--	--	O	Open-drain output. Active-low after the supply voltage (V_{CC}) exceeds the undervoltage-lockout threshold. Toggle the pin by pulling PB_IN high.
PGND1	23	23	23	23	23	I	GND for converter 1
PGND2	19	19	19	19	19	I	GND for converter 2
$\overline{\text{RESET}}$	--	14	14	14	14	O	Open-drain active-low reset output, 100-ms reset-delay time
THRESHOLD	--	7	7	7	7	I	Reset input
V_{CC}	3	3	3	3	3	I	Power supply for digital and analog circuitry of DCDC1, DCDC2 and LDOs. Connect this pin to the same voltage supply as VINDCDC1/2.
VDCDC2	18	18	18	18	18	I	Feedback voltage-sense input, connect directly to the output of converter 2.
VINDCDC1/2	21	21	21	21	21	I	Input voltage for VDCDC1 and VDCDC2 step-down converters. Connect this pin to the same voltage supply as V_{CC}.
VINLDO1	29	29	29	29	29	I	Input voltage for LDO1

TERMINAL FUNCTIONS (continued)

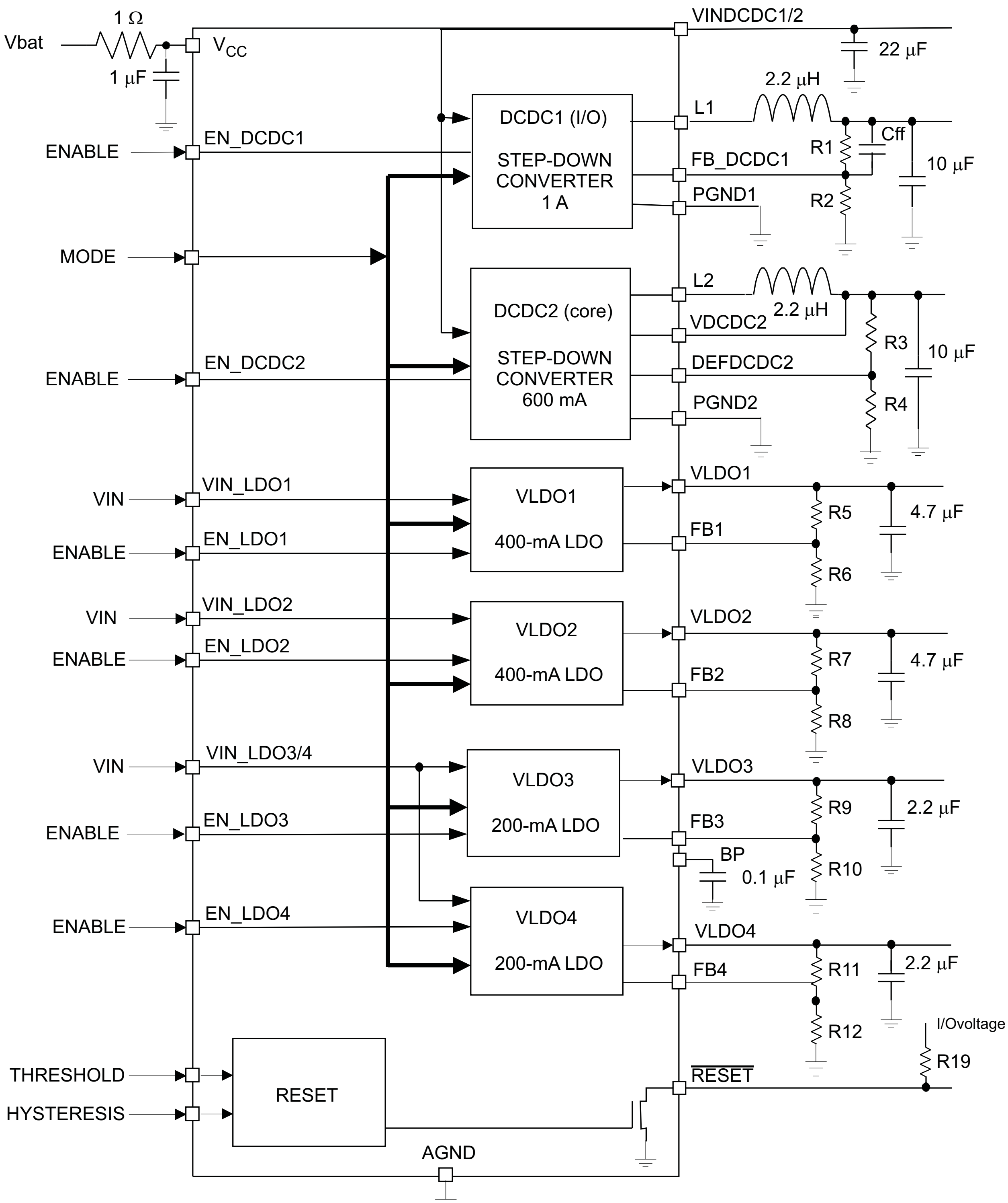
TERMINAL						I/O	DESCRIPTION
NAME	TPS65050-Q1	TPS65051-Q1	TPS65052-Q1	TPS65054-Q1	TPS65056-Q1		
VINLDO2	4	4	4	4	4	I	Input voltage for LDO2
VINLDO3/4	11	11	11	11	11	I	Input voltage for LDO3 and LDO4
VLDO1	30	30	30	30	30	O	Output voltage of LDO1
VLDO2	5	5	5	5	5	O	Output voltage of LDO2
VLDO3	10	10	10	10	10	O	Output voltage of LDO3
VLDO4	12	12	12	12	12	O	Output voltage of LDO4
Thermal pad	--	--	--	--	--		Connect to GND.

FUNCTIONAL BLOCK DIAGRAM

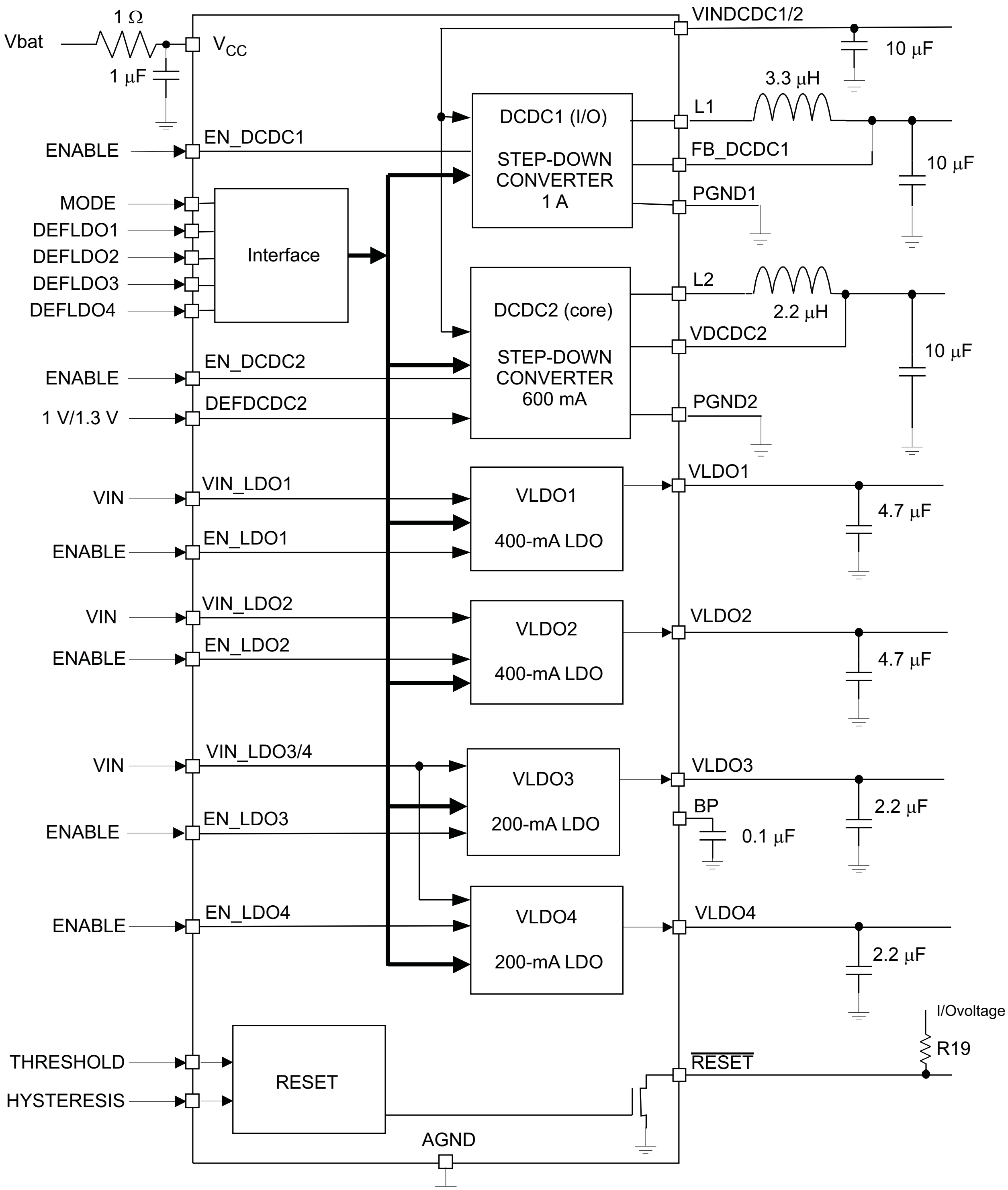
TPS65050-Q1



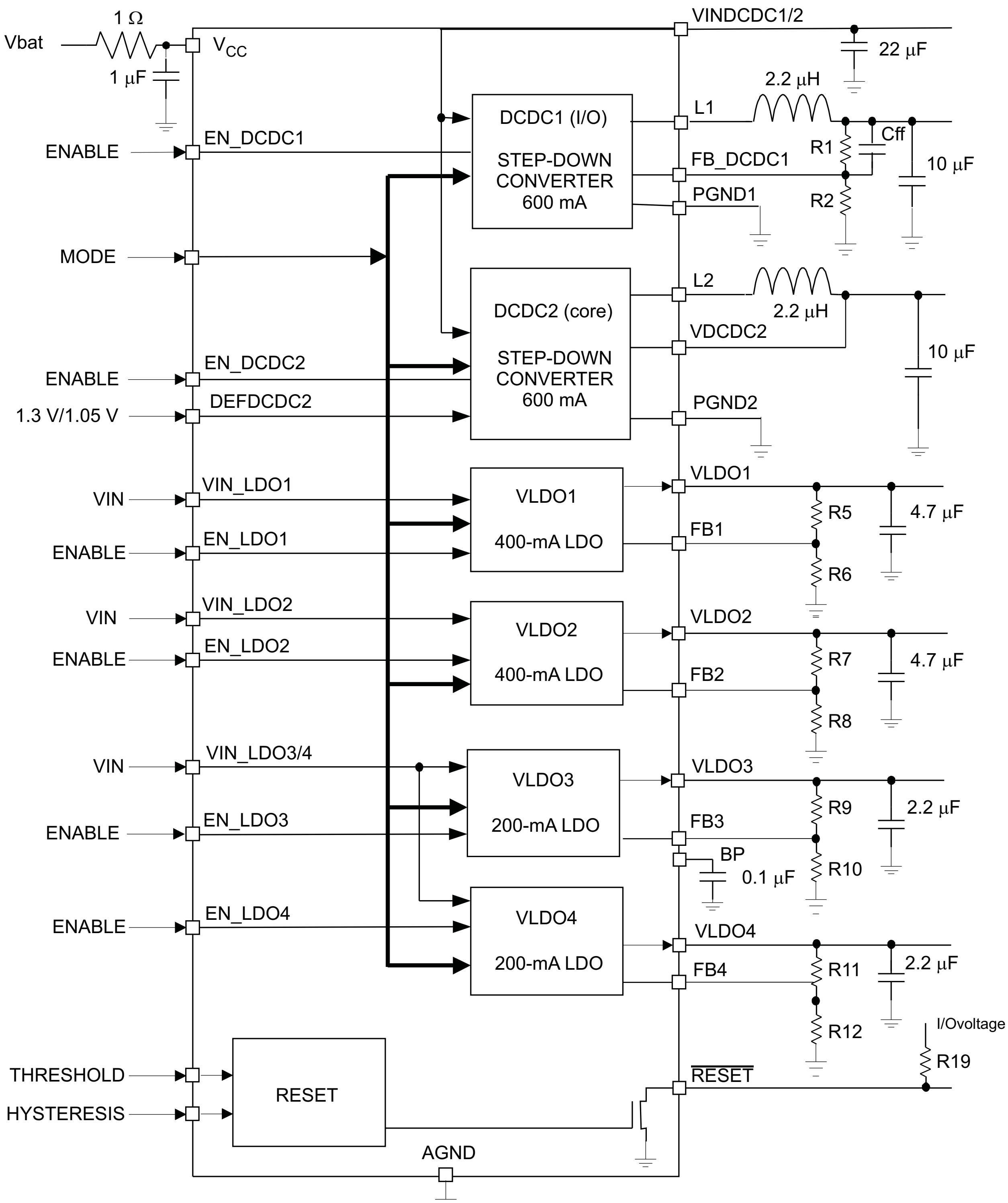
TPS65051-Q1


Vbat
1 Ω
1 µF
VCC
VINDCDC1/2
22 µF
2.2 µH
ENABLE
EN_DCDC1
DCDC1 (I/O)
STEP-DOWN CONVERTER 1 A
L1
FB_DCDC1
PGND1
R1
R2
Cff
10 µF
MODE
DCDC2 (core)
STEP-DOWN CONVERTER 600 mA
L2
VDCDC2
DEFDCDC2
PGND2
R3
R4
EN_DCDC2
VIN
VIN_LDO1
EN_LDO1
VLDO1
400-mA LDO
FB1
R5
R6
4.7 µF
VIN_LDO2
EN_LDO2
VLDO2
FB2
R7
R8
VIN_LDO3/4
EN_LDO3
VLDO3
200-mA LDO
FB3
BP
0.1 µF
R9
R10
2.2 µF
EN_LDO4
VLDO4
FB4
R11
R12
I/Ovoltage
R19
THRESHOLD
HYSTERESIS
RESET
AGND

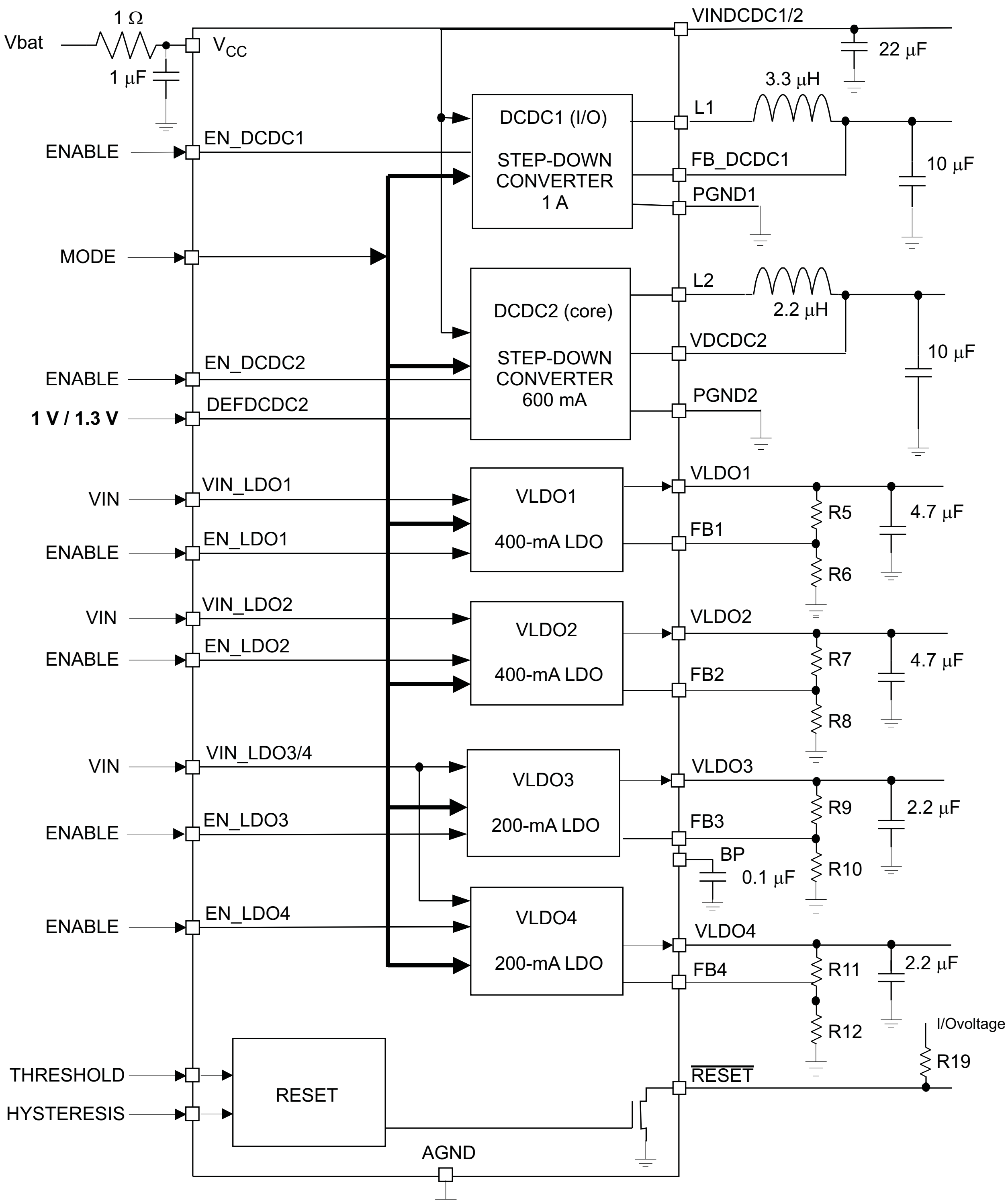
TPS65052-Q1


1 Ω
Vbat
VCC
1 µF
ENABLE
EN_DCDC1
MODE
DEFLDO1
DEFLDO2
DEFLDO3
DEFLDO4
Interface
ENABLE
EN_DCDC2
1 V/1.3 V
DEFDCDC2
VIN
VIN_LDO1
ENABLE
EN_LDO1
VIN
VIN_LDO2
ENABLE
EN_LDO2
VIN
VIN_LDO3/4
ENABLE
EN_LDO3
ENABLE
EN_LDO4
THRESHOLD
HYSTERESIS
RESET
AGND
DCDC1 (I/O)
STEP-DOWN
CONVERTER
1 A
DCDC2 (core)
STEP-DOWN
CONVERTER
600 mA
VLDO1
400-mA LDO
VLDO2
400-mA LDO
VLDO3
200-mA LDO
VLDO4
200-mA LDO
VINDCDC1/2
10 µF
3.3 µH
L1
FB_DCDC1
10 µF
PGND1
L2
2.2 µH
VDCDC2
10 µF
PGND2
VLDO1
4.7 µF
VLDO2
4.7 µF
VLDO3
BP
0.1 µF
2.2 µF
VLDO4
2.2 µF
I/Ovoltage
R19
RESET

TPS65054-Q1


Vbat
1 Ω
1 µF
VCC
VINDCDC1/2
22 µF
ENABLE
EN_DCDC1
DCDC1 (I/O)
STEP-DOWN
CONVERTER
600 mA
L1
2.2 µH
R1
Cff
FB_DCDC1
10 µF
PGND1
R2
MODE
DCDC2 (core)
STEP-DOWN
CONVERTER
600 mA
L2
2.2 µH
VDCDC2
10 µF
ENABLE
EN_DCDC2
1.3 V/1.05 V
DEFDCDC2
PGND2
VIN
VIN_LDO1
VLDO1
400-mA LDO
VLDO1
R5
4.7 µF
ENABLE
EN_LDO1
FB1
R6
VIN
VIN_LDO2
VLDO2
400-mA LDO
VLDO2
R7
4.7 µF
ENABLE
EN_LDO2
FB2
R8
VIN
VIN_LDO3/4
VLDO3
200-mA LDO
VLDO3
R9
2.2 µF
ENABLE
EN_LDO3
FB3
BP
0.1 µF
R10
ENABLE
EN_LDO4
VLDO4
200-mA LDO
VLDO4
R11
2.2 µF
FB4
R12
I/Ovoltage
R19
THRESHOLD
HYSTERESIS
RESET
RESET
AGND

TPS65056-Q1


Vbat
1 Ω
1 µF
VCC
VINDCDC1/2
22 µF
3.3 µH
L1
DCDC1 (I/O)
STEP-DOWN CONVERTER 1 A
FB_DCDC1
PGND1
10 µF
ENABLE
EN_DCDC1
MODE
L2
2.2 µH
DCDC2 (core)
STEP-DOWN CONVERTER 600 mA
VDCDC2
10 µF
ENABLE
EN_DCDC2
1 V / 1.3 V
DEFDCDC2
PGND2
VIN
VIN_LDO1
VLDO1
400-mA LDO
VLDO1
R5
4.7 µF
FB1
R6
ENABLE
EN_LDO1
VIN
VIN_LDO2
VLDO2
400-mA LDO
VLDO2
R7
4.7 µF
FB2
R8
ENABLE
EN_LDO2
VIN
VIN_LDO3/4
VLDO3
200-mA LDO
VLDO3
R9
2.2 µF
FB3
BP
0.1 µF
R10
ENABLE
EN_LDO3
ENABLE
EN_LDO4
VLDO4
200-mA LDO
VLDO4
FB4
R11
2.2 µF
R12
I/Ovoltage
R19
THRESHOLD
HYSTERESIS
RESET
RESET
AGND

TYPICAL CHARACTERISTICS

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	LDO4 load transient response		Figure 16
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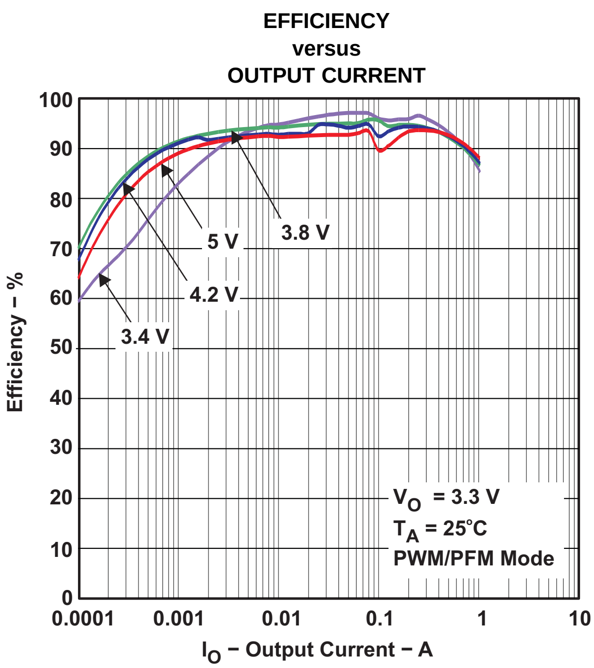

Figure 1.

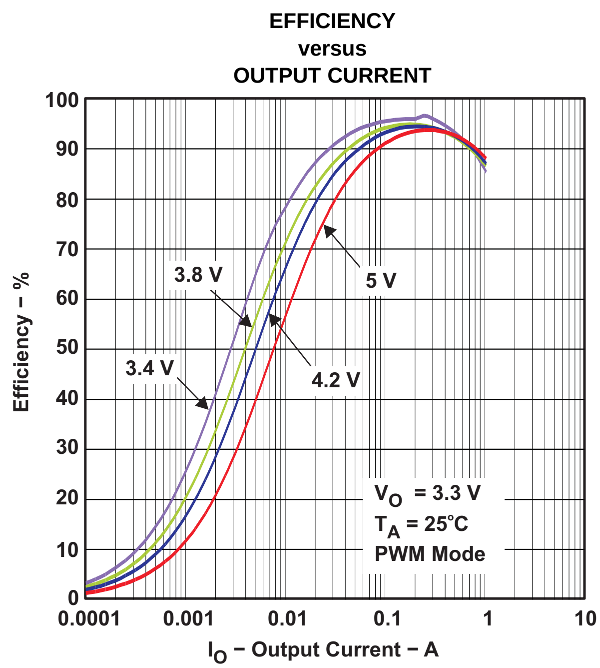

Figure 2.

TYPICAL CHARACTERISTICS (continued)

EFFICIENCY
versus
OUTPUT CURRENT

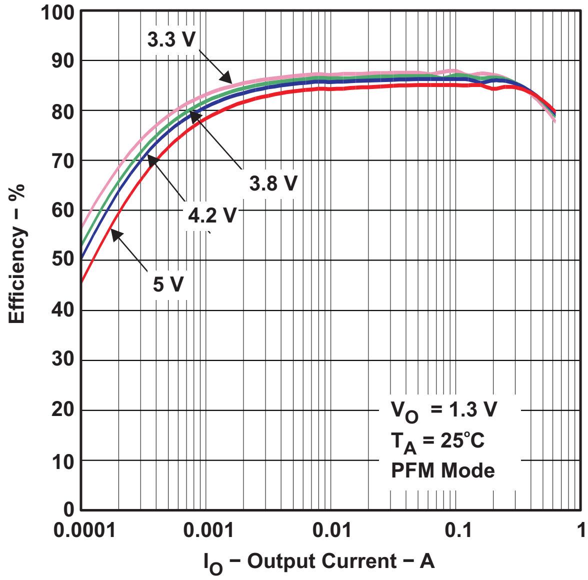

Figure 3.

EFFICIENCY
versus
OUTPUT CURRENT

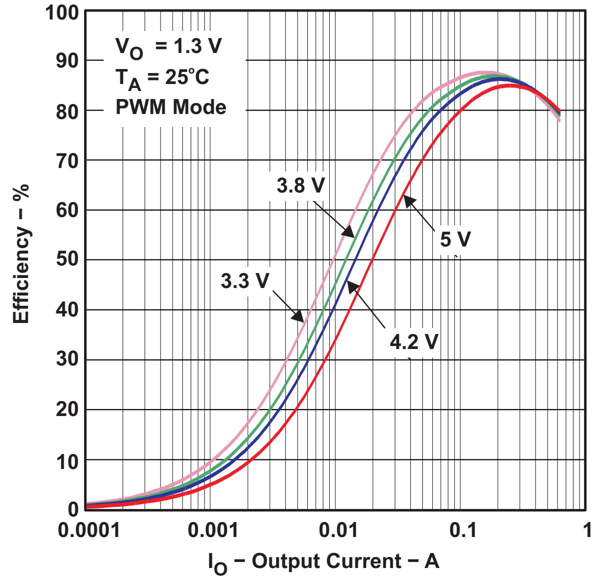

Figure 4.

OUTPUT VOLTAGE RIPPLE
PWM or PFM MODE = LOW

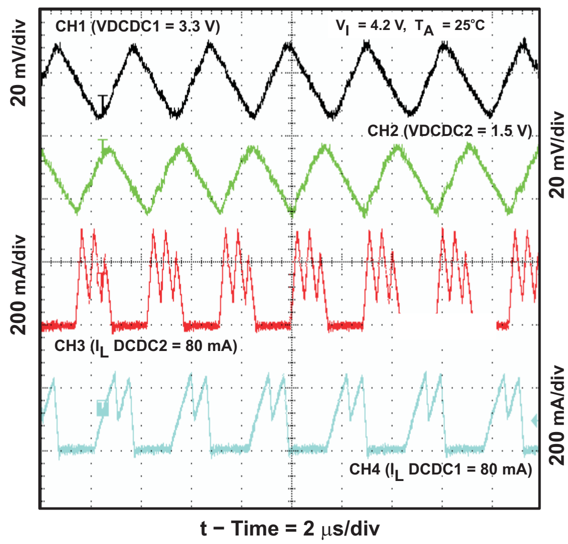

Figure 5.

OUTPUT VOLTAGE RIPPLE
PWM MODE = HIGH

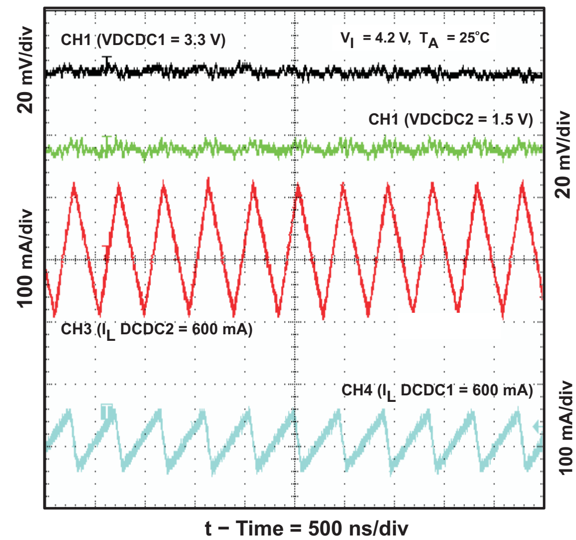

Figure 6.

TYPICAL CHARACTERISTICS (continued)

DCDC1 STARTUP TIMING

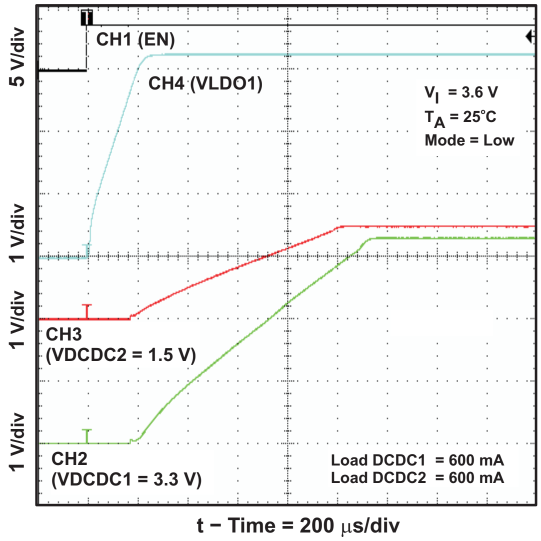

Figure 7.

LDO1 TO LDO4 STARTUP TIMING

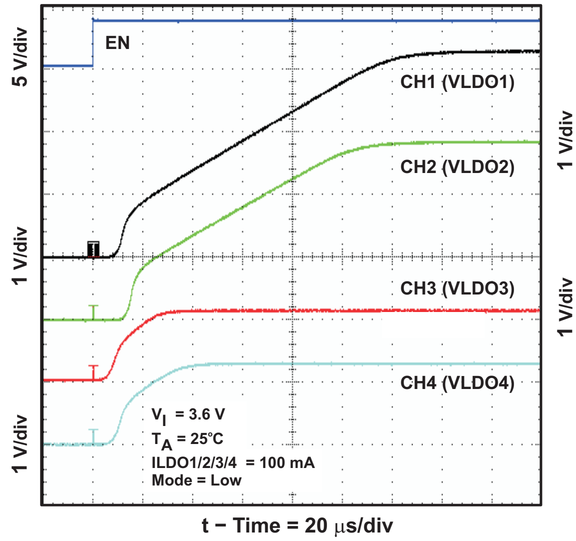

Figure 8.

DCDC1 LOAD TRANSIENT RESPONSE

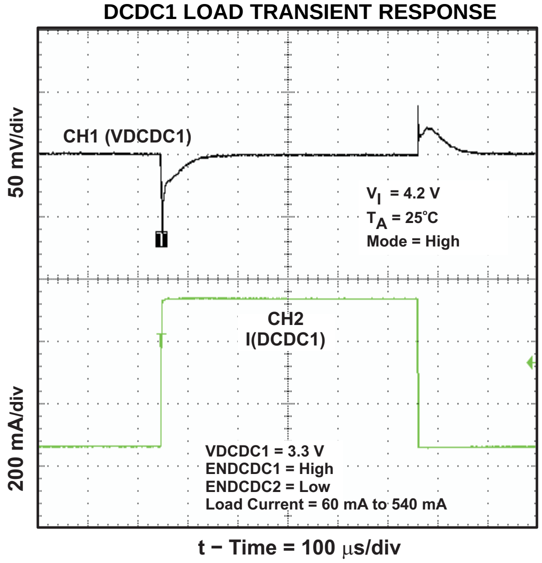

Figure 9.

DCDC1 LOAD TRANSIENT RESPONSE

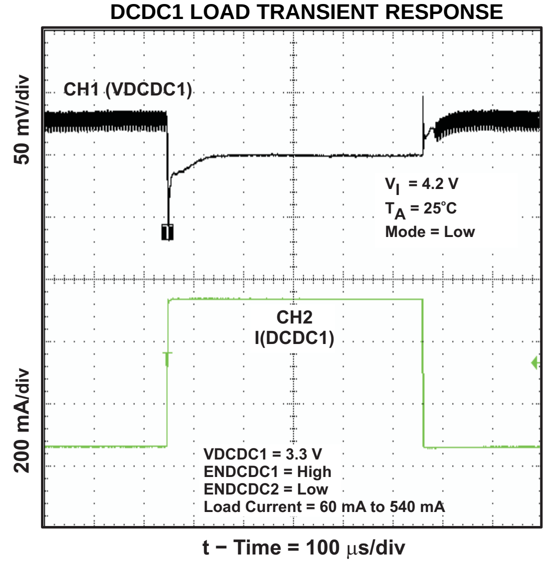

Figure 10.

TYPICAL CHARACTERISTICS (continued)

DCDC2 LOAD TRANSIENT RESPONSE

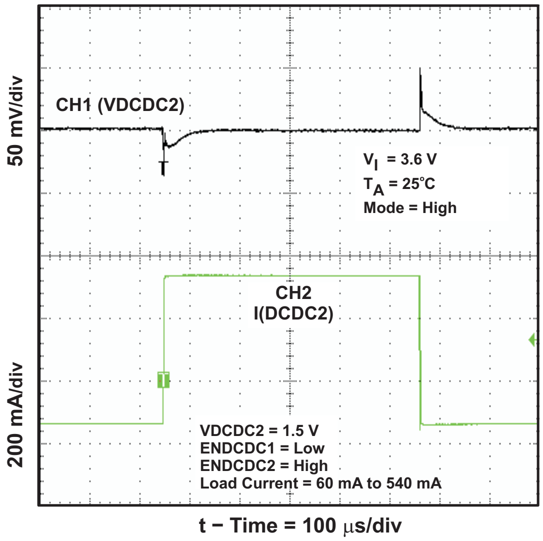

Figure 11.

DCDC2 LOAD TRANSIENT RESPONSE

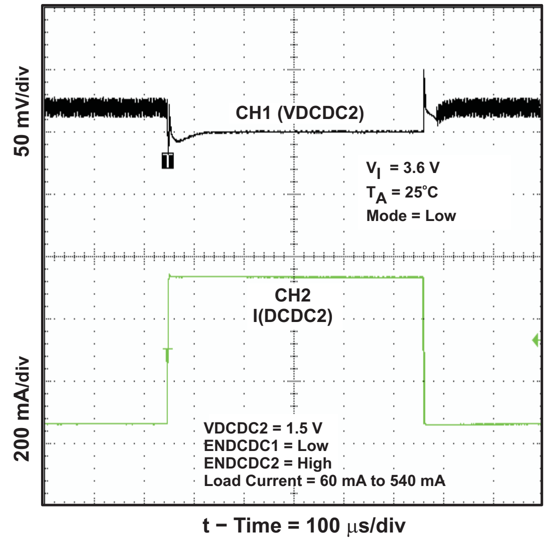

Figure 12.

DCDC1 LINE TRANSIENT RESPONSE

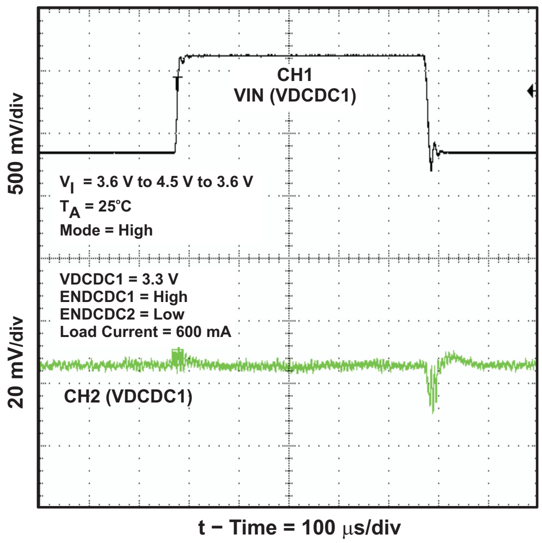

Figure 13.

DCDC2 LINE TRANSIENT RESPONSE

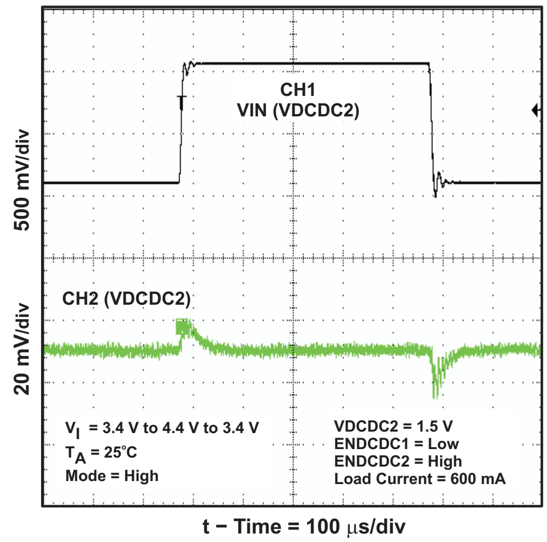

Figure 14.

TYPICAL CHARACTERISTICS (continued)

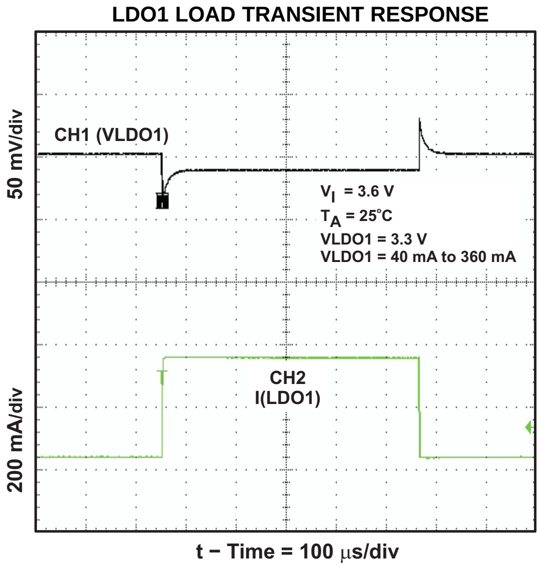

Figure 15.

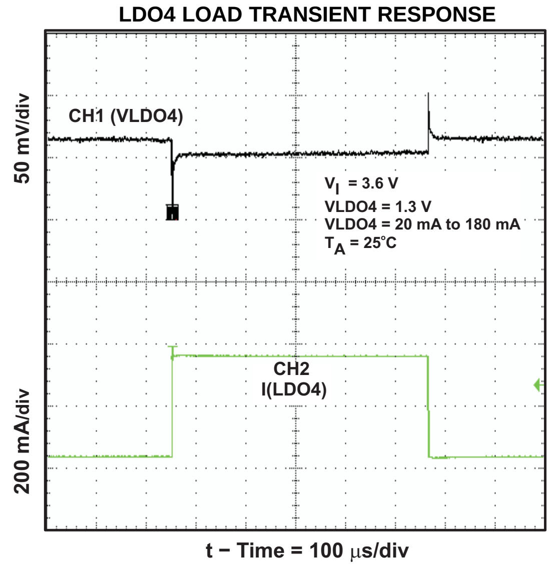

Figure 16.

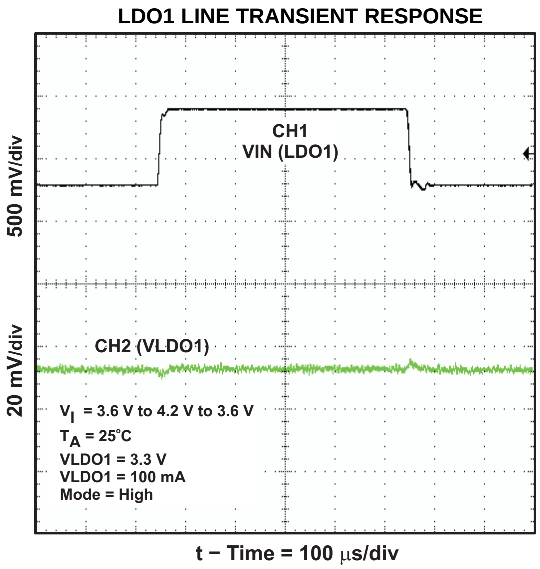

Figure 17.

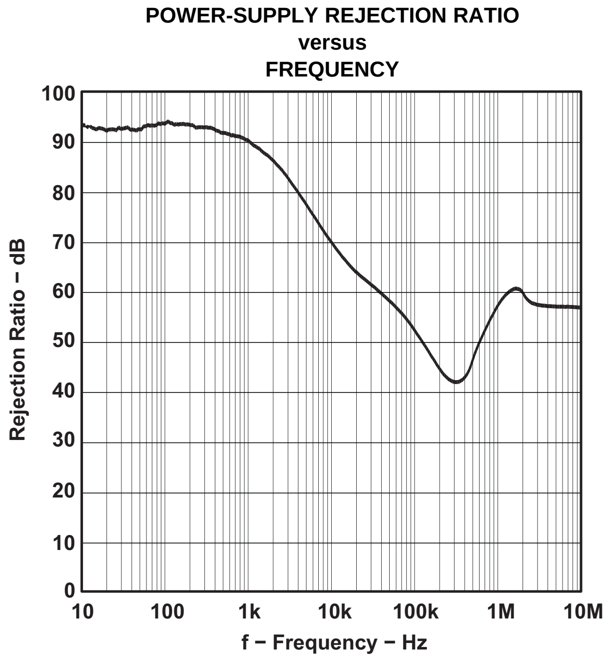

Figure 18.

DETAILED DESCRIPTION

Operation

The TPS6505x-Q1 devices each include two synchronous step-down converters. The converters operate with 2.25-MHz (typical) fixed-frequency pulse-width modulation (PWM) at moderate to heavy load currents. At light load currents, the converters automatically enter power-save mode and operate with PFM (pulse-frequency modulation).

During PWM operation, the converters use a unique fast-response voltage-mode controller scheme with input voltage feed-forward to achieve good line and load regulation, allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the P-channel MOSFET switch turns on, the inductor current ramps up until the current comparator trips, and the control logic turns off the switch. The current-limit comparator turns off the switch if the current exceeds the limit of the P-channel switch. After the adaptive dead time, which prevents shoot-through current, the N-channel MOSFET rectifier turns on, and the inductor current ramps down. The clock signal turning off the N-channel rectifier and turning on the on the P-channel switch initiates the next cycle.

The two dc-dc converters operate synchronized to each other, with converter 1 as the master. A 180° phase shift between converter 1 and converter 2 decreases the input rms current, allowing the use of smaller input capacitors.

DCDC1 Converter

An external resistor divider connected to FB_DCDC1 pin for TPS65050-Q1, TPS65051-Q1, and TPS65054-Q1 sets the converter 1 output voltage. For TPS65052-Q1, with its output voltage fixed to 3.3 V, connect this pin directly to the output. See the *Application Information* section for more details. The maximum output current on DCDC1 is 600 mA for TPS65050-Q1 and TPS65054-Q1. For TPS65051-Q1, TPS65052-Q1, and TPS65056-Q1, the maximum output current is 1 A.

DCDC2 Converter

Connect he VDCDC2 pin directly to the DCDC2 converter output voltage. The DEFDCDC2 pin selects the DCDC2 converter output voltage.

TPS65050-Q1 and TPS65051-Q1: An external resistor divider sets the output voltage. Connect the DEFDCDC2 pin to the external resistor divider.

TPS65052-Q1, TPS65054-Q1, and TPS65056-Q1: Connect the DEFDCDC2 pin either to GND, or to V_{CC}. The converter 2 output voltage defaults to:

Device	DEFDCDC2 = Low	DEFDCDC2 = High
TPS65052-Q1 , TPS65056-Q1	1 V	1.3 V
TPS65054-Q1	1.3 V	1.05 V

Power-Save Mode

Setting the MODE pin to 0 enables the power-save mode. If the load current decreases, the converters enter the power-save mode of operation automatically. During power-save mode, the converters operate with reduced switching frequency in PFM mode, and with a minimum quiescent current to maintain high efficiency. The converters position the output voltage 1% above the nominal output voltage. This voltage-positioning feature minimizes voltage drops caused by a sudden load step.

To optimize the converter efficiency at light load, the TPS6505x-Q1 monitors average current. If in PWM mode, the inductor current remains below a certain threshold, then the device enters power-save mode. Use Equation 1 to calculate the typical threshold:

$$I_{(PFM\_enter)} = \frac{VINDCDC}{32\ \Omega} \tag{1}$$

A. Average output current threshold to enter PFM mode.

$$I_{(PSMDCDC\_leave)} = \frac{VINDCDC}{24\ \Omega} \tag{2}$$

B. Average output current threshold to leave PFM mode.

During power-save mode, a comparator monitors the output voltage. As the output voltage falls below the skip-comparator (skip comp) threshold, the P-channel switch turns on, and the converter effectively delivers a constant current. If the load is below the delivered current, the output voltage rises until it crosses the skip comp threshold again; then all switching activity ceases, reducing the quiescent current to a minimum until the output voltage has dropped below the threshold. If the load current is greater than the delivered current, the output voltage falls until it crosses the skip-comparator-low (skip comp low) threshold set to 1% below nominal V_O; then the device exits power-save mode, and the converter returns to the PWM mode.

These control methods reduce the quiescent current to 12 µA per converter and the switching frequency to a minimum, achieving the highest converter efficiency. The PFM mode operates with low output-voltage ripple. The ripple depends on the comparator delay and the size of the output capacitor; increasing capacitor value decreases the output ripple voltage.

Disable the power-save mode by driving the MODE pin high. In forced-PWM mode, both converters operate with fixed-frequency PWM mode regardless of the load.

Dynamic Voltage Positioning

This feature reduces the voltage under- and overshoots at load steps from light to heavy load and vice versa. It is activated In the power-save mode of operation, running the converter in PFM mode activates dynamic voltage positioning. Dynamic voltage positioning provides more headroom for both the voltage drop at a load step and the voltage increase at a load throw-off, thereby improving load-transient behavior.

At light loads, in which the converters operate in PFM mode, the typical output-voltage regulation is 1% higher than the nominal value. In the event of a load transient from light load to heavy load, the output voltage drops until it reaches the skip-comparator-low threshold, set to 1% below the nominal value, and enters PWM mode. During a release from heavy load to light load, active regulation turning on the N-channel switch minimizes the voltage overshoot.

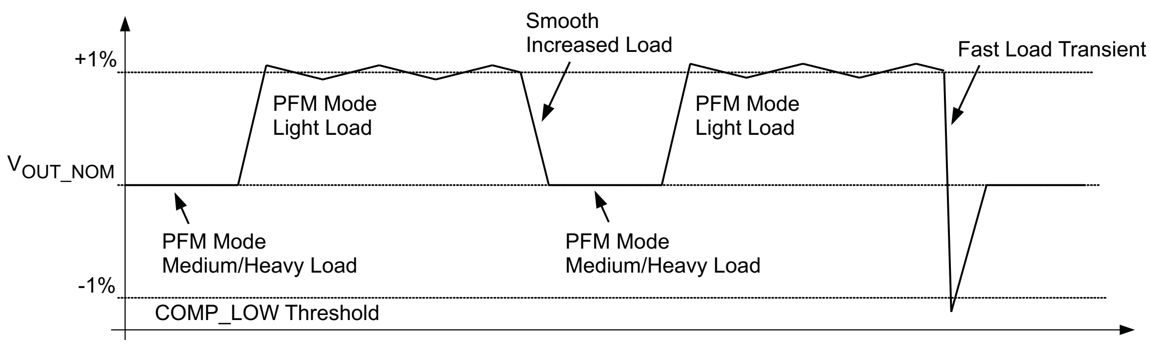

Figure 19. Dynamic Voltage Positioning

Soft Start

The two converters have an internal soft-start circuit that limits the inrush current during start-up. During soft start, control of the output-voltage ramp-up is as shown in Figure 20.

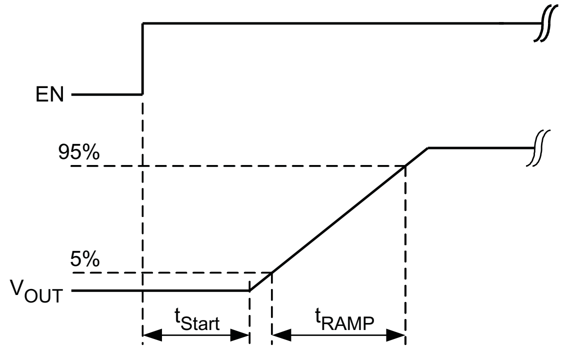

Figure 20. Soft Start

100% Duty-Cycle Low-Dropout Operation

The converters offer a low input-to-output voltage difference while still maintaining operation with the use of the 100% duty-cycle mode. In this mode, the P-channel switch is constantly on. This operational mode is useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range, (that is, the minimum input voltage to maintain regulation depends on the load current and output voltage) and can be calculated as:

$$V_I(min) = V_O(max) + I_O(max) \times (r_{DS(on)}(max) + R_L) \quad (3)$$

with:

- I_O max = maximum output current plus inductor ripple current
- $r_{DS(on)}$ max = maximum P-channel switch $r_{DS(on)}$
- R_L = dc resistance of the inductor
- V_O (max) = nominal output voltage plus maximum output-voltage tolerance

Undervoltage Lockout

The undervoltage-lockout circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery, and disables all internal circuitry. The undervoltage-lockout threshold, sensed at the V_{CC} pin, is typically 1.8 V, maximum 2 V.

Mode Selection

The MODE pin allows mode selection between forced PWM mode and power-save mode for both converters. Connecting this pin to GND enables the automatic PWM and power-save mode of operation. The converters operate in fixed-frequency PWM mode at moderate-to-heavy loads and in the PFM mode during light loads, maintaining high efficiency over a wide load-current range.

Pulling the MODE pin high forces both converters to operate constantly in the PWM mode even at light load currents. The advantage is the converters operate with a fixed frequency that allows simple filtering of the switching frequency for noise-sensitive applications. In this mode, the efficiency is lower compared to the power-save mode during light loads. For additional flexibility, it is possible to switch from power-save mode to forced-PWM mode during operation. This allows efficient power management by adjusting the operation of the converters to the specific system requirements.

Enable

To start up each converter independently, the device has a separate enable pin for each dc-dc converter and for each LDO. If EN_DCDC1, EN_DCDC2, EN_LDO1, EN_LDO2, EN_LDO3, or EN_LDO4 is set to high, the corresponding converter starts up with soft start as previously described.

Pulling the enable pin low forces the device into shutdown, with a shutdown quiescent current as defined in the electrical characteristics. In this mode, the P- and N-Channel MOSFETs turn off, and the entire internal control circuitry switches off. If disabled, internal 350-Ω resistors pull the outputs of the LDOs low, actively discharging the output capacitor. Proper operation requires termination of the enable pins. Do not leave them unconnected.

$\overline{\text{RESET}}$

The TPS65051-Q1, TPS65052-Q1, TPS65054-Q1, and TPS65056-Q1 contain circuitry that can generate a reset pulse for a processor with a 100-ms delay time. The device senses the input voltage for a comparator at the THRESHOLD pin. When the voltage exceeds the threshold, the output goes high with a 100-ms delay time. An external resistor connected to the HYSTERESIS input defines the hysteresis. This circuitry is functional as soon as the supply voltage at V_{CC} exceeds the undervoltage-lockout threshold. The TPS6505x-Q1 has a shutdown current (all dc-dc converters and LDOs are off) of 9 µA.

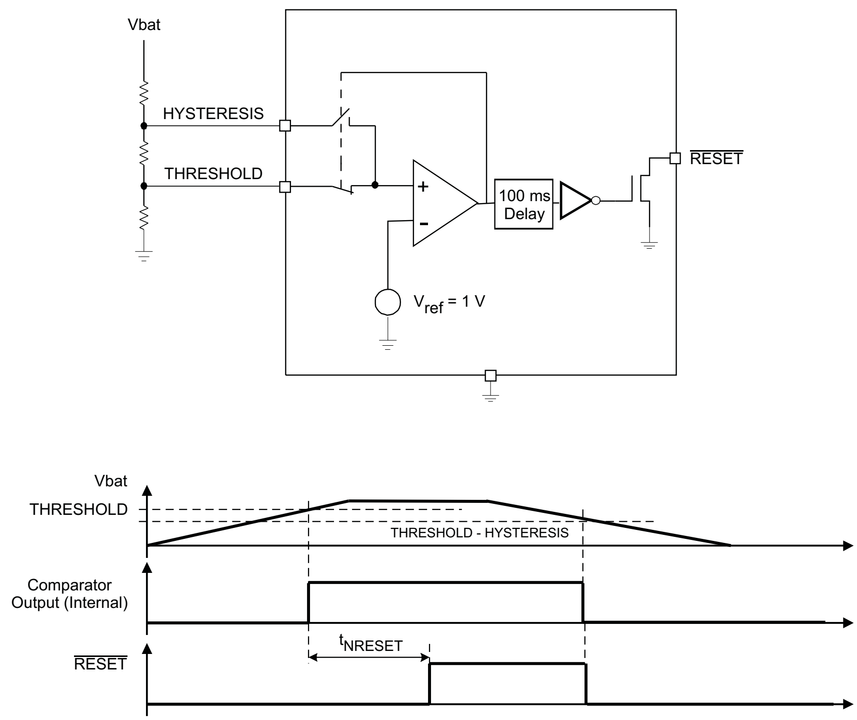

Figure 21. $\overline{\text{RESET}}$ Pulse Circuit

Push-Button ON-OFF (PB-ON-OFF)

The TPS65050-Q1 provides a PB-ON-OFF functionality instead of supervising a voltage with the threshold and hysteresis inputs. The device holds the output at PB_OUT low after application of voltage at V_{CC}. Only after pulling the input at PB_IN high once, the output driver at PB_OUT goes to its inactive state, driven high with its external pullup resistor. Further low-high pulses at PB_IN toggle the status of the PB_OUT output. Connecting the PB_OUT output to the enable input of the converters allows shutdown and start-up of the converters with a single push on a button.

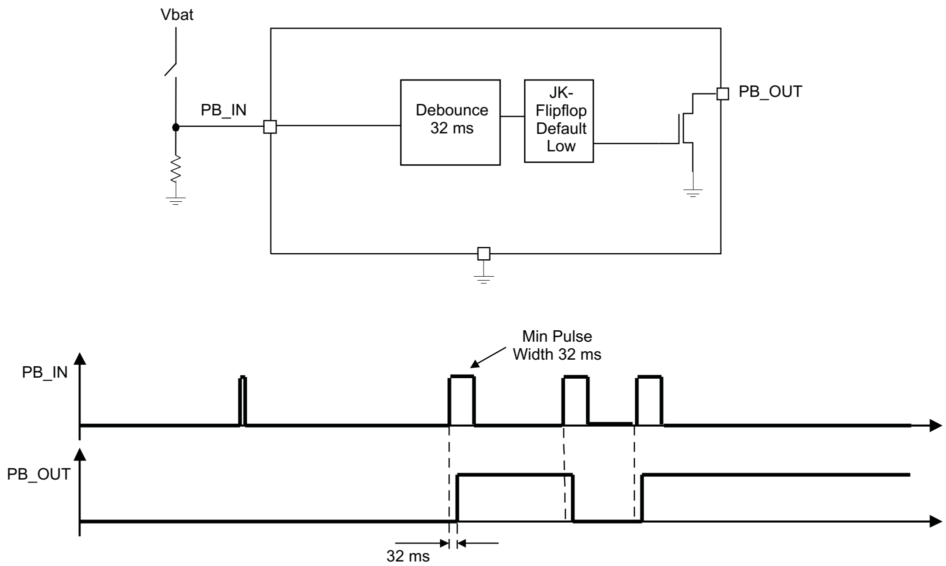

Figure 22. Push-Button Circuit

Short-Circuit Protection

All outputs are short-circuit protected with a maximum output current as defined in the *Electrical Characteristics*.

Thermal Shutdown

As soon as the junction temperature, T_J, exceeds 150°C (typically) for the dc-dc converters, the device goes into thermal shutdown. In this mode, the P- and N-channel MOSFETs turn off. The device continues its operation when the junction temperature falls below the thermal shutdown hysteresis again. A thermal shutdown for one of the dc-dc converters disables both converters simultaneously.

The thermal shutdown temperature for the LDOs is typically 140°C. Therefore, an LDO used to power an external voltage never heats up the chip high enough to turn off the dc-dc converters. If one LDO exceeds the thermal shutdown temperature, all LDOs turn off simultaneously.

Low Dropout Voltage Regulators

The design of the low-dropout voltage regulators allows them to operate well with small ceramic input and output capacitors. They operate with input voltages down to 1.5 V. The LDOs offer a maximum dropout voltage of 280 mV at rated output current. Each LDO supports a current-limit feature. The EN_LDO1, ENLDO2, EN_LDO3, and EN_LDO4 pins enable the LDOs. In TPS65050-Q1 and TPS65052-Q1, the the use of four pins sets the output voltage of the LDOs. Connect the DEFLDO1 to DEFLDO4 pins either to GND or Vbat (V_{CC}) to define a set of output voltages for LDO1 to LDO4 according to Table 1. Connecting the DEFLDOx pins to a voltage different from GND or V_{CC} causes increased leakage current into V_{CC}. In TPS65051-Q1 and TPS65054-Q1, the use of external resistor dividers sets the output voltage of the LDOs .

TPS65050-Q1 and TPS65052-Q1 default voltage options are adjustable with DEFLDO4…DEFLDO1 according to Table 1.

Table 1. Default Options

DEFLDO1	DEFLDO2	DEFLDO3	DEFLDO4	VLDO1	VLDO2	VLDO3	VLDO4
				400-mA LDO 1.8 V–5.5 V Input	400-mA LDO 1.8 V–5.5 V Input	200-mA LDO 1.5 V–5.5 V Input	200-mA LDO 1.5 V–5.5 V Input
0	0	0	0	3.3 V	3.3 V	1.85 V	1.85 V
0	0	0	1	3.3 V	3.3 V	1.5 V	1.5 V
0	0	1	0	3.3 V	2.85 V	2.85 V	2.7 V
0	0	1	1	3.3 V	2.85 V	2.85 V	2.5 V
0	1	0	0	3.3 V	2.85 V	2.85 V	1.85 V
0	1	0	1	3.3 V	2.85 V	1.85 V	1.85 V
0	1	1	0	3.3 V	2.85 V	1.5 V	1.5 V
0	1	1	1	3.3 V	2.85 V	1.5 V	1.3 V
1	0	0	0	3.3 V	2.85 V	1.1 V	1.3 V
1	0	0	1	2.85 V	2.85 V	1.85 V	1.85 V
1	0	1	0	2.7 V	3.3 V	1.2 V	1.2 V
1	0	1	1	2.5 V	3.3 V	1.5 V	1.5 V
1	1	0	0	2.5 V	3.3 V	1.5 V	1.3 V
1	1	0	1	1.85 V	1.85 V	1.35 V	1.35 V
1	1	1	0	1.8 V	2.5 V	3.3 V	2.85 V
1	1	1	1	1.2 V	1.8 V	1.1 V	1.3 V

APPLICATION INFORMATION

Output-Voltage Setting

Converter 1 (DCDC1)

An external resistor network can set the output voltage of converter 1. Calculate the output voltage using Equation 4,

$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \tag{4}$$

with an internal reference voltage V_{ref}, 0.6 V.

TI recommends setting the total resistance of R1 + R2 to less than 1 MΩ. The resistor network connects to the input of the feedback amplifier, therefore requiring a small feed-forward capacitor in parallel with R1. A typical value of 47 pF is sufficient.

Converter 2 (DCDC2)

Select the output voltage of converter 2 as follows:

- Adjustable output voltage defined with external resistor network on pin DEFDCDC2. This option is available for TPS65050-Q1 and TPS65051-Q1.
- Two default fixed output voltages selectable by pin DEFDCDC2, see Table 2. This option is available for TPS65052-Q1, TPS65054-Q1, and TPS65056-Q1.

Table 2. Default Fixed Output Voltages

Converter 2	DEFDCDC2 = Low	DEFDCDC2 = High
TPS65050-Q1	—	—
TPS65051-Q1	—	—
TPS65052-Q1	1 V	1.3 V
TPS65054-Q1	1.3 V	1.05 V
TPS65056-Q1	1 V	1.3 V

Calculation of the adjustable output voltage is similar to that for the DCDC1 converter. TI recommends setting the total resistance of R3 + R4 to less than 1 MΩ. Route the DEFDCDC2 line separate from noise sources, such as the inductor or the L2 line. Connect the VDCDC2 line directly to the output capacitor. As VDCDC2 is the sense pin for the output of L2, there is no need for a feedforward capacitor in conjunction with R3.

Using an external resistor divider at DEFDCDC2:

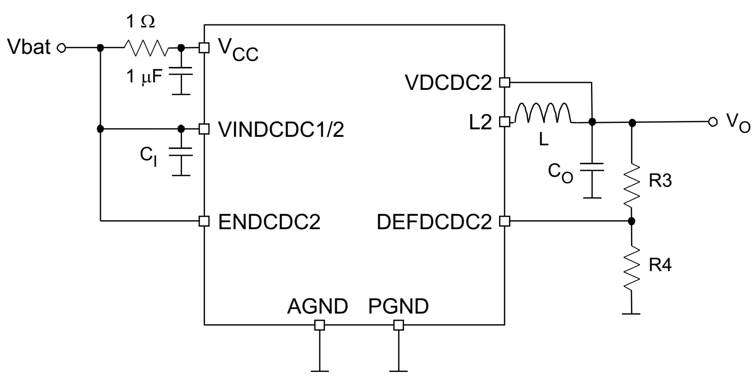

Figure 23. External Resistor Divider

$V_{(DEFDCDC2)} = 0.6\ V$

$$V_O = V_{(DEFDCDC2)} \times \frac{R3 + R4}{R4} \qquad R3 = R4 \times \left(\frac{V_O}{V_{(DEFDCDC2)}} \right) - R4 \tag{5}$$

See Table 3 for typical resistor values:

Table 3. Typical Resistor Values

OUTPUT VOLTAGE	R3	R4	NOMINAL VOLTAGE	Typical CFF
3.3 V	680 kΩ	150 kΩ	3.32 V	47 pF
3 V	510 kΩ	130 kΩ	2.95 V	47 pF
2.85 V	560 kΩ	150 kΩ	2.84 V	47 pF
2.5 V	510 kΩ	160 kΩ	2.51 V	47 pF
1.8 V	300 kΩ	150 kΩ	1.8 v	47 pF
1.6 V	200 kΩ	120 kΩ	1.6 V	47 pF
1.5 V	300 kΩ	200 kΩ	1.5 V	47 pF
1.2 V	330 kΩ	330 kΩ	1.2 V	47 pF

Output Filter Design (Inductor and Output Capacitor)

Inductor Selection

The two converters operate with a 2.2-μH output inductor. A designer can use larger or smaller inductor values to optimize the performance of the device for specific operation conditions. The selected inductor must be rated for its dc resistance and saturation current. The dc resistance of the inductance directly influences the efficiency of the converters. Therefore, select an inductor with lowest dc resistance for highest efficiency. The minimum inductor value is 1.5 μH, but the circuit requires an output capacitor of 22 μF minimum in this case. For an output voltage above 2.8 V, TI recommends an inductor value of 3.3 μH minimum. Lower values result in an increased output-voltage ripple in PFM mode.

Equation 6 calculates the maximum inductor current under static load conditions. The saturation-current rating of the inductor should be higher than the maximum inductor current as calculated with Equation 6. This recommendation is because during heavy load transient the inductor current rises above the calculated value.

$$\Delta I_L = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \qquad I_L(max) = I_O(max) + \frac{\Delta I_L}{2} \tag{6}$$

with:

- f = Switching frequency (2.25-MHz typical)
- L = Inductor value
- $\Delta\ I_L$= Peak-to-peak inductor ripple current
- $I_L max$ = Maximum inductor current

The highest inductor current occurs at maximum V_I. Open-core inductors have a soft saturation characteristic, and they can normally handle higher inductor currents versus a comparable shielded inductor.

A more-conservative approach is to select the inductor current rating just for the maximum switch current of the corresponding converter. Give consideration to the difference in the core material from inductor to inductor, which has an impact on the efficiency, especially at high switching frequencies. See Table 4 and the typical applications for possible inductors.

Table 4. Tested Inductors

Inductor Type	Inductor Value	Supplier
LPS3010	2.2 µH	Coilcraft
LPS3015	3.3 µH	Coilcraft
LPS4012	2.2 µH	Coilcraft
VLF4012	2.2 µH	TDK

Output-Capacitor Selection

The advanced fast-response voltage-mode control scheme of the two converters allows the use of small ceramic capacitors with a value of 22-µF (typical), without having large output-voltage undershoots and overshoots during heavy load transients. TI recommends ceramic capacitors having low ESR values, which result in the lowest output-voltage ripple.

If ceramic output capacitors are used, the capacitor RMS ripple current rating always meets the application requirements. For completeness, the RMS ripple current is calculated as:

$$I_{(RMSCout)} = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (7)$$

At nominal load current, the inductive converters operate in PWM mode, and the overall output voltage ripple is the sum of the voltage spike caused by the output-capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V_O = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \times \left(\frac{1}{8 \times C_O \times f} + ESR\right) \quad (8)$$

where the highest output voltage ripple occurs at the highest input voltage V_I.

At light load currents, the converters operate in power-save mode and the output-voltage ripple depends on the output-capacitor value. The internal comparator delay and the external capacitor set the output-voltage ripple. The typical output-voltage ripple is less than 1% of the nominal output voltage.

Input-Capacitor Selection

The nature of the buck converters having a pulsating input current requires a low-ESR input capacitor for best input-voltage filtering and minimizing the interference with other circuits caused by high input-voltage spikes. The converters require a ceramic input capacitor of 10 µF. Increase the input capacitor as desired for better input-voltage filtering, without any limit.

Table 5. Possible Capacitors

Capacitor Value	Size	Supplier	Type
2.2 µF	0805	TDK C2012X5R0J226MT	Ceramic
2.2 µF	0805	Taiyo Yuden JMK212BJ226MG	Ceramic
10 µF	0805	Taiyo Yuden JMK212BJ106M	Ceramic
10 µF	0805	TDK C2012X5R0J106M	Ceramic
10 µF	0603	Taiyo Yuden JMK107BJ106MA	Ceramic

Low-Dropout Voltage Regulators (LDOs)

An external resistor network sets the output voltage of all four LDOs in TPS65051-Q1, TPS65054-Q1, and TPS65056-Q1. Calculate the output voltage using Equation 9:

$$V_O = V_{ref} \times \left(1 + \frac{R5}{R6}\right) \tag{9}$$

with an internal reference voltage, V_{ref}, of 1 V (typical).

TI recommends setting the total resistance of R5 + R6 to less than 1 MΩ. Typically, there is no feedforward capacitor needed at the voltage dividers for the LDOs.

$$V_O = V_{(FB\_LDOs)} \times \frac{R5 + R6}{R6} \qquad R5 = R6 \times \left(\frac{V_O}{V_{(FB\_LDOs)}}\right) - R6 \tag{10}$$

Typical resistor values:

Table 6. Typical Resistor Values

OUTPUT VOLTAGE	R5	R6	NOMINAL VOLTAGE
3.3 V	300 kΩ	130 kΩ	3.31 V
3 V	300 kΩ	150 kΩ	3 V
2.85 V	240 kΩ	130 kΩ	2.85 V
2.8 V	360 kΩ	200 kΩ	2.8 V
2.5 V	300 kΩ	200 kΩ	2.5 V
1.8 V	240 kΩ	300 kΩ	1.8 v
1.5 V	150 kΩ	300 kΩ	1.5 V
1.3 V	36 kΩ	120 kΩ	1.3 V
1.2 V	100 kΩ	510 kΩ	1.19 V
1.1 V	33 kΩ	330 kΩ	1.1 V

LAYOUT CONSIDERATIONS

Application Circuits

PB_IN and Sequencing

One can use the PB_OUT pin to enable one or several converters. After power up, the PB_OUT pin is low, and pulls down the enable pins connected to PB_OUT; EN_DCDC1, and EN_LDO1 in Figure 24. Pulling PB_IN to V_{CC} for longer than 32 ms turns off the PB_OUT pin. Hence, a pullup resistor to V_{CC} pulls the enable pins high, enabling the DCDC1 converter and LDO1. The enable signal for DCDC2 and LDO2 to LDO4 is the output voltage of DCDC1 ($V_{OUT}1$). The battery ($V_{(bat)}$) directly powers LDO1 with its output voltage of 3.3 V and LDO2 for an output voltage of 2.5 V. To save power, the input voltage for the lower voltage rails at LDO3 and LDO4 derives from the output of the step-down converters, keeping the voltage drop at the LDOs low to increase efficiency. Because the output of DCDC1 powers LDO3 and LDO4, the total output current on $V_{OUT}1$, LDO3, and LDO4 must not exceed the maximum rating of DCDC1.

Figure 25 shows the power up timing for this application.

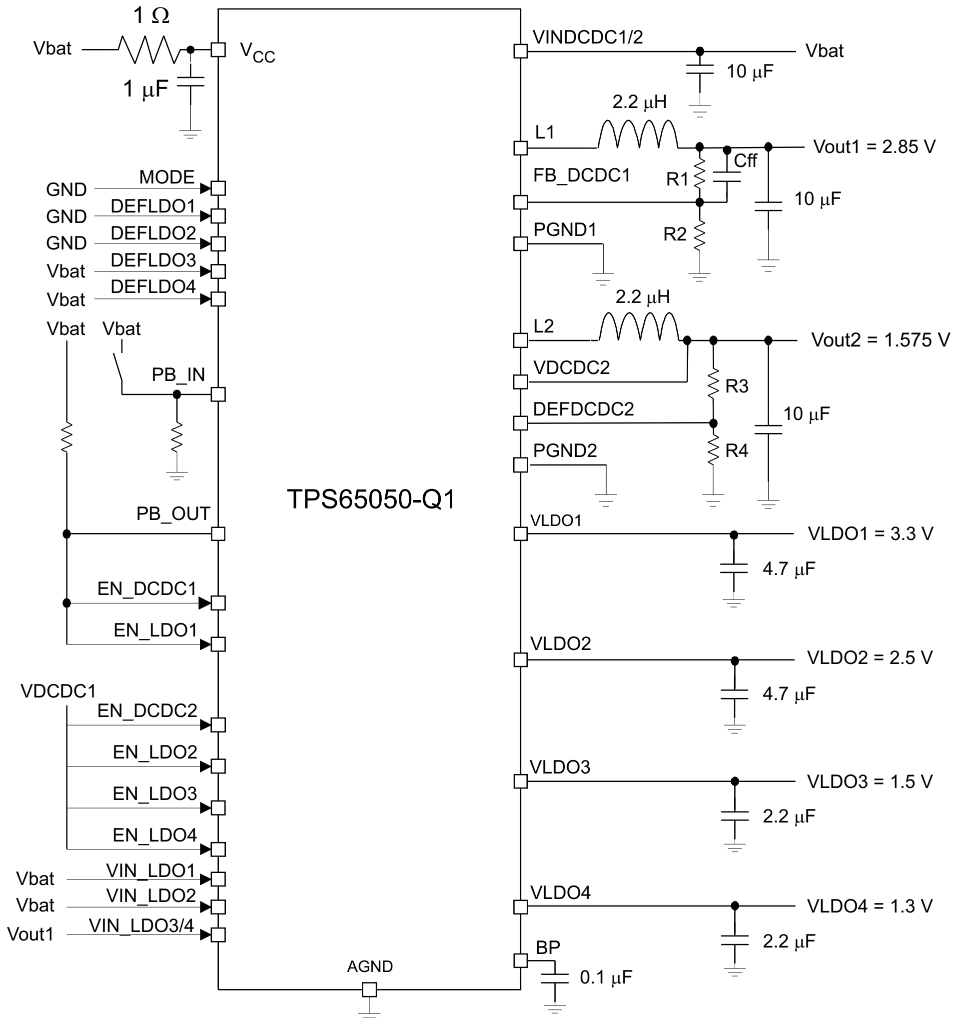

Figure 24. PB_OUT Circuit

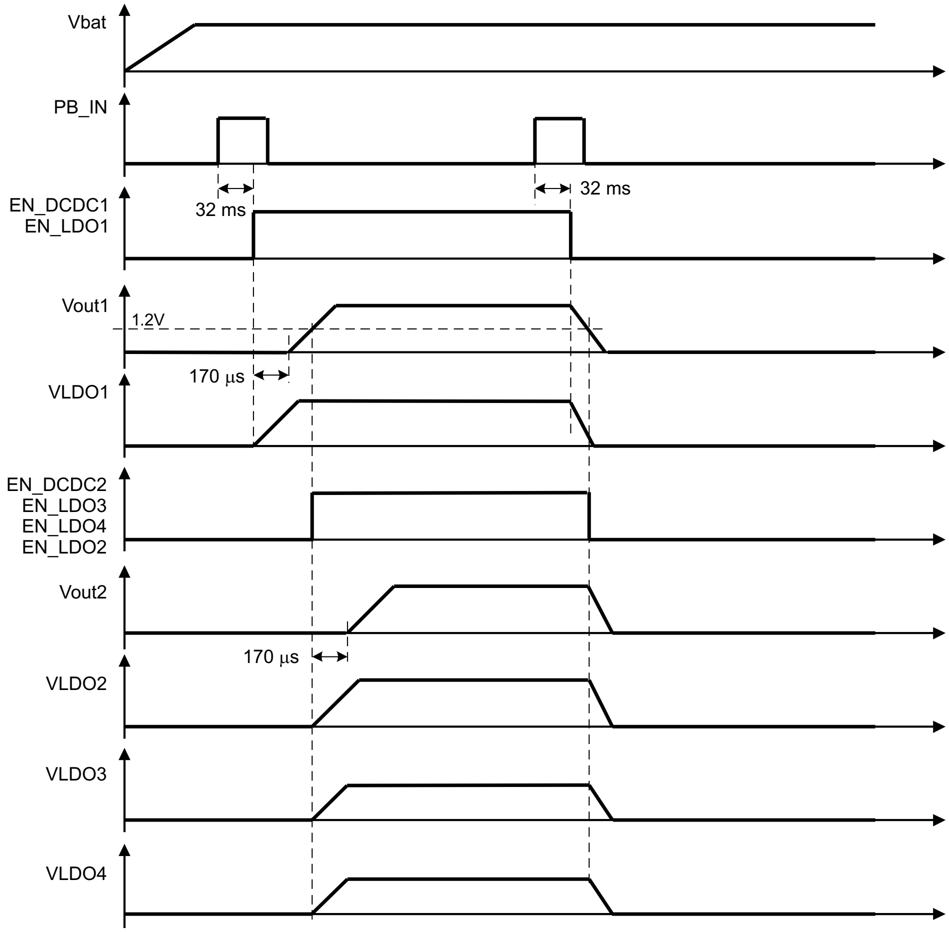

Figure 25. Power-Up Timing

$\overline{\text{RESET}}$

TPS65051-Q1, TPS65052-Q1, TPS65054-Q1, and TPS65056-Q1 contain a comparator for supervising a voltage connected to an external voltage divider, and generating a reset signal if the voltage is lower than the threshold. The rising-edge delay is 100 ms at the open-drain $\overline{\text{RESET}}$ output. Calculate the values for the external resistors R3 to R5 as follows:

V_L = lower voltage threshold

V_H = higher voltage threshold

V_{REF} = reference voltage (1 V)

Example:

- V_L = 3.3 V
- V_H = 3.4 V

  Set R5 = 100 kΩ

  → R3 + R4 = 240 kΩ

  → R4 = 3.03 kΩ

  → R3 = 237 kΩ

$$R3 + R4 = R5 \times \left(\frac{V_H}{V_{ref}} - 1 \right)$$

$$R4 = R5 \times \frac{V_H - V_L}{V_L} \quad (11)$$

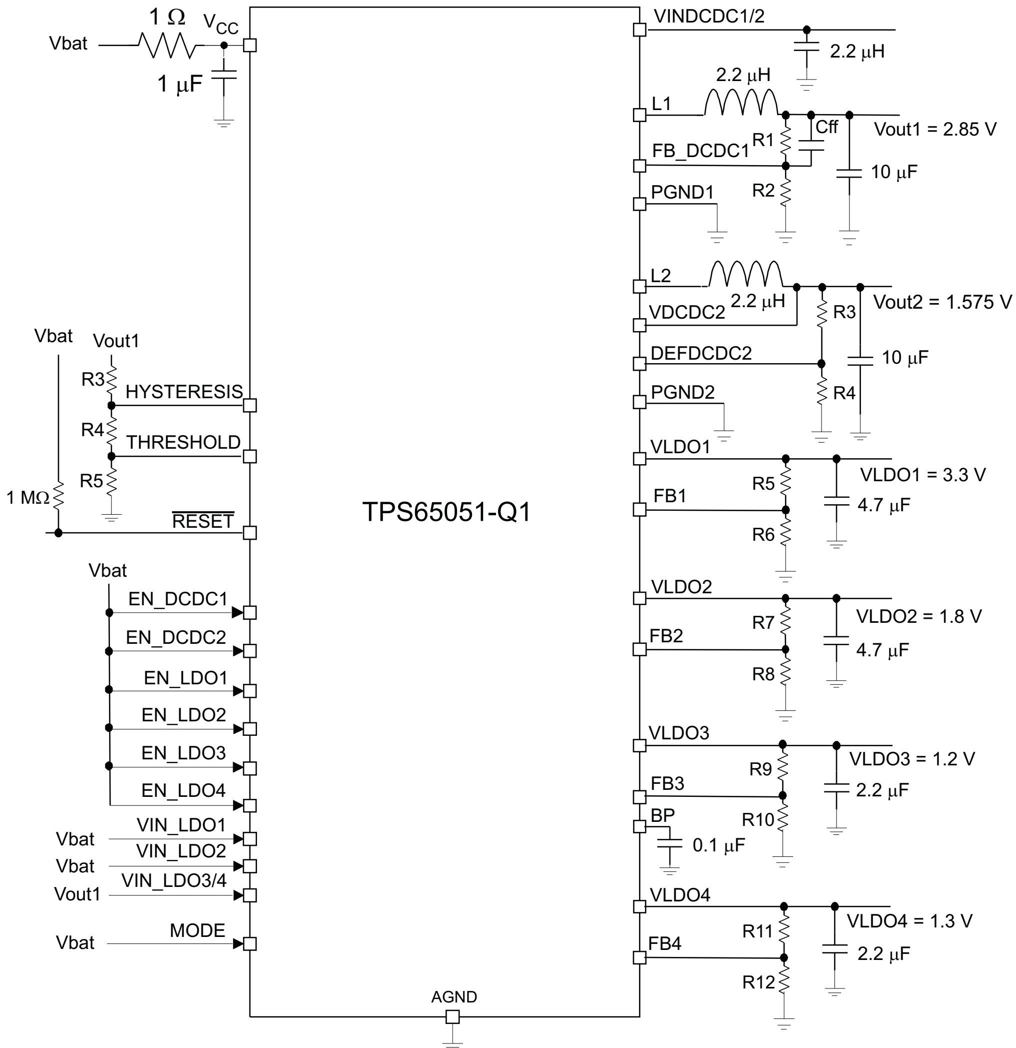

Figure 26. $\overline{\text{RESET}}$ Circuit

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS65051QRSMRQ1	ACTIVE	VQFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 65051Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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OTHER QUALIFIED VERSIONS OF TPS65051-Q1 :

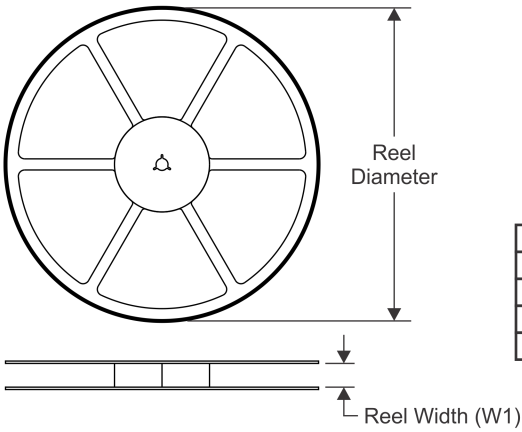
- Catalog: TPS65051

NOTE: Qualified Version Definitions:

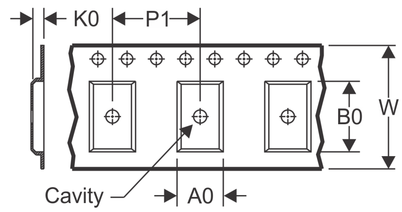
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

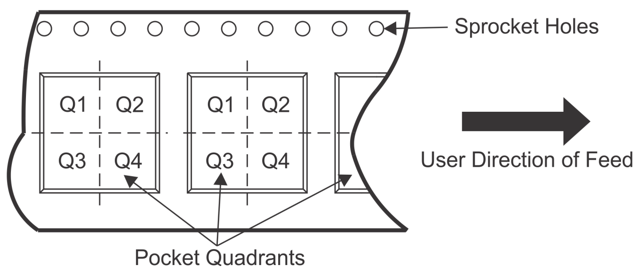


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

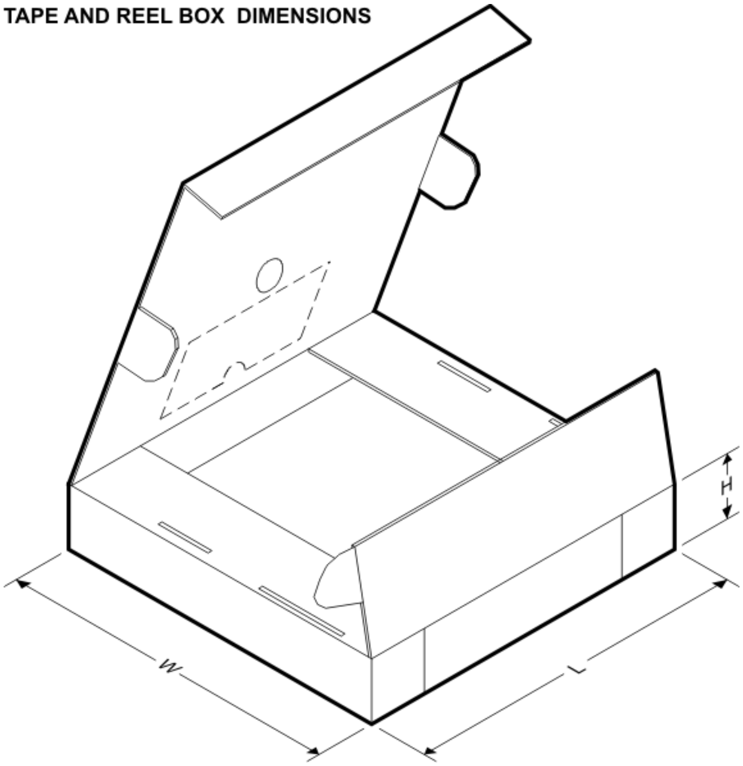
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65051QRSMRQ1	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

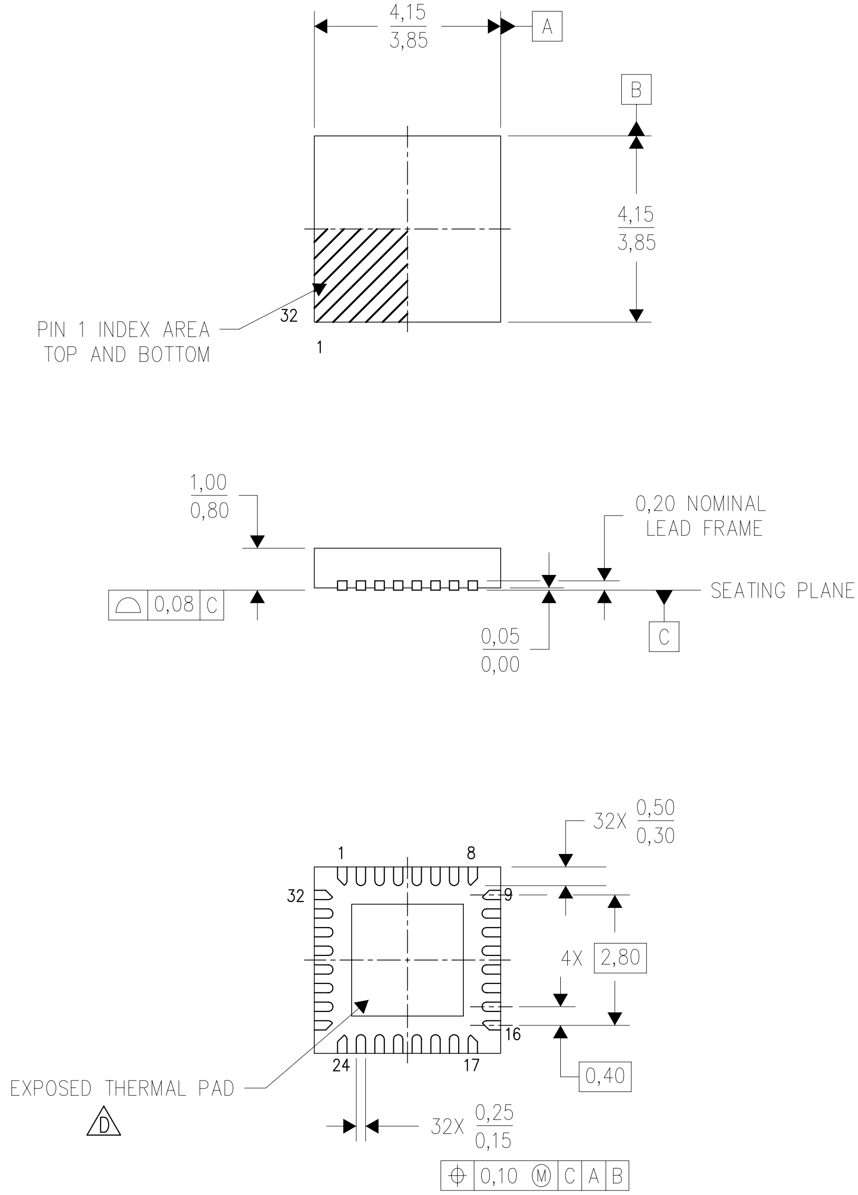
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65051QRSMRQ1	VQFN	RSM	32	3000	367.0	367.0	35.0

RSM (S-PVQFN-N32) PLASTIC QUAD FLATPACK NO-LEAD



4207560/B 03/10

NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.

B. This drawing is subject to change without notice.

C. QFN (Quad Flatpack No–Lead) Package configuration.

D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

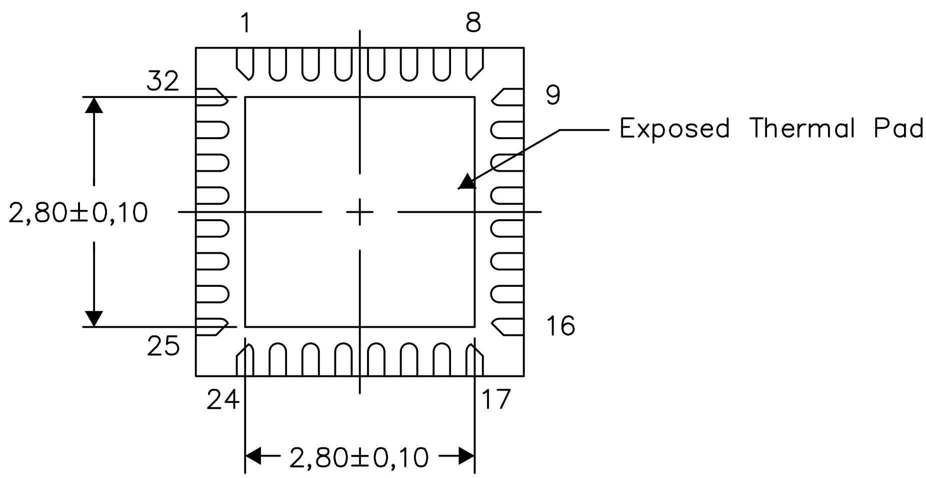
RSM (S-PVQFN-N32) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



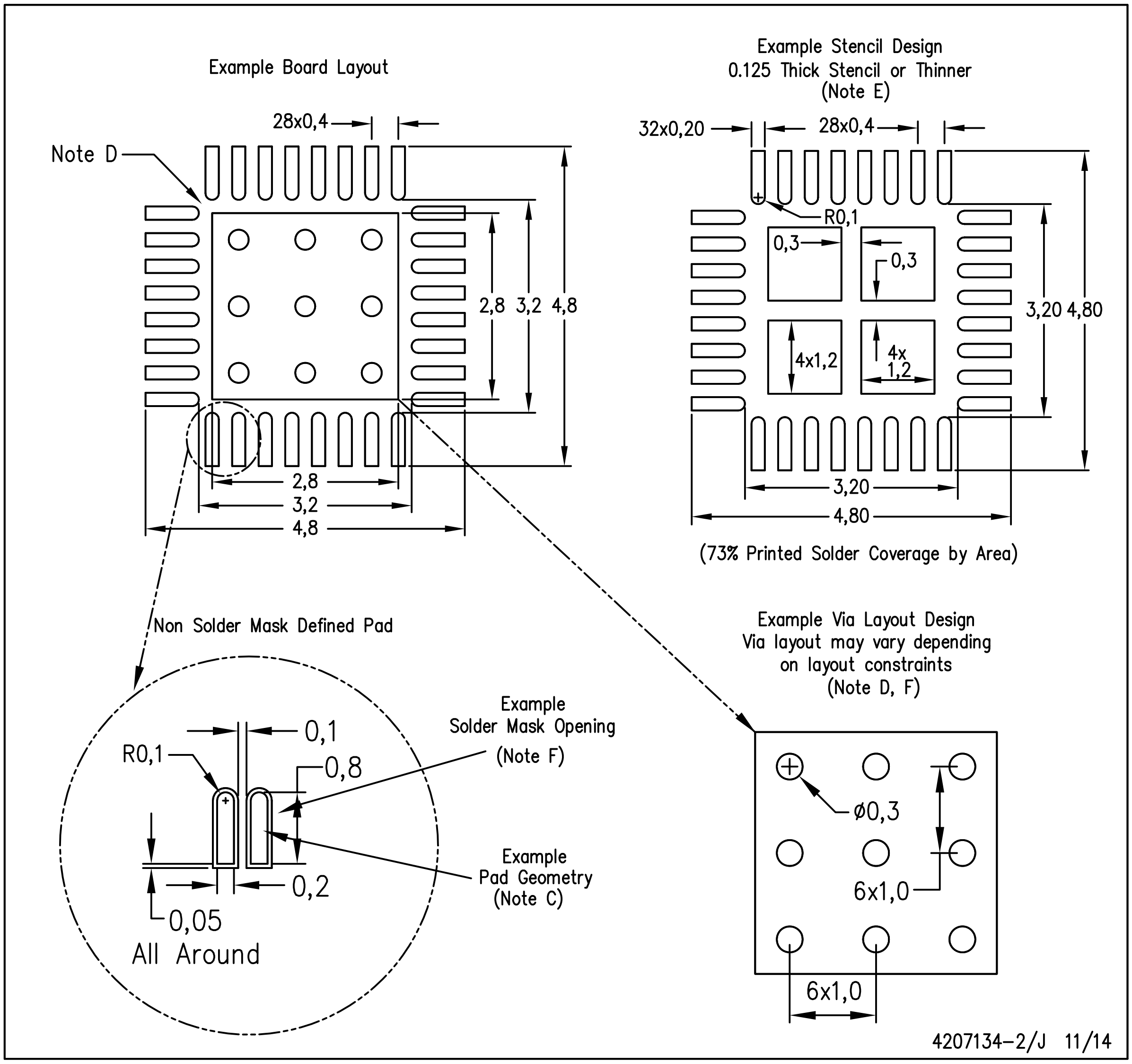
Bottom View

Exposed Thermal Pad Dimensions

4207868-2/I 07/14

NOTE: All linear dimensions are in millimeters

RSM (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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